A Nanowatt Area-Efficient 16-Channel Bandpass Filterbank using Floating Active Capacitance Multiplier for Acoustic Signal Processing

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***Abstract*—This paper introduces an area-efficient nanowatt 16-channel bandpass filterbank tailored for acoustic signal processing in Artificial Internet of Things (AIoT) sensor systems. Integration of a floating active capacitance multiplier (FACM) adeptly addresses the inherent challenge of increased area in source-follower-based filters due to their larger capacitance. Compared to conventional gm-C circuits, this work offers reduced power consumption, a more straightforward structure, and tunability. In a standard 0.13-µm CMOS process, simulations reveal the filterbank's frequency range spans from 90 Hz to 5 kHz with a gain of 17dB, and a total power consumption of 97nW for the 16 channels. When benchmarked against contemporary BPFs, this work achieves an unparalleled area efficiency of 0.038mm^2/channel and superior linearity. Such a compact and energy-efficient design offers a competitive solution for analog feature extraction in edge AI applications.**

Keywords—ultra-low-power, bandpass filterbank, compact, capacitance multiplier, acoustic signal, AIoT.

I. INTRODUCTION

The rapid advancement of the Artificial Internet of Things (AIoT) networks is driving the rise of pervasive intelligent sensing. In the IoT era, advanced auditory processing systems, encompassing but not limited to voice activity detectors (VAD) and keyword spotting, have flourished for years. The analog front-end plays a pivotal role in the AIoT architecture, sensing sensor outputs and facilitating signal amplification and conditioning. Historically, this front-end primarily consisted of amplifiers and ADC blocks, relegating the bulk of the information processing to digital circuits. However, recent research trends are increasingly pivoting towards analog signal processing due to its superior energy efficiency compared to digital circuits[1-5]. Fig. 1 illustrates a quintessential analog-intensive signal processing chain utilized in acoustic inference sensing systems. Within this chain, acoustic feature extraction (AFE) is predominantly analog. Notably, within the analog AFE, the filterbank is paramount[6]. As a core block for feature extraction, it often consumes the most power, and its Q-factor significantly influences the accuracy for diverse auditory processing applications[2].

In analog AFEs, the bandwidth of filters predominantly lies below 8kHz[1-6]. Achieving such low cutoff frequencies typically necessitates large capacitors, leading to increased chip area and associated costs. Active capacitance multipliers (ACM) offer a compelling solution, amplifying capacitance via active circuits[7,8]. Based on operational paradigms, ACMs fall into Current Mode (C-Mode) and Voltage Mode (V-Mode); by interfacing, they're distinguished as grounded ACM or floating ACM (FACM). Yet, most ACM studies target uW power regimes. Transferring these designs to nW circuits can confront issues like sub-threshold regions and misaligned internal operating points, compromising ACM functionality. In recent years, research on nW level ACMs has been sparse, with only a few notable works, specifically references [9,10], but they exclusively address grounded ACMs. This renders them unsuitable for direct application in commonly differential BPF circuits.

This work was supported by the Agency for Science, Technology and Research (A*STAR), Singapore under the Nanosystems at the Edge Programme, grant no. A18A1b0055.

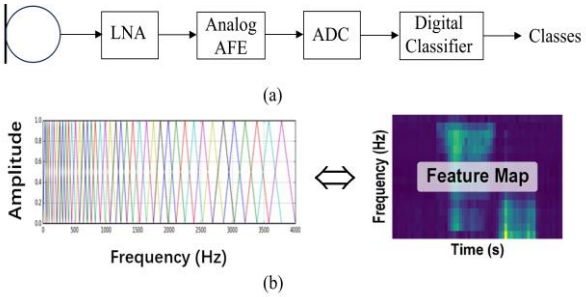

Fig.1. (a) Analog signal processing chain in acoustic inference sensing systems. (b) Filter bank for acoustic feature extraction.

This paper introduces an ultra-low-power 16-channel source-follower-based BPF bank. A novel FACM architecture is proposed to address the challenges posed by increased area due to large capacitors. Furthermore, the deployment of CMFB at low supply voltages markedly enhances the circuit's linearity. The remainder of this paper is structured as follows: Section II details the architecture of the proposed 16-channel bandpass filterbank and delves into the design specifics of the circuit blocks. Section III presents the post-layout simulation results. Finally, Section IV offers conclusions and summarises the work.

II. 16-CHANNEL BANDPASS FILTERBANK WITH FLOATING ACTIVE CAPACITANCE MULTIPLIER

A. Linear Tunable Source-follower-based Bandpass Filter

To streamline the analysis, Fig.2 presents the equivalent circuit of the core filter circuit in the following filterbank. Transistors M_1 and M_2 form a super-source-follower structure, while the floating capacitors C_1 and C_2 provide the poles. The current from source I_2 should exceed that from I_1. Different from the traditional super-source-follower lowpass filter [10], this work ingeniously utilizes the drain of M_1 as the output point, leveraging two poles to form a 2-order bandpass filter. All transistors operate in the subthreshold

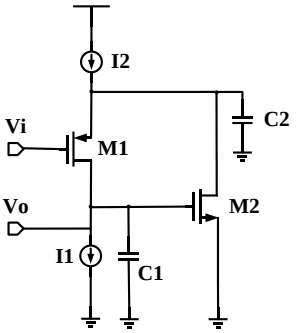

Fig.2. The single-ended equivalent circuit of SF-C based filter.

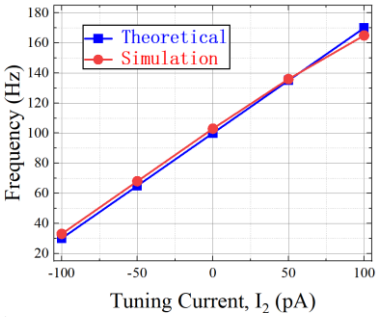

Fig.4. Cutoff frequency versus the tuning biasing current.

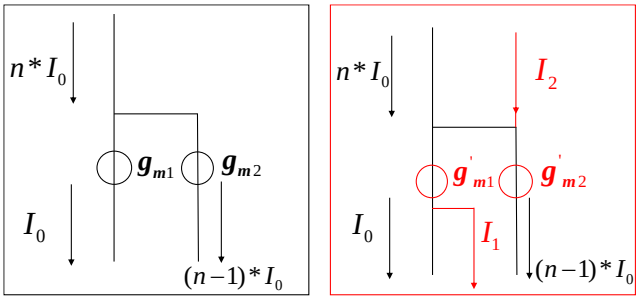

Fig.3. The simplified diagram of current distribution.(a) before tuning. (b) after tuning.

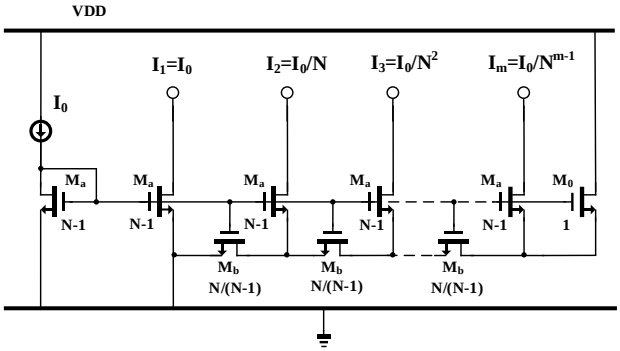

Fig.5. The current divider of NMOS version in the bandpass filterbank.

region. Based on small signal model analysis, the s-domain transfer function is given by

$$H(s) = \frac{\frac{g_{m1}}{C_1}s}{s^2 + \frac{g_{ms1}}{C_2}s + \frac{g_{ms1}g_{m2}}{C_1C_2}} \quad (1)$$

where $g_{ms1} = g_{m1} + g_{mb1} = (1+\eta)g_{m1}$ is the source transconductance and η is the body effect trans-conductance ratio (η ~0.2-0.5). From (1), the expressions of cutoff frequency f_0, quality factor Q and the passband gain A can be given by

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{g_{ms1}g_{m2}}{C_1C_2}}, Q = \sqrt{\frac{g_{m2}C_2}{g_{ms1}C_1}}, A = \frac{C_2g_{m1}}{C_1g_{ms1}} \quad (2)$$

Obviously, the performance is dependent on the body effect of M_1. Selecting M_1 as a PMOS can effectively mitigate this influence. If the body effect is neglected ($g_{ms1} \approx g_{m1}$), it can be observed that the key parameters are closely related to g_{m1} and g_{m2}. This forms the foundation for the tuning in this work. In the subthreshold region, the drain current is approximately proportional to the transconductance. Therefore, by adjusting the two current sources in Fig.2, the tuning of g_m can be achieved. Fig.3 shows the simplified diagram of current distribution before and after tuning by adjusting the current sources.

Assuming n is 5 first, after tuning, the transconductance, center frequency and Q-factor are:

$$\begin{aligned} & g'_{m1} = \frac{I_0 + I_1}{I_0}g_{m1}, \text{and } g'_{m2} = \frac{4I_0 - I_1 + I_2}{4I_0}g_{m2} \\ & \Rightarrow f'_0 = f_0\sqrt{\frac{(I_0+I_1)(4I_0-I_1+I_2)}{4I_0^2}}, Q' = Q\sqrt{\frac{4I_0-I_1+I_2}{4(I_0+I_1)}} \end{aligned} \quad (3)$$

During the tuning process, it is generally desirable to only alter a single variable while keeping others constant. Given that the DC gain remains unaffected by current variations, when tuning center frequency, it is necessary to keep the Q-factor consistent before and after the tuning, that is:

$$\text{let } Q' = Q, \text{then } f'_0 = f_0\sqrt{\frac{(I_0+I_1)(4I_0-I_1+I_2)}{4I_0^2}} = f_0\left(\frac{I_1}{I_0}+1\right) \quad (4)$$

From equation (4), it can be observed that the tuned center frequency f_0 is directly proportional to the tuning current I_1, thereby constituting a linear tuning, which is crucial for the overall tuning of the subsequent filterbank. Fig.4 shows the simulation and theoretical values for this linear tuning.

B. Current Divider

It can be observed from equations (2), the filter's cutoff frequency is directly proportional to the equivalent transconductance, g_m. And the drain current I_d is also proportional to g_m. Therefore, the proposed 16-channel BPF bank requires exponentially scaled bias currents to generate exponential I_d in excepted log distribution frequency range. Fig. 5 illustrates the current divider circuit [12,13], which is designed to generate exponentially scaled bias currents $I_{1,ch1}$, $I_{1,ch2}$,…, $I_{1,ch16}$ and $I_{2,ch1}$, $I_{2,ch2}$,…, $I_{2,ch16}$ across the 16 channels.

In the figure, all NMOS transistors have the same size, yet the ratio of size ratios varies. This is achieved by the series and parallel combination of transistors. In this design, we have m=16 and N=1.298, then N-1 equals 1/3 (three transistors in series), and N/(N-1) equals 4 (four transistors in parallel, i.e., multiplier number equals 4). In this case, $I_1=I_0$, $I_2=I_0/1.298$, $I_3=I_0/1.298^2$, …, $I_{16}=I_0/1.298^{15}$. Then the exponentially scaled bias currents for the 16 channels are obtained. It's worth mentioning that, in the PMOS version of the current bias used in this work, the body of all PMOS

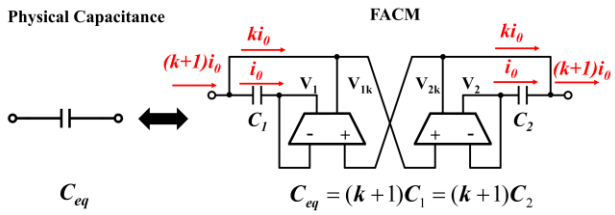

Fig.6. The equivalent diagram of the physical capacitance and floating active capacitance multiplier.

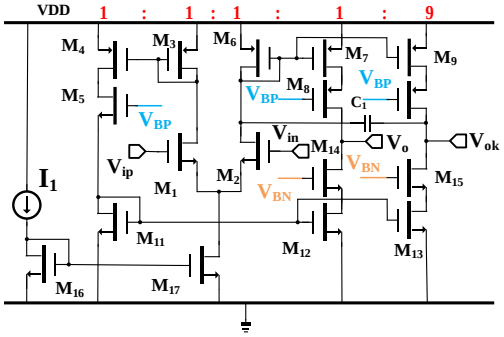

Fig.7. The proposed amplifier in FACM.

transistors are connected to the VDD/2 voltage to reduce V_{th}. This is particularly important for low-voltage designs.

C. *Floating Active Capacitance Multiplier*

The circuit configuration to implement the floating capacitor multiplier is shown in Fig.6. The principle of the FACM is similar to the current-mode grounded ACM [14-19], and it consists of two differential input-output amplifiers and two physical capacitors. In Fig.6, k is the current amplification factor of the $V_{1,2}$ port compared to $V_{1k,2k}$, and $C_{1,2}$ represents the value of the small physical capacitor. The FACM achieves a large equivalent capacitance C_{eq} using a small physical capacitors $C_{1,2}$.

The differential amplifier circuit is shown in Fig.7. And the amplification ratio of the current mirror is illustrated by the red numerals in the figure. M_5, M_8, M_{10}, and M_{14} are utilized in a Common Source Common Gate (CSCG) cascode structure to increase the output impedance. Similar to the grounded ACM [10], the output impedance determines the low-frequency point of the floating ACM, which is particularly noteworthy for low-frequency applications. The capacitor C_1 is used as a Miller compensation capacitor to improve stability. In terms of stability simulation for the proposed amplifier, the open-loop gain and phase of V_k is simulated. The DC gain is 65dB. With the same compensation capacitor (0.3pF MIMCAP), the phase margin of proposed amplifier is 78° and the phase margin of the conventional compensation capacitor methods [16,20] is 1.8°. This work achieves a significantly higher phase margin.

D. *Proposed 16-channel Bandpass Filterbank with FACM*

Fig.8 illustrates the proposed BPF with FACM, which combines the linear tuning BPF from Section II.A and the FACM from Section II.C. $M_{1,2,3,4}$ constitute the core source-follower-based BPF. M_5 and M_6 serve as source follower buffers to enhance the load capability of the BPF. I_1, I_3, I_4, I_6 are current sources provided by current divider in the Section II.B. They are exponentially scaled for different channels.

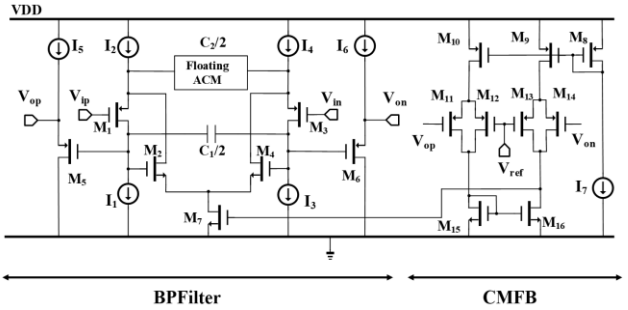

Fig.8. The proposed bandpass filter with FACM and CMFB.

The small capacitor, $C_1/2$, is directly implemented using a physical capacitor, while the larger capacitor, $C_2/2$, is realized through FACM to conserve area.

The Common-Mode Feedback (CMFB) circuit on the right detects the minute difference between the output common-mode voltage and V_{ref}, and feeds back to the filter. Compared to the BPF in Section II.A, CMFB stabilizes the gate voltage of M_2 and M_4 at a reasonable value, ensuring that the key transistors continue to operate in the subthreshold region. This improves the linearity for large signal inputs under low supply voltage. In addition, M_7 also utilizes source degeneration technology to enhance linearity.

III. Results And Disscusions

The proposed 16-channel bandpass filterbank with FACM is implemented in a commercial 0.13-μm CMOS process. The power supply voltage is 0.6 V. Fig.9 presents the layout of the proposed 16-channel BPF, occupying an area of 0.82mm². In Fig.8, $I_2=I_4=I_7=12nA/1.298^n$, and $I_1=I_3=6nA/1.298^n$, where n is the channel number. MIM capacitance $C_1/2$ is 1pF. And the equivalent capacitance $C_2/2$ is 8pF, which is produced by two 0.8pF MIM capacitors and a FACM with a multiplier factor of 10. Furthermore, since the power consumption of the ACM itself is comparable to that of the BPF, in order to maintain a compact area while saving power, this work has channels 1 to 6 of the BPF use FACM technology, while channels 7 to 16 reduce the current and capacitance to half of their theoretical values to keep the center frequency unchanged. The total power consumption of the proposed 16-channel BPF bank is 97nW, and the breakdown of power consumption is shown in Fig.10. From the DC operating point simulation, the CMFB operates effectively within an input span of 75mV to 518mV, adequate for the designated BPF. Moreover, Fig.11 showcases the quiescent output voltages of the BPF across 15 corners, with and without CMFB. The results underscore that the proposed CMFB approach diminishes the maximum output voltage fluctuation from 129mV to a minimal 16mV, which substantially bolsters linearity.

The AC response of the 16-channel BPF bank is depicted in Fig.13 when Q-factor is 3.2 and 10. The bandwidth of this filter bank ranges from 92Hz to 5060Hz, with a gain of 17dB. In this depiction, the red and blue curve correspond to Q-factors of 3.2 and 10, respectively. Importantly, there's a trade-off in selecting the Q value, balancing the power consumption and feature extraction efficiency of the BPF. For comparative purposes in this work, unless otherwise stated, a Q value of 3.2 is adopted. In the Fig. 14, the blue curve represents the magnitude curve of the equivalent capacitance generated by the FACM. The bandwidth of this capacitance is significantly higher than the center frequency of channel 6 to ensure sufficient margin.

TABLE II. BENCHMARK WITH PRIOR ARTS OF THE SINGLE CHANNEL BANDPASS FILTER

	This work		2021 JSSC [2]	2021 BioCAS [21]	2018 TCAS-I [22]	2015 NEWCAS [23]	2007 TBioCAS [24]
Process(μm)	**0.13**		0.065	0.18	0.35	0.18	0.35
Topology	**tunable-SSF-C with FACM**		boost g_m-FVF-C	g_m-C	OTA with HDQDPs	g_m-C	g_m-C
	1st filter	**16th filter**					
VDD(V)	**0.6**		0.6	1	1.8	1	1
Order	**2**		2	2	2	4	6
f_0(Hz)	**92**	**5060**	100-5k	950	2k	1000	670
Gain(dB)	**17**	**16.5**	13	-1.5	0	0	0
Q	**3.2**	**3.2**	2	1.3-1.8	0.96	4	NA
Integrated IRN(μVrms)	**27**	**7.6**	30-50	207(inband)	72.93	177(inband)	50.12
THD @input signal level	**1%@ 40mV$_{pp}$**	**1%@ 40mV$_{pp}$**	NA	NA	42.8dB (0.7%)	1%@ 120mV$_{in,rms}$	1%@ 40mV$_{pp}$
DR(dB)	**54.4**	**65.4**	NA	51.98	NA	53.6	49
Power of single channel(nW)	**9.3**	**8.4**	14(16-ch.)	13.2	107.2	6	68
FOM[a] (10^{-13}J)	**5.6**	**0.08**	NA	1.3	NA	0.28	3.4
Area(mm^2)	**0.038/channel**		NA	0.08	0.12	NA	0.234
Application	**Acoustic Signal**		Acoustic Signal	Cochlear Implants	Biomedical Applications	Biomedical Applications	Acoustic Signal

[a] FoM=(Power*VDD)/(n*fc*DR), where n is the order of the filter. [15]

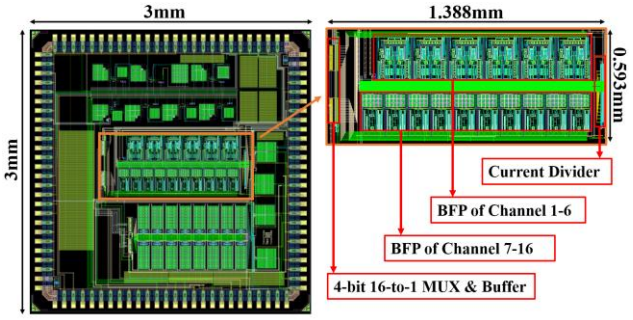

Fig.9. The layout of the proposed 16-channel bandpass filterbank.

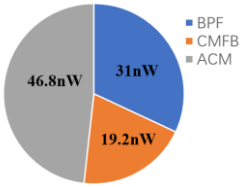

Fig.10. The breakdown of 16-channel BPF bank.

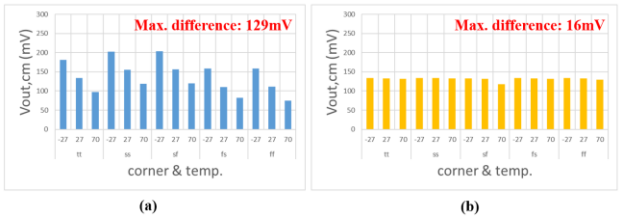

Fig.11. The simulated output quiescent voltages of the BPF in 15 corners (a) without CMFB (b) with CMFB.

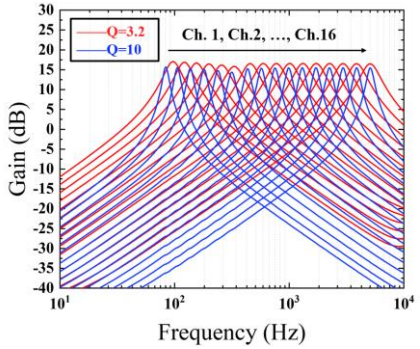

Fig.13. The AC response of 16-channel BPF bank when Q is 3.2 & 10.

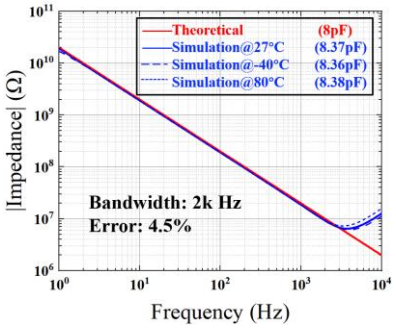

Fig.14. The AC response of the equivalent capacitance of the FACM.

TABLE I. SUMMARY OF CORNER, TEMPERATURE AND VOLTAGE VARIATIONS FOR THE GAIN OF CH. 7.

Temp. (°C)	**-40**			**27**			**80**		
VDD (V)	**TT**	**SS**	**FF**	**TT**	**SS**	**FF**	**TT**	**SS**	**FF**
0.54	16.6	16.7	16.5	16.5	16.6	16.4	15.9	16.4	15.3
0.6	16.7	16.7	16.5	16.5	16.6	16.4	15.8	16.3	15.3
0.66	16.7	16.7	16.5	16.5	16.6	16.4	15.2	16.1	14.1

Table I presents the gain of Channel 7 subjected to temperature, corner and voltage variations. Channel 7 is selected due to its lower current drive and the absence of CMFB for internal voltage stabilization. The choice of gain is made as, unlike Q-factor and frequency, it is not tunable. And the performance of the proposed bandpass filterbank with FACM is summarized and compared with other state-of arts in Table II. From the comparison, it can be observed that, due to the implementation of the CMFB and FACM technology, this work possesses the highest dynamic range and the smallest area. It is imperative to highlight that within the table, there exists an 11dB discrepancy between the DR values of ch.1 and ch.16 from this work. This deviation is attributed to the distinct calculation approach employed for IIRN. In the current work, the IIRN computation initiates from 1Hz. If, analogous to [21,23], one solely focuses on in-band noise computation, the DR values for filters across different channels should be closely aligned.

IV. CONCLUSIONS

This paper implements a nanowatt, compact and tunable 16-channel bandpass filterbank. Within the frequency range pertinent to acoustic signals, this design surpasses conventional g_m-C filters in both linearity and compactness. Most analog AFE architectures traditionally feature one or two amplifier stages preceding the filterbank. This work offers a sophisticated solution for analog AFE in AIoT

sensor systems, emphasizing ultra-low power operation without the integral requirement for amplifiers.

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