nature communications

Article

https://doi.org/10.1038/s41467-025-64579-5

Scalable transition metal dichalcogenide memtransistor arrays with Schottky-barrier control for energy-efficient artificial neural networks

Received: 26 May 2025

Accepted: 22 September 2025

Published online: 28 October 2025

Check for updates

Xiangyu Hou[1,7] ✉, Wei Zhang[1,7], Sisheng Duan[1], Tengyu Jin[2] ✉, Xiangrui Geng[1], Ming Lin[3], Yichen Cai[1], Jingyu Mao[4], Yizhuo Luo[1], Jinlong Zhu[5], Junhao Lin[5] & Wei Chen[1,4,6] ✉

Memtransistors that integrate memristor and transistor functionalities are promising candidates for scalable, energy-efficient neuromorphic computing. However, achieving high performance in memtransistor arrays—particularly in terms of resistive switching ratio, uniformity, and scalability—remains a significant challenge for practical deployment in artificial neural networks. Here, we present scalable memtransistor arrays based on transition metal dichalcogenides (TMDCs), where the Schottky barrier is precisely controlled by modulating vacancy distribution and migration behavior. This approach enables a substantial improvement in the resistive switching ratio, reaching 10^5 through gate modulation. The device-to-device variation is maintained below 6.8%, and the power consumption is as low as 1 pJ per operation. These devices demonstrate high performance in artificial neural network applications, achieving greater than 98% accuracy in image recognition tasks. Furthermore, the devices exhibit remarkable scalability, with a cell size as small as $4.65\,F^2$, and can be further miniaturized by adjusting the channel size without affecting the switching performance. This work highlights the potential of TMDC-based memtransistor arrays for energy-efficient, high-performance artificial neural networks, offering a scalable solution for next-generation neuromorphic computing hardware.

Artificial neural networks (ANNs) are one of the foundations of modern artificial intelligence (AI), enabling breakthroughs in image recognition, natural language processing, and real-time decision-making[1,2]. Conventional von Neumann architectures, which based on a central processing unit (CPU) and a memory, face increasing challenges in meeting the growing demand for high-speed data processing and energy efficiency, making them unsuitable for power-constrained environments such as edge AI and autonomous systems. Neuromorphic computing as a computing-in-memory architecture has been proposed to overcome the limitations of conventional accelerators for

[1]Department of Chemistry, National University of Singapore, Singapore, Singapore. [2]Shanghai Key Laboratory of High Temperature Superconductors, Department of Physics, Shanghai University, Shanghai, China. [3]Institute of Materials Research and Engineering (IMRE), Agency for Science, Technology and Research (A*STAR), Singapore, Singapore. [4]Department of Physics, National University of Singapore, Singapore, Singapore. [5]Department of Physics, Southern University of Science and Technology, Shenzhen, China. [6]National University of Singapore (Suzhou) Research Institute, Suzhou, China. [7]These authors contributed equally: Xiangyu Hou, Wei Zhang. ✉e-mail: houxy@nus.edu.sg; tyjin@shu.edu.cn; phycw@nus.edu.sg

advanced ANNs[3,4]. While application-specific integrated circuits (ASICs) based on complementary metal-oxide-semiconductor (CMOS) technology have been developed to enable in-memory computing, their reliance on tens of devices to emulate a single synapse results in significant area overhead, limiting their scalability for large-scale neuromorphic systems[5]. To realize hardware-efficient ANNs, neuromorphic devices should support high-density integration, low-power operation, and precise weight modulation.

Memtransistors, which integrate memristor and transistor functionalities in a single unit, have emerged as promising candidates for hardware-efficient ANNs[6–8]. Unlike conventional transistors that require external memory elements, or memristors that need additional circuitry such as one-transistor-one-memristor (1T1M) configurations[9–12], memtransistors leverage a multi-terminal architecture that allows for area efficiency, dynamic conductance tuning, and multilevel resistive states, making them well-suited for ANN-based processing. Beyond their roles in ANN acceleration, memtransistors also hold potential for multi-mode sensing-computation integration, where electrical and optical signals, as well as environmental factors, can be simultaneously processed within a unified architecture[13,14].

Two-dimensional (2D) transition metal dichalcogenides (TMDCs), with their atomic-scale thickness, present a promising platform for the high-density integration of memtransistors[15–18]. Particularly, as channel lengths of 2D field-effect transistor (FET) shrink below 100 nm[19–21], 2D memtransistors have the potential to surpass Moore's law, offering an avenue toward ultra-compact, beyond-CMOS neuromorphic processors through 2D-CMOS hybrid integration. Current memtransistors based on monolayer (ML) TMDCs primarily exploit Schottky barrier modulation to achieve resistive switching, particularly in polycrystalline or defect-rich MoS_2, where vacancy migration under an external electric field dynamically alters the Schottky barrier[7,13,22–27]. However, the random and uncontrolled nature of defect distributions has hindered the scalability of ML TMDC memtransistors, restricting most reported devices to micrometer-scale channel lengths, with few demonstrations of large-scale memtransistor arrays. The non-uniform vacancy migration behavior in polycrystalline or defect-rich materials further exacerbates significant device-to-device variability and poor fabrication yield, which obscures the underlying switching mechanisms and introduces large performance variability, severely limiting the practical deployment of 2D memtransistor-based hardware. Despite increasing demand for single-crystalline TMDCs, their application in memtransistors remains limited, primarily due to the prevalence of polycrystalline materials, which restricts the choice of viable channel materials and hinders broader attention to the field. Therefore, achieving precise Schottky barrier modulation and scalability in single-crystalline TMDC memtransistors is crucial for realizing high-density and highly uniform arrays, paving the way for their integration into next-generation neuromorphic computing hardware.

Here we demonstrate scalable MoS_2 memtransistor arrays with precise Schottky barrier modulation, achieved through controlled oxidation processes that regulate vacancy distribution and migration behavior. The fabricated memtransistors exhibit a substantial improvement in the resistive switching ratio, reaching 10^4, and further enhancement to 10^5 with 7 distinct resistive states through gate modulation. The array features a channel length scaled down to 500 nm with a cell size as small as $4.65F^2$, and according to the Schottky barrier model, the channel length can be further miniaturized without compromising the switching performance. To validate its neuromorphic computing capabilities, we design and implement a hardware-based ANN utilizing a 5 × 5 memtransistor array, where device states are directly mapped to synaptic weights. The device-to-device variation is maintained below 6.8%, and the device yield can achieve 100%, ensuring high uniformity and reliability. The ANN is trained and tested for image processing and recognition tasks, demonstrating over 98% accuracy in classification. This memtransistor fabrication approach is also applicable to mechanically exfoliated MoS_2 and $MoTe_2$, indicating a versatile fabrication strategy for 2D TMDC memtransistors. Our results highlight the potential of high-density, low-power 2D memtransistor arrays for next-generation neuromorphic processors, bridging the gap between emerging material innovations and practical AI hardware applications.

Results

Schottky-barrier controlled memtransistor arrays

To fabricate a Schottky-barrier controlled memtransistor, a critical aspect of our approach is the selective oxidation treatment, which modulates sulfur vacancies in designated regions, leading to spatially controlled Schottky barriers engineering. Figure 1a, b illustrates the fundamental device structure and fabrication process. The memtransistor consists of a MoS_2 channel integrated into a multi-terminal configuration, allowing for both gate-controlled conductance tuning and memory functionality. The oxidized area is designed and controlled by etching PMMA films. The oxidation level is controlled by the duration of the oxygen plasma treatment. Details of the memtransistor fabrication is provided in the Methods. We fabricate 12 × 6 arrays of ML and few-layer (FL, ~ three layers) MoS_2-based memtransistor with varying channel lengths on SiO_2/Si substrates (Fig. 1c, d and Supplementary Fig. 1). The cross-sectional transmission electron microscopy (TEM) images confirm the structural modifications of a memtransistor cell after plasma treatment (Fig. 1e). The high-resolution images (Fig. 1f) show the oxidized and pristine MoS_2 are near the left and right electrodes, respectively. Sulfur vacancies causing lattice disorders and thickness thinning (about 1.6 nm) can be observed in the treated MoS_2 area, while the untreated area can find a three-layer MoS_2 and the thickness of about 2.1 nm. Through a systematic study of the thickness variation with treatment time, it was found that the sample thins by 0.1 nm for every second of treatment (Supplementary Fig. 2). This is consistent with the TEM data, which shows a 0.5 nm reduction after 5 seconds of treatment. Corresponding energy dispersive X-ray spectroscopy (EDS) reveals the elemental distributions in the device (Fig. 1g). Sulfur and oxygen contents in the treated region are lower and higher than in the untreated region, respectively, confirming the localized oxidation effects and ensuring reproducibility and reliability in large-scale integration. Using this approach, we successfully fabricate individual memtransistor devices based on mechanically exfoliated MoS_2 and $MoTe_2$ (Supplementary Figs. 3 and 4) and scalable array structures on CVD-grown ML and FL MoS_2.

Mimicking biological synapses is crucial for hardware-based ANNs. As illustrated in Fig. 2a–d and Supplementary Fig. 5, the MoS_2 memtransistor shows the artificial synaptic characteristics, such as short- and long-term plasticity (STP and LTP). As the duration time or number of the programming pulse raise, transition from STP to LTP can be observed, suggesting that the MoS_2 memtransistor cell can emulate a single synapse for neuromorphic computing (Fig. 2b, c). Robust and tunable conductance states can be achieved through pulse modulation (Fig. 2d), which is critical for implementing synaptic weight tuning in ANN architectures. To demonstrate the practical application of our memtransistor arrays in neuromorphic computing, we fabricate a 5 × 5 hardware-efficient ANNs for image processing and recognition (Fig. 2e–g). In comparison with state-of-the art memtransistors that based on vacancy migration[7,22–25,27], ferroelectric materials[28], ion-induced phase change[29,30] and moiré synapse[31], our approach offers a significant advantage in terms of resistive switching ratio, uniformity, scalability and energy efficiency (Fig. 2h). These results suggest that Schottky-barrier-engineered MoS_2 memtransistor arrays have the potential to achieve the requirements of the International Roadmap for Devices and System (IRDS)[32].

To elucidate the underlying mechanism of Schottky barrier modulation, Fig. 3 presents atomic-scale and spectroscopic investigations. The memtransistor is designed based on vacancy migration to

https://doi.org/10.1038/s41467-025-64579-5

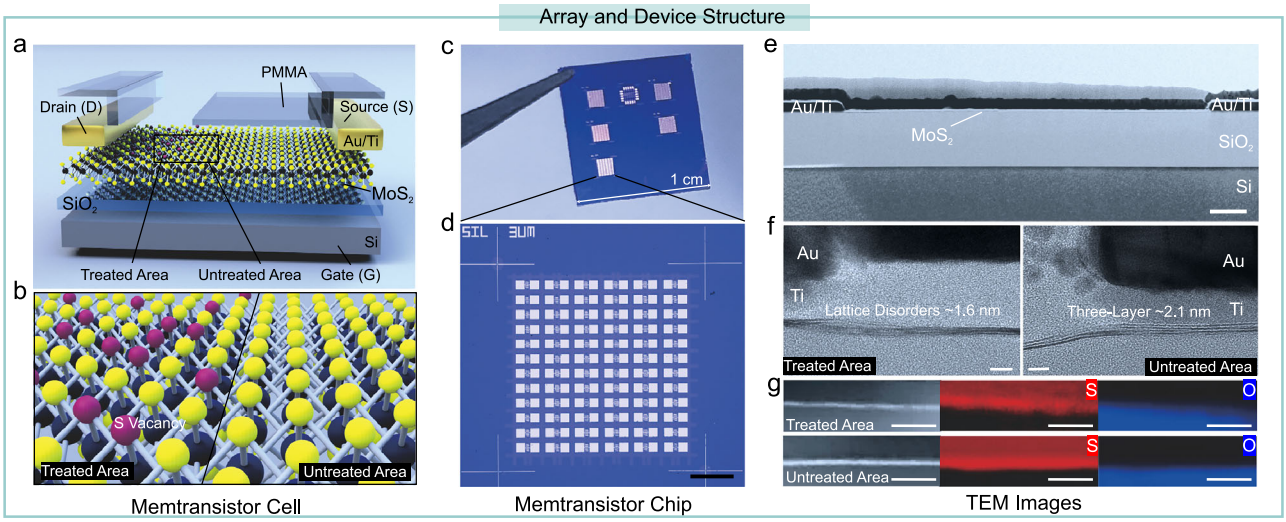

Fig. 1 | Structure of MoS_2 memtransistor arrays. a Schematic of the MoS_2 memtransistor structure, highlighting the selectively treated and untreated areas for Schottky barrier modulation. **b** Schematic of the atomic model of the treated MoS_2. The introduction of controlled oxidation in the treated area leads to localized sulfur vacancy redistribution. **c** Optical images of the fabricated memtransistor chip, demonstrating large-scale integration with 12 × 6 arrays. **d** A 12 × 6 array with the channel length of 3 μm. Scale bar, 300 μm. **e** The cross-sectional transmission electron microscopy (TEM) image of a memtransistor cell. Scale bar, 200 nm. **f** The high-resolution TEM images of the memtransistor cell, revealing the structural characteristics of the treated and untreated regions, confirming the presence of lattice disorder (~1.6 nm) and oxygen incorporation in the modified Schottky interface. Scale bar, 4.8 nm for the image of the treated area and 4.2 nm for the image of the untreated area. **g** Corresponding elemental distributions of a memtransistor cell, which further verifies the spatially controlled oxidation effects, enabling precise Schottky barrier engineering. Scale bar, 20 nm.

tune the Schottky barrier height (Φ_{SB}). According to the Schottky barrier-FET model, the I_{DS}-V_{DS} curves can be expressed as[7,33]:

$$I_{DS} = D\exp\left[\frac{e(V_G - V_{th})}{c_r kT}\right]\left[1-\exp\left(\frac{-eV_{DS}}{kT}\right)\right]\exp\left[\frac{-e}{kT}\left(\Phi_{SB} - \sqrt{\frac{eV_{DS}}{4\pi\varepsilon_i d}}\right)\right] \quad (1)$$

Where D, e and k represent fitting parameter, the charge of the electron and the Boltzmann constant, respectively. The first exponential term represents the gate voltage (V_G) modulation, where I_{DS} increases with V_G, demonstrating the memtransistor's gate tunability. The second exponential term accounts for the asymmetry in I_{DS} under positive and negative bias. The last exponential term describes the contribution of Φ_{SB}. Random vacancies with high Φ_{SB} causes the memtransistor keep in high resistive state (HRS). When a bias is applied, vacancies migrate along grain boundaries, reducing Φ_{SB} and transitioning the device to a low-resistance state (LRS). As shown in Fig. 3a, b, we increase Φ_{SB} at the electrodes/channel interface through MoS_2 oxidation. Initially, random vacancies induce a large Φ_{SB}, maintaining the device in HRS. Upon applying a programming bias, vacancy migration lowers Φ_{SB}, enabling the LRS state.

To minimize uncontrolled vacancies, high-quality MoS_2 growth is essential. Figure 3c, d presents high-resolution scanning tunneling microscopy (STM) images of MoS_2 grown on a highly oriented pyrolytic graphite (HOPG) substrate, revealing a moiré pattern with an atomic spacing of 0.326 nm—consistent with pristine MoS_2 and indicating minimal vacancies. The scanning tunneling spectroscopy (STS) results in Fig. 3e confirm a bandgap of ~1.8 eV. Additionally, the grown MoS_2 characterized by AFM and Raman mapping (Supplementary Fig. 6), as well as the FET arrays fabricated from grown MoS_2 (Fig. 3f) exhibit high uniformity, further confirming the material's quality and low vacancy concentration. Spectroscopic analysis further validates that the controlled sulfur vacancy can be produced by plasma treatment. Raman spectra in Fig. 3g show that the intensity of the two characteristic peaks (E^1_{2g}, A_{1g}) of MoS_2 weakens after oxygen plasma treatment, while the intensity of the Si substrate characteristic peak at 520 cm^{-1} remains unchanged. This indicates that both the in-plane and out-of-plane vibrational modes between Mo and S atoms are weakened, suggesting the formation of S vacancies. Additionally, in Supplementary Fig. 2b, c, different vacancy concentrations in MoS_2 can be obtained by varying the treatment duration. The gradual decrease in characteristic peak intensity with increasing treatment time further confirms that more vacancies are generated as the treatment time increases. The X-ray photoelectron spectroscopy (XPS) spectra also provide evidence for the presence of S vacancies. In Fig. 3h, the Mo 3d core-level XPS spectra exhibit a pronounced Mo–O bond feature and sub-peaks typically associated with sulfur vacancies after treatment, indicating the formation of S vacancies[13,14,34,35]. The S $2p_{1/2}$ and S $2p_{3/2}$ peaks in Fig. 3i show no significant change after treatment, suggesting that the presence of S vacancies does not significantly affect the overall S 2p peak profile. The results of ultraviolet photoelectron spectroscopy (UPS) data indicate that a Schottky barrier height of 0.56 eV is formed between the oxidized MoS_2 and the pristine MoS_2, leading to a HRS in the device (Fig. 3j). These spectroscopic results provide experimental support for our design mechanism. Combined with the TEM results in Fig. 1, this further demonstrates that a controllable vacancy distribution and concentration can be achieved in high-quality MoS_2 through oxygen plasma treatment, enabling the fabrication of memtransistors with stable switching behavior.

Based on the memtransistor cell design and vacancy regulation method, the fabrication and device performance of vacancy-tunable memtransistor arrays are presented in Figs. 4 and 5. Figure 4a and Supplementary Fig. 7 illustrate the step-by-step fabrication process. High-quality MoS_2 grown on a SiO_2/Si substrate is selected as the base material. First, electron-beam lithography (EBL) and electron-beam evaporation (EBE) are used to design and deposit electrodes and markers. Then, marker alignment is utilized to define the channel. Finally, controlled oxidation areas are designed using marker alignment, and the vacancy concentration and area in the memtransistor array are adjusted by controlling the oxygen plasma treatment time. The detailed fabrication process can be found in the Methods section. Figure 4b presents an optical image of the memtransistor array before treatment, where the cells adopt an interdigitated electrode design (Fig. 4c) to minimize the impact of uncontrollable vacancies while

https://doi.org/10.1038/s41467-025-64579-5

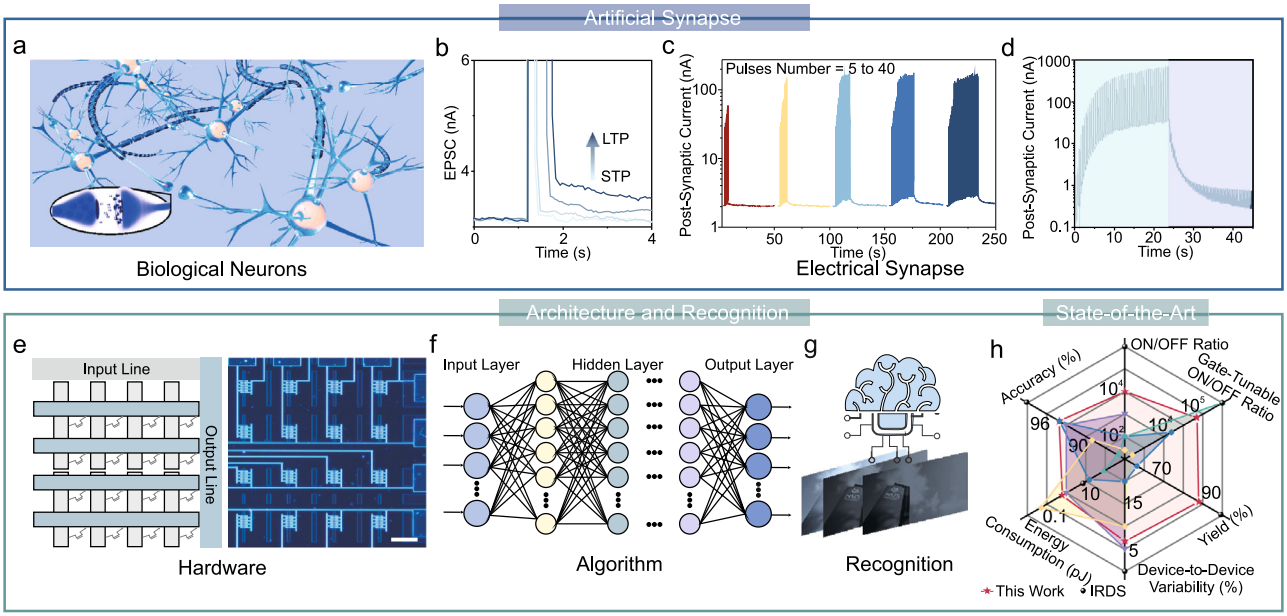

Fig. 2 | Functions of MoS_2 memtransistor arrays. a Schematic of biological neurons. The biological synapse illustration provides a conceptual comparison, where vacancy-driven Schottky barrier modulation mimics synaptic weight tuning. **b** Excitatory postsynaptic current (EPSC) of the memtransistor generated by a single V_D pulse with different duration times. **c** EPSC generated by various numbers of V_D pulses. **d** Long-term plasticity (LTP) characteristics of the memtransistor. The synaptic behavior of the memtransistor is demonstrated by EPSC responses under pulse stimuli, showing both short-term plasticity (STP) and LTP characteristics. Multi-level conductance modulation is achieved through pulse number variation, ensuring stable weight updating, which is critical for artificial neural network (ANN) implementation. **e**–**g** Memtransistor-based neural network system for image recognition. 2D memtransistor array integrated into a hardware ANN framework (**e**) for image recognition tasks. Scale bar, 100 μm. **f**, **g** illustrate the schematic of the image recognition algorithm (**f**) and the corresponding results (**g**) respectively. **h** In comparison with state-of-the art memtransistors based on vacancy migration (blue line)[7,22–25,27], ferroelectric materials (green line)[28], ion-induced phase change (purple line)[29,30], and moiré synapse (yellow line)[31].

enhancing the effect of artificially designed vacancies. The dark-field image (Fig. 4d) reveals that no significant large-area defects exist in the device before oxidation, consistent with the STM results of Fig. 3c, d. Figure 4e, f demonstrates how marker calibration enables precise control of the oxidation pattern. Figure 4e shows that during multiple oxidation processes within the same array to regulate vacancy concentration, the designed oxidation patterns remain accurately aligned, ensuring that increasing treatment time leads to a higher vacancy concentration without altering the oxidation area. Figure 4f illustrates the controlled oxidation areas, where the channel length between electrodes is 3 μm, and the designed oxidation lengths correspond to one-quarter, one-half, three-quarters, and the entire channel length.

Figure 5a presents the representative performance of a memtransistor cell. The ON/OFF ratio of the cell exceeds 10^4, demonstrating excellent switching capability. Figure 5b displays the results over ten switching cycles, revealing that the cycle-to-cycle variation can be as low as 5.4%. The gate-dependent tuning of the memtransistor's performance is shown in Fig. 5c. The empirical cumulative distribution function (ECDF) plot indicates that different gate voltages enable clear differentiation of resistance states, achieving at least seven distinct states. Furthermore, the ON/OFF ratio can be enhanced to 10^5, meeting the stringent requirements for high-performance neuromorphic device applications[36]. The corresponding gate-modulated I_{DS}-V_{DS} characteristics and transfer curves are shown in Supplementary Fig. 8, further demonstrating the gate-tunable behavior of the memtransistor. In addition, the clockwise hysteresis observed in the transfer curves also indicates the presence of vacancy-related traps in the device[7].

Figure 5d–f, along with Supplementary Figs. 9 and 10, illustrate the tunability of vacancy-controlled memtransistor arrays in ML and FL MoS_2 devices. The results indicate that, regardless of the layer thickness, the devices with the smallest oxidation area exhibit the highest ON/OFF ratio. As the oxidation area increases, the ON/OFF ratio decreases, primarily due to the increased charge trapping effect induced by vacancies[37]. Additionally, due to the competing effects of charge trapping and vacancy migration, the performance differences between ML and FL memtransistors become more pronounced at varying vacancy concentrations. ML MoS_2 is more sensitive to vacancy concentration changes. As the vacancy concentration increases, the charge trapping effect in ML MoS_2 memtransistor becomes more significant, leading to a rapid decline in the ON/OFF ratio. The clear variation of the ON/OFF ratio with vacancy concentration also provides a potential application pathway for using memtransistors in quality assessment and monitoring of TMDC materials.

Retention and endurance characteristics of ML and FL MoS_2 memtransistors are shown in Supplementary Figs. 11 and 12. FL MoS_2 memtransistors exhibit stable performance, with over 100 switching cycles, retention times exceeding 10^3 s and endurance under nearly 10,000 LTP/LTD pulses. In contrast, ML MoS_2 devices exhibit greater susceptibility to oxidative degradation, primarily due to the adsorption of oxygen and water molecules at vacancy sites[14]. Consequently, its endurance under electric field stress and retention in natural environments are both compromised[38–40]. To address this issue, future improvements will focus on strategies to prevent environmental exposure of vacancy sites, such as introducing dielectric encapsulation layers and fabricating top-gate electrode structures to enhance device stability and reliability.

Statistical performance of the memtransistor array

To further demonstrate the uniformity of the fabrication method, a statistical analysis of the memtransistor array was conducted. Figure 6a presents the normalized distribution of the ON and OFF states for a 12 × 6 array. The results show a clear distinction between the ON and OFF states, with the ON state exhibiting better uniformity compared to the OFF state. This is primarily due to the measurement limit of our testing instrument at extremely low

https://doi.org/10.1038/s41467-025-64579-5

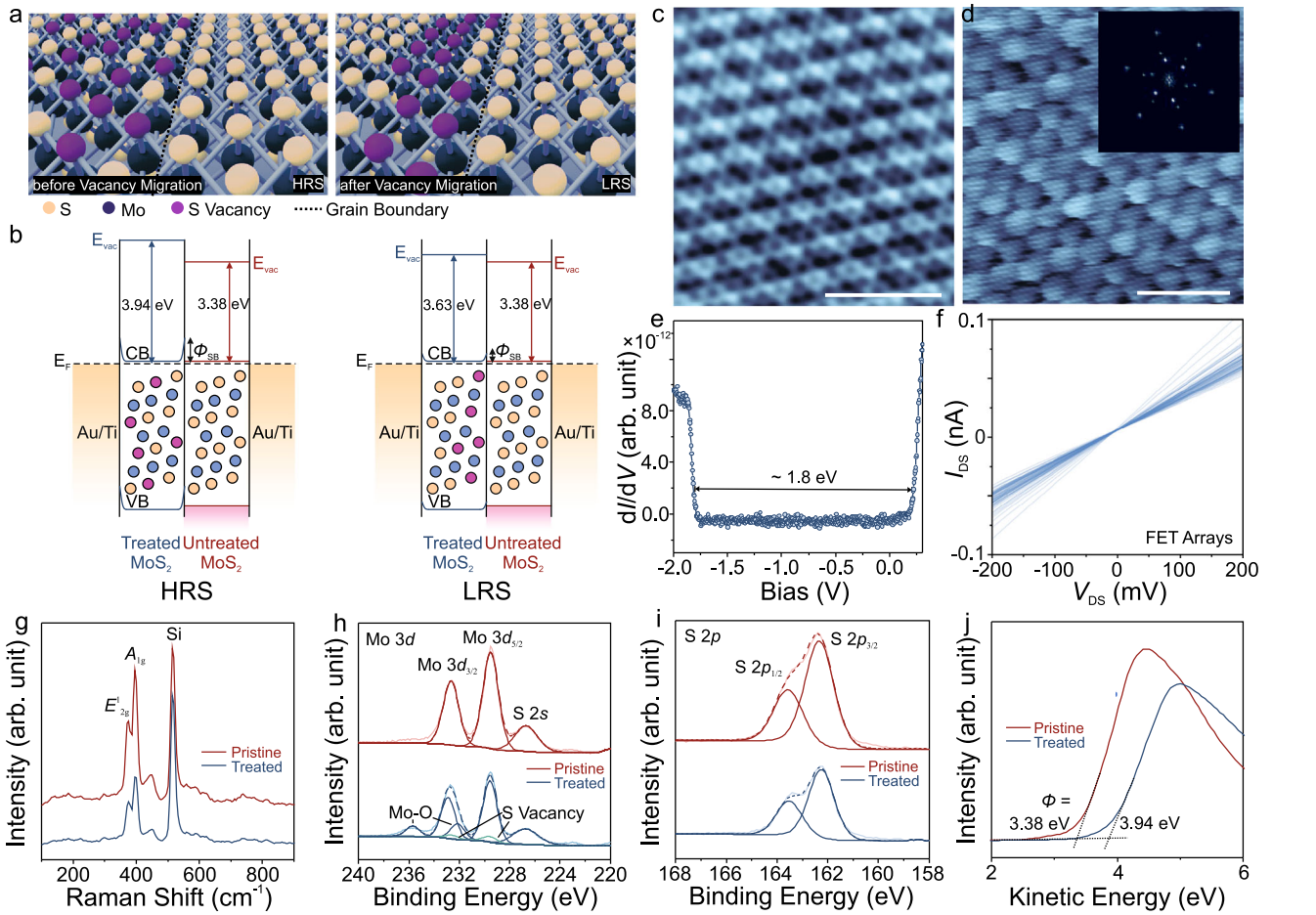

Fig. 3 | Schottky barrier modulation mechanism and characteristics in MoS_2 memtransistors. a Atomic schematic of sulfur vacancy before and after migration, leading to a switching from the high resistance state (HRS) to the low resistance state (LRS). E_{vac} (vacuum level energy), E_F (Fermi level), Φ_{SB} (Schottky barrier height), CB (conduction band), and VB (valence band). **b** The energy band diagrams for treated and untreated MoS_2 regions before and after vacancy migration, illustrating the Schottky barrier modulation. **c**, **d** High-resolution scanning tunneling microscopy (STM) images of high-quality monolayer MoS_2 on the highly oriented pyrolytic graphite (HOPG) substrate. **c** shows the moiré pattern formed by MoS_2/HOPG. Scale bar, 2.5 nm. **d** reveals a lattice spacing of 0.326 nm, consistent with MoS_2. Scale bar, 1 nm. The inset is a diffraction pattern from STM. **e** The scanning tunneling spectroscopy (STS) of the MoS_2/HOPG substrate. The bandgap of monolayer MoS_2 is about 1.8 eV. **f** Electrical characterization of field-effect transistor (FET) arrays based on monolayer MoS_2. **g** Raman spectra comparing pristine and treated MoS_2. The intensity change of two peaks indicates sulfur vacancy induced structural modifications. **h** X-ray photoelectron spectroscopy (XPS) spectra of the Mo 3 *d* core levels confirm the presence of Mo–O bonding in the treated MoS_2 region, suggesting controlled oxidation at vacancy sites. **i** XPS spectra of the S 2*p* core levels. The intensity ratio of the S $2p_{1/2}$ to S $2p_{3/2}$ peaks decreases after treatment, further verifying the presence of sulfur vacancy. **j** Ultraviolet photoelectron spectroscopy (UPS) analysis shows a shift in the work function, correlating with the Schottky barrier height modification from 3.38 eV to 3.94 eV. These results collectively demonstrate that vacancy engineering effectively tunes the Schottky barrier, enabling precise modulation of memtransistor electrical characteristics.

currents in the OFF state. Since the array cells are independent, no leakage or sneak currents were observed when analyzing the device yield. The primary influencing factors include the relatively small ON/OFF ratio (<10) and the narrow memory window ($\Delta V_{TH} < 1$ V) under a constant current of 1 nA (Fig. 6b)[41]. Based on this analysis, the device yield is approximately 89%.

Figure 6c, d uses statistical methods to illustrate that the ON and OFF states of the array can be clearly distinguished. In Fig. 6c, the ON and OFF states follow Gaussian distributions, and their current values are well-separated. The ECDF plot (Fig. 6d) further confirms the clear differentiation between the ON and OFF states. Additionally, Fig. 6e examines the variation in the set voltage at 1 nA, revealing that the device-to-device variation across the array is less than 20%. The high device yield and minimal device-to-device variation provide a solid foundation for hardware-efficient ANNs.

Scalable and high-density memtransistor arrays

As mentioned, the size of each cell in the one memristor structure, using the λ-based design rules ($F = 4\lambda$ = the minimum half-pitch), is $4F^2$, while the resulting 1T1M structure will be larger than this, reaching $7F^2$ or more[27,42]. However, the cell size of the memtransistor can be reduced to a size close to or smaller than that of the 1M structure by scaling the channel length and width, as well as by using shared electrodes. As shown in Fig. 7a, the size of a single memristor cell is already $4F^2$. To achieve effective regulation, a transistor needs to be added to form the 1T1M structure, which increases the size and reduces the array density. For our memtransistor arrays with a 3 μm channel length, the cell size is $6F^2$ when sharing source and drain electrodes. Since the channel length of 2D transistors can be scaled down to the nanoscale, we can reduce the cell size by scaling the channel length. When the channel length is reduced to 500 nm, the cell size approaches $4.65F^2$, which is close to the 1 M cell size. If the channel width is halved at this point, the cell size can theoretically be further reduced to $2.3F^2$. From the relationship between the channel length and the cell size of the memtransistor shown in Fig. 7b, when the channel length reaches the submicron level, the cell size can approach that of the 1 M cell. If the λ value is fixed, further reduction in the cell size can be achieved by adjusting the electrode and channel width.

https://doi.org/10.1038/s41467-025-64579-5

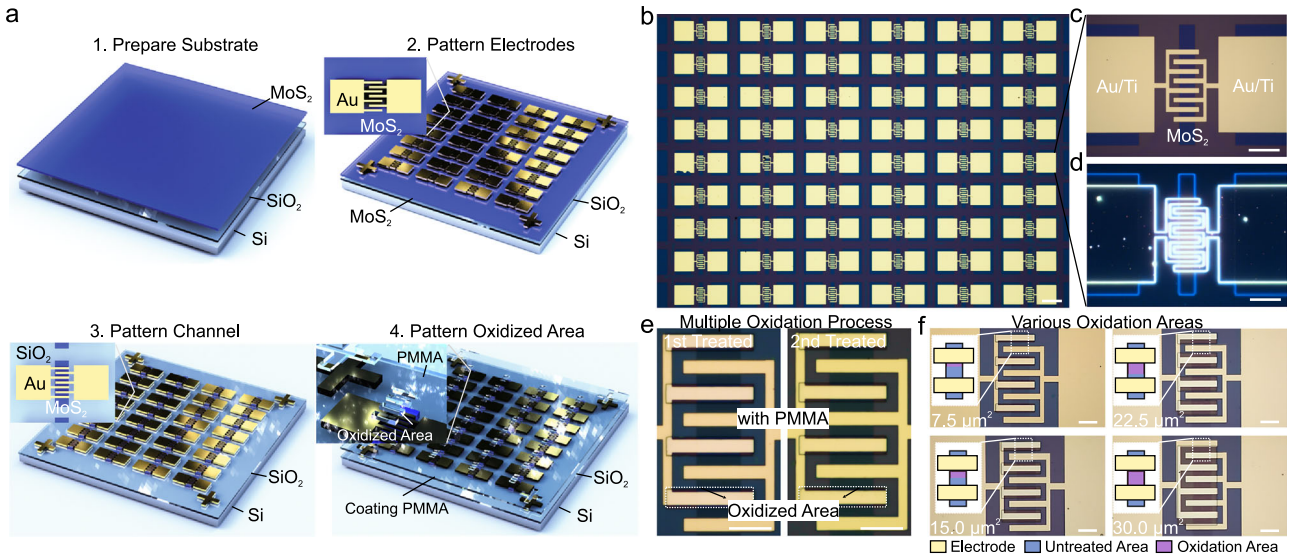

Fig. 4 | The fabrication process of the MoS_2 memtransistor arrays with controlled Schottky barrier modulation. a The step-by-step fabrication process of the memtransistor arrays. **b** Optical images of a MoS_2 memtransistor array before the oxidation treatment. Scale bar, 60 μm. **c** The bright-field image of memtransistor cell. Scale bar, 10 μm. **d** The dark-field microscope image of the memtransistor cell. Scale bar, 10 μm. No defect can be observed in the dark-field image showing the high-quality of the pristine MoS_2. **e** Optical image comparison of two identical oxidation patterns designed on the same memtransistor cell. The oxidation locations remain unchanged, demonstrating the high precision and controllability of the oxidation process. Scale bar, 10 μm. **f** A series of optical images showing different oxidation area sizes. The corresponding schematic illustrations highlight the oxidation regions in red, with oxidation areas ranging from 7.5 to 30 $μm^2$. Scale bar, 10 μm.

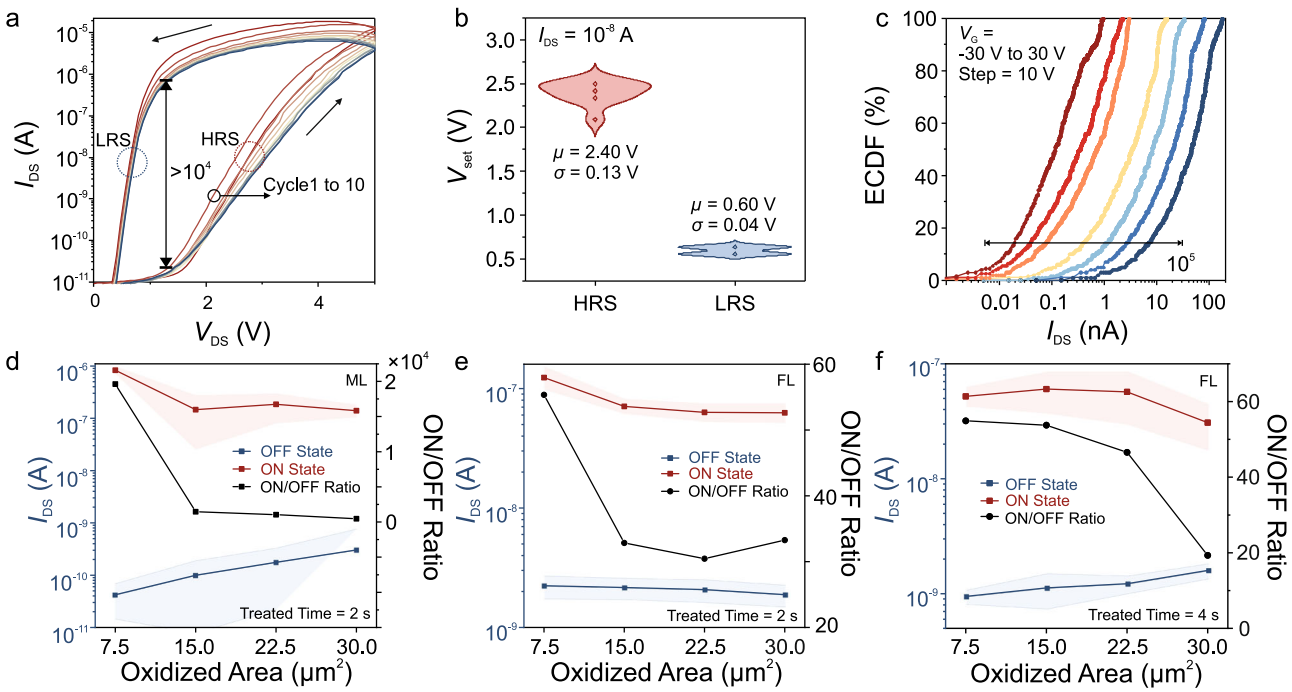

Fig. 5 | The device characterization of the MoS_2 memtransistor arrays with controlled Schottky barrier modulation. a 10 cycles of the I_{DS}-V_{DS} characteristics of a monolayer MoS_2 memtransistor. The oxidation area is 7.5 $μm^2$. **b** A statistical distribution of the set voltage of 10^{-8} A for the HRS and LRS. μ (mean) and σ (standard deviation). **c** The empirical cumulative distribution function (ECDF) of the measured current under different gate voltages. The gate voltages are ranging from −30 V to 30 V. **d**–**f** The influence of the oxidized area on ON/OFF ratio. The memtransistors are based on monolayer (ML) MoS_2 with an oxidation time of 2 s (**d**), and few-layer (FL) MoS_2 with oxidation time of 2 s (**e**) and 4 s (**f**), respectively.

Thus, we further fabricate a scaled array, scaling both the channel length and electrode width to 1 μm and 500 nm, and analyze the changes in device performance during this process. Supplementary Fig. 1 shows that the cell size significantly reduces when the channel length and electrode width are reduced. Figure 7c presents the array structure with a 500 nm channel length. The bright-field (Fig. 7d) and dark-field (Fig. 7e) microscope images show the case where the oxidation region is designed. It can be observed that the oxidized area can still be well designed and fabricated. This demonstrates that our array fabrication method can be applied to scaled arrays, and we believe this method can also be adapted to advanced sub-100 nm technologies to achieve smaller channel lengths and cell size[19–21]. Figure 7f and

https://doi.org/10.1038/s41467-025-64579-5

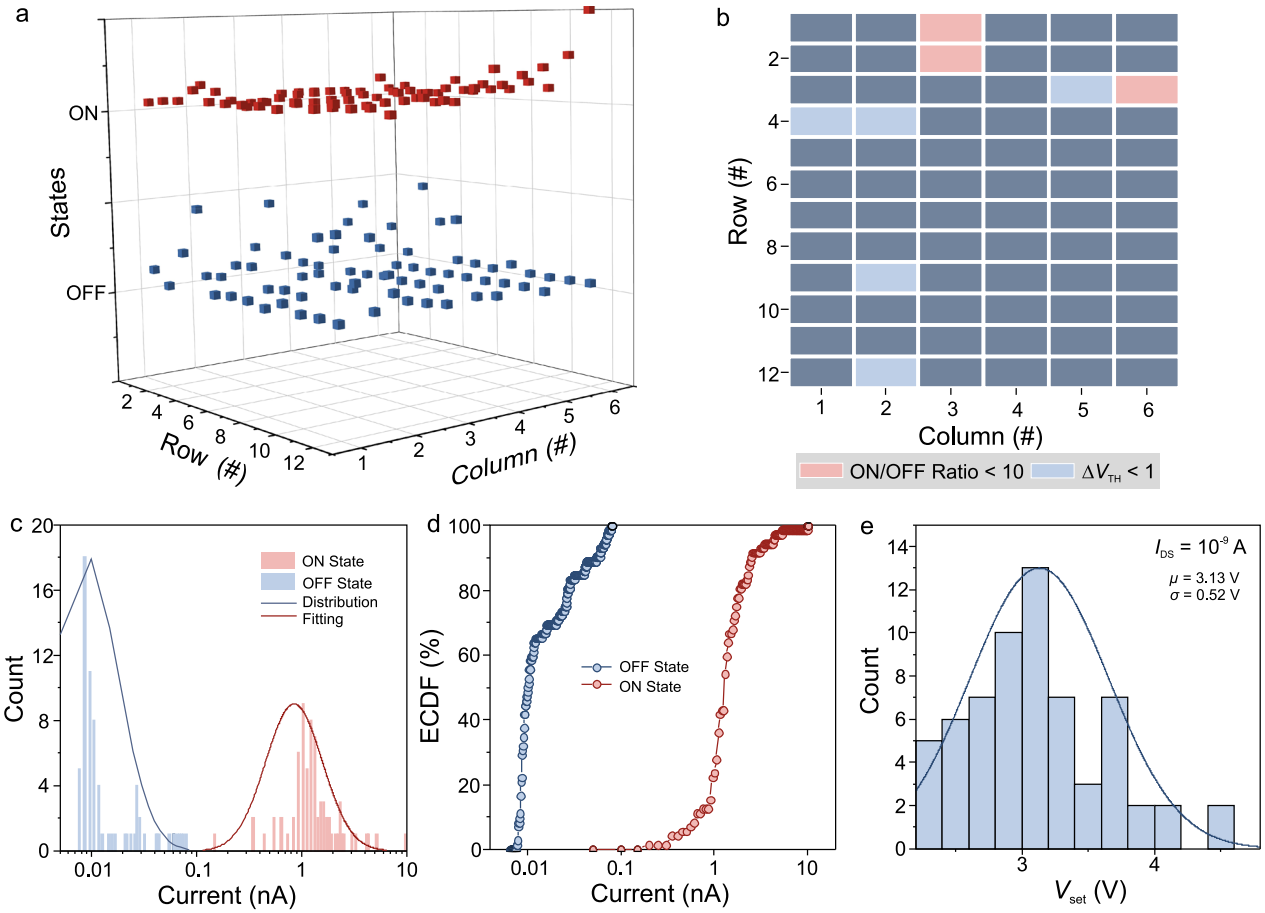

Fig. 6 | A statistical device characterization of the MoS_2 memtransistor array. **a** Three-dimensional map of normalized ON/OFF states of the 6 × 12 memtransistor array. **b** Distribution on the array of each categorized failed device. **c** Distribution of ON/OFF states. The data are fitted with a Gaussian distribution. **d** Empirical cumulative distribution function (ECDF) as a function of the ON/OFF states. **e** Histogram of the switch voltage at a set voltage of 10^{-9} A of the 64 memtransistor cells. The blue line is fitted with a Gaussian distribution.

Supplementary Fig. 13a show the switching curves corresponding to the 500 nm channel length, indicating that the set voltage can be less than 1 V. Based on the 2D grain-boundary compact model that accounts for voltage-dependent defect migration, the defect states induced by grain boundaries are described using an exponential band-tail distribution[27,43,44]. Two key parameters in this model are the total defect density N_{t0}, typically ranging from 10^{12} to 10^{13} cm^{-1}, and the band-tail width parameter k_BT_0, which is set to $5k_BT_{room}$, consistent with previous studies[45]. The migration barrier, a critical dynamic parameter that governs the switching behavior, lies between 0.6 and 2.5 eV. When a medium barrier of ~1.5 eV is considered, the required set voltage is estimated to be approximately 0.8 V for a grain size of 1 μm. Based on this scaling, a 1 V set voltage is sufficient to induce defect migration in a device with a 500 nm channel length and a grain size of 125 nm, thereby increasing the device density while also reducing power consumption. Figure 7g–i displays the statistical results of the array, where the switching states can be distinguished in the scaled case. The array statistical results with a 1 μm channel length further demonstrate the uniformity of this array fabrication method (Supplementary Fig. 14). Supplementary Fig. 13 also shows the synaptic characteristics of the memtransistor with a 500 nm channel length. Under a pulse voltage of less than 1 V, the device still exhibits excellent short-term and long-term synaptic characteristics, effectively reducing the device's power consumption.

When the effect of gate modulation is not considered ($V_G = 0$ V) and only the influence of Schottky emission is taken into consideration, the Schottky barrier model can be rewritten as the following equation:

$$\ln\left(\frac{I_{DS}}{T^2}\right) = \ln(A^*) - \frac{e\phi_{SB}}{kT} - \frac{e}{kT}\sqrt{\frac{eV_{DS}}{4\pi\varepsilon_i d}} \quad (2)$$

Where A^* is the Richardson constant. From this equation, the intercept can be used to estimate the Φ_{SB} corresponding to HRS and LRS of the memtransistor. Figure 7j illustrates the variation of Φ_{SB} during channel length scaling, which is not only crucial for achieving low-power and high-density integration in practical applications, but also offers a statistically robust platform to investigate the evolution of device working mechanisms with respect to channel dimensions. It can be observed that the ratio of Φ_{SB} in HRS and LRS remains unchanged as the channel length decreases. This indicates that the channel length of the memtransistor can theoretically be further reduced, increasing array density while maintaining a high ON/OFF ratio with lower energy consumption. The role of vacancy-induced charge trapping is analyzed by the space-charge-limited current (SCLC) model[37,46], which reflects the influence of localized trap states, as illustrated in Supplementary Fig. 15. The results reveal that both ML and FL devices exhibit distinct segments in their I_{DS}-V_{DS} curves that follow well-defined power-law behavior (i.e., $I \propto V^m$), with clear transition points (kinks). At voltages below 1.2 V, the exponent m is approximately 2, consistent with the classic SCLC regime where current scales quadratically with voltage, indicating that charge trapping dominates under low bias. At higher voltages, m exceeds 2, suggesting a transition into the trap-filled limit (TFL) regime, where

https://doi.org/10.1038/s41467-025-64579-5

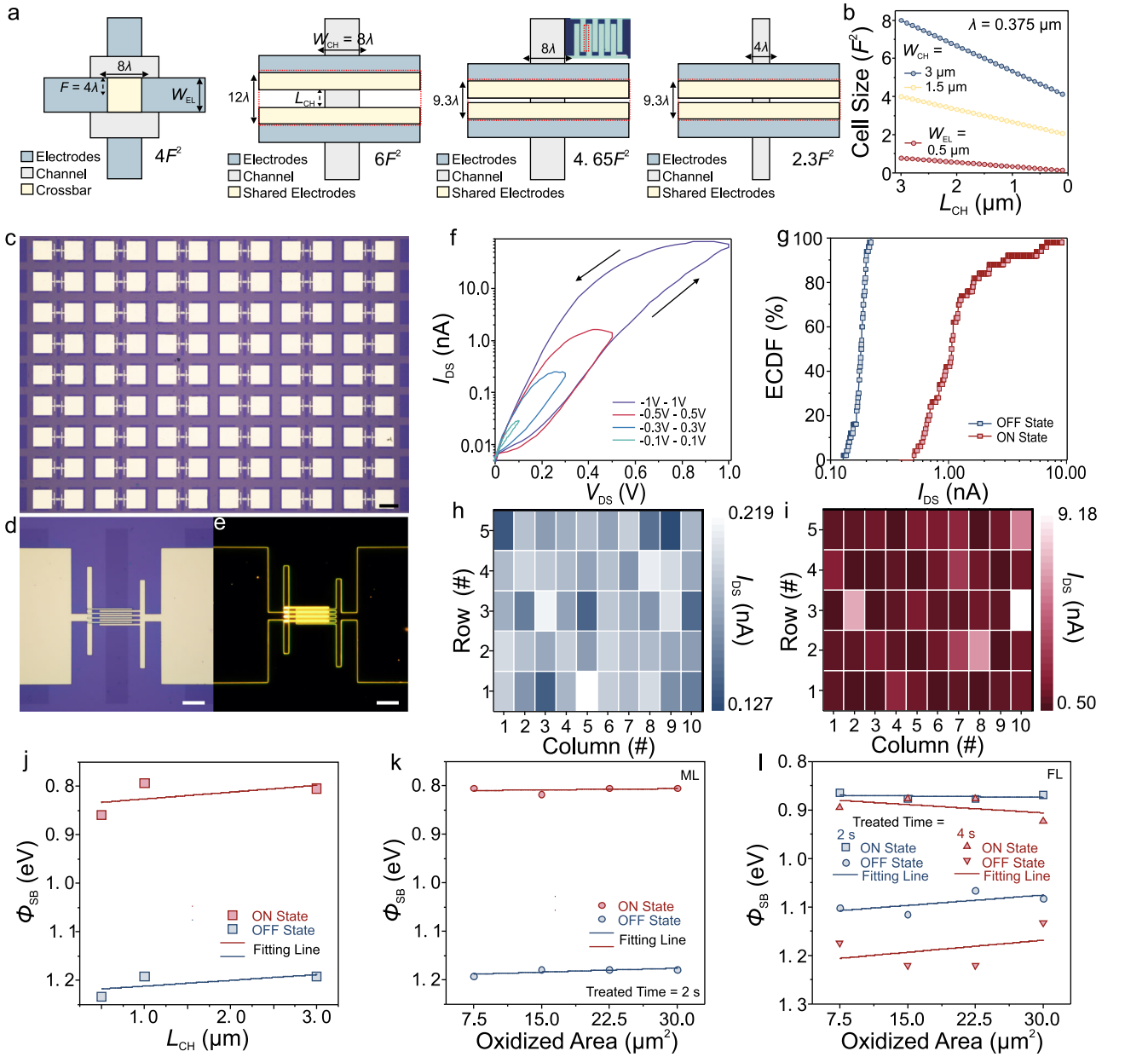

Fig. 7 | Schottky barrier variation with device scaling. a Schematic illustration of the cell sizes in crossbar and memtransistor structures. The crossbar configuration has a size of $4F^2$, while the memtransistor cell size can be reduced to $2.3F^2$ by sharing source/drain electrodes and minimizing the channel length (L_{CH}) and width (W_{CH}). The inset shows an optical image of a device with a channel length of 500 nm and electrode width (W_{EL}) of 3 μm. Scale bar, 6 μm. $F = 4\lambda$ = the minimum half-pitch. **b** Relationship between channel length and device size. The blue, yellow, and red lines correspond to channel widths of 3 μm, 1.5 μm, and 0.5 μm, respectively. **c** Optical image of an array with a channel length and electrode width of 500 nm. Scale bar, 60 μm. Bright-field (**d**) and dark-field (**e**) of a memtransistor cell with a designed oxidation region. Scale bar, 10 μm. **f** I_{DS}-V_{DS} characteristics of a monolayer MoS_2 memtransistor with a 500 nm channel length under different setting voltages. **g** Empirical cumulative distribution function (ECDF) plot of the memtransistor array with a 500 nm monolayer MoS_2 channel. Mapping of OFF-state (**h**) and ON-state (**i**) distribution in the memtransistor array. **j** Relationship between Schottky barrier height in ON/OFF states and channel length. Red and blue lines represent the corresponding fitted curves, respectively. **k** Correlation between Schottky barrier height and oxidized area in monolayer MoS_2 under different switching states. Red and blue lines represent the corresponding fitted curves, respectively. **l** Correlation between Schottky barrier height and oxidized area in few-layer MoS_2 under different switching states. The blue and red lines correspond to oxidation treatment times of 2 s and 4 s, respectively. The red and blue lines above correspond to the ON-state fitted curves, and those below correspond to the OFF-state fitted curves.

the trap states become fully occupied and the influence of vacancy migration becomes increasingly significant.

Figure 7k presents the Φ_{SB} distribution of ML MoS_2 memtransistors under different oxidation areas. The results show that despite variations in the oxidation area, the ratio of Φ_{SB} remains unchanged. This confirms that the ON/OFF ratio changes observed in Fig. 5d for ML MoS_2 memtransistors primarily originate from charge trapping effects, where a higher vacancy density leads to increased charge trapping, ultimately reducing the ON/OFF ratio[37]. For FL MoS_2 memtransistors, vacancy migration plays a more significant role during short oxidation treatments. Figure 7l depicts the relationship between Φ_{SB} and oxidation area under two different treatment durations. The results indicate that although increased oxidation time leads to more vacancies and enhances charge trapping, the Φ_{SB} ratio significantly increases. This trend aligns with the changes in the ON/OFF ratio observed in Fig. 5e, f. This suggests that in FL MoS_2 memtransistors, the Φ_{SB}

https://doi.org/10.1038/s41467-025-64579-5

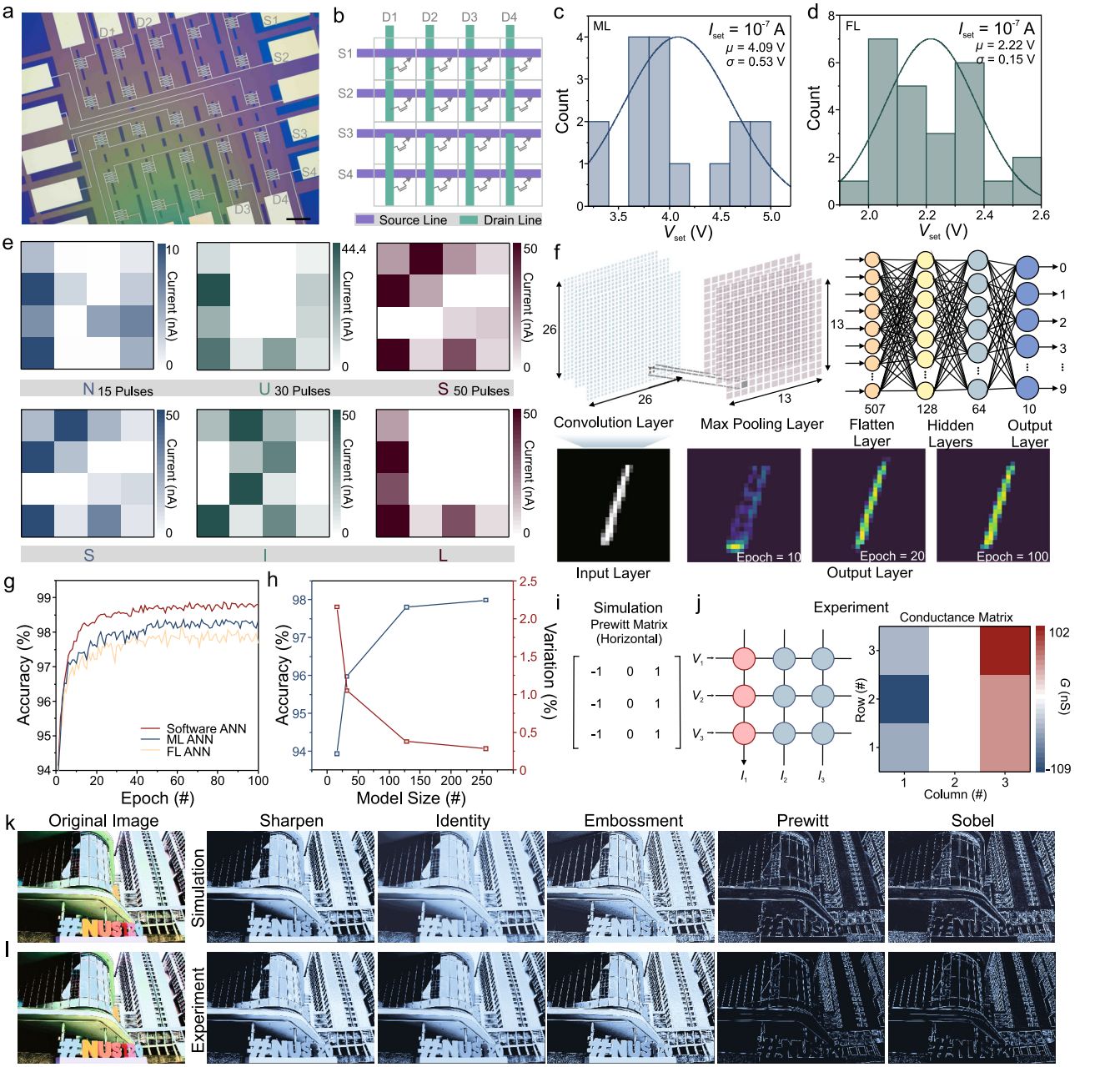

Fig. 8 | Hardware-efficient artificial neural network system. a Optical image of the fabricated 5 × 5 memtransistor array. Scale bar, 100 μm. **b** Schematic diagram of a 4 × 4 subarray with the same structure. Histogram statistics of the switch voltage at a set voltage of 10^{-7} A for single-layer (**c**) and few-layer (**d**) arrays. Solid lines are fitted to the data with a Gaussian distribution. **e** Mapping of the 4 × 4 subarray under different numbers of potentiation and depression pulses. "N" represents the result after 15 potentiation pulses; "U" represents the result after 30 potentiation pulses; the upper "S" represents the result after 50 potentiation pulses; "SIL" represents the reversed formation after applying 50 depression pulses to non-forming letter positions in an array fully written with 50 potentiation pulses. **f** Schematic representation of the neural network recognizing MNIST database patterns. **g** Recognition accuracy of a monolayer and few-layer neural network system based on the MNIST dataset, matching the software methods. **h** Variations in array uniformity (red line) and recognition accuracy (blue line) for different model sizes. **i**, **j** Schematic of a 3 × 3 subarray used for Prewitt convolution-based image processing, employing encoding formats for horizontal matrix structures. **i** is the Prewitt matrix. **j** is the operation and the obtained conductance mapping. Comparison of various convolutional image processing results between simulation (**k**) and experimental (**l**) implementations. The simulation and experimental results are based on the convolution matrix and conductance matrix, respectively.

variation is more dominant under low vacancy conditions. Further increasing the oxidation time may improve the ON/OFF ratio of FL MoS_2 memtransistors to match that of ML MoS_2 devices. Based on these results, we conclude that in vacancy-migration-based memtransistors, vacancy-induced charge trapping limits the ON/OFF ratio variation. To maximize the Schottky barrier modulation while minimizing charge trapping effects, it is crucial to maintain a controlled yet minimal vacancy distribution range.

Image processing by the memtransistor-based ANN system

Using the same array fabrication method, we constructed a 5 × 5 memtransistor array for neuromorphic hardware applications (Fig. 8a and Supplementary Fig. 16). A structurally symmetric 4 × 4 subarray is selected to demonstrate hardware programming capabilities (Fig. 8b). As shown in Fig. 8c, d, this array exhibits excellent device-to-device uniformity in both ML and FL configurations, with a minimal variation rate below 6.8% and a 100% yield. Figure 8e and Supplementary Fig. 17

present the device performance under multiple potentiation and depression pulses in the 4 × 4 array. The results indicate that both the neuromorphic update signal (NUS), programmed and read after different numbers of potentiation pulses, and the signal-inhibiting learning (SIL), programmed and read after potentiation pulses following depression, are accurately realized. This confirms the good control over sneak current in the array, ensuring that each cell operates independently.

The fabricated array is first applied to a small-size image recognition based on Modified National Institute of Standards and Technology (MNIST) dataset. A training dataset of 60000 handwritten digit images is sent to the ANN for training and then the recognition accuracy is obtained by performing validation process using another 10000 hand written digit images. As shown in Supplementary Fig. 18, three devices exhibit distinct characteristics in terms of nonlinearity factors and asymmetric ratios[47]. For Device 1, the nonlinearity factor of LTP and LTD is 0.48 and -0.21, respectively, indicating a relatively high degree of symmetry. In contrast, Devices 2 and 3 show higher LTP linearity, with nonlinearity factors of -1.0 and -0.95, respectively. However, the LTD processes of these two devices exhibit pronounced nonlinearity and asymmetry. It can be observed that the device with higher symmetry (Device 1) achieves better accuracy, whereas Devices 2 and 3, which exhibit lower symmetry, result in relatively poorer recognition performance. To address the issue of non-ideal synaptic behavior, a gradually increasing pulse voltage scheme was employed to mitigate the nonlinearity caused by the rapid conductance drop during the initial LTD pulses[48]. In parallel, algorithmic optimization was implemented to improve the recognition accuracy of the neural network under such non-ideal synaptic conditions (Methods and Supplementary Fig. 19). The ANN construction and the evolution of image with epoch numbers during training are shown in Fig. 8f. The MNIST classification accuracy exceeds 98% (Fig. 8g and Supplementary Fig. 20), which is comparable with purely software results. Figure 8h and Supplementary Figs. 21 and 22 illustrate the change in average accuracy and uniformity across different model sizes. It is evident that as the model size increases, the overall accuracy improves while the variation rate decreases.

Having achieved a uniform array, we further extend its application to convolutional image processing. Various convolution kernels are used to extract features from target images: Prewitt and Sobel kernels are mainly used for edge detection, the Embossment kernel adds a 3D-like effect, the Identity kernel is used for testing or skipping processing, and the Sharpen kernel enhances image details[11,49]. The target image was used as input for various convolutional kernel operations. Then the image grey scale intensity is divided into 3 × 3 sub-images. The sub-images are mapped into voltages and applied to the rows of the array, constructing various target convolutional kernels (Fig. 8i). The dot product of input voltages and conductance values could be naturally achieved by Ohm's Law and Kirchhoff's current law. The detailed multiple state information and hardware kernel configurations are shown in Supplementary Table 1 and Supplementary Fig. 23, respectively. The conductance (G) matrix mapping of Prewitt horizontal kernel is shown in Fig. 8j and other G matrix mappings are shown in Supplementary Fig. 23, respectively. Figure 8k, l and Supplementary Fig. 24 show the close agreement between the hardware-based and software-based convolutional kernel processing results demonstrates the potential of our ANN system for edge detection in image processing applications.

Discussion

We successfully demonstrated scalable MoS_2 memtransistor arrays with precise Schottky barrier modulation, achieved through controlled oxidation engineering to regulate vacancy distribution and migration dynamics. This approach enables high ON/OFF ratios (up to 10^5), multilevel conductance states, and uniform device characteristics, with device-to-device variation maintained below 6.8% and a fabrication yield of 100%. The memtransistor arrays were further integrated into a hardware-based ANN with synaptic weights encoded as resistive states, achieving over 98% classification accuracy in image recognition tasks.

Beyond immediate performance enhancements, our results reveal that a limited number of vacancies localized near the contacts can effectively modulate the Schottky barrier. In contrast, vacancies situated far from the contacts or present in excessive concentrations predominantly lead to undesirable charge trapping, which degrades device performance. These findings underscore the importance of spatially controlled vacancy engineering—specifically, confining vacancy formation to regions near the contacts—to optimize Schottky barrier modulation. Such a strategy is crucial for advancing single-crystalline TMDC-based devices toward high-density, low-power neuromorphic computing applications. The demonstrated scalability down to 500 nm channel lengths, along with the theoretical feasibility of further miniaturization without compromising switching characteristics, suggests that 2D memtransistor arrays can provide a viable pathway for beyond-CMOS neuromorphic processors. Looking forward, integrating this approach with advanced fabrication techniques, multi-layer stacking, or hybrid CMOS-2D architectures could further enhance device performance and enable large-scale, energy-efficient AI accelerators[50–52]. By addressing key challenges in device uniformity, scalability, and neuromorphic integration, this study establishes a practical and scalable framework for 2D memtransistor-based ANN hardware, bridging the gap between emerging material innovations and real-world AI applications.

Methods

Characterization

Raman measurements were performed using a WITec Alpha 300 R confocal Raman microscope with a 532 nm laser. Cross-section samples were prepared using a dual-beam focused ion beam (FIB) system (FEI Helios Nanolab 450S). TEM characterization and image acquisition were performed using an FEI Titan 80–300 TEM system operating at a 200 kV accelerating voltage. The XPS core-level spectra was measured in a ultrahigh vacuum chamber (base pressure ~ 10^{-10} mbar) and obtained using Al $K\alpha$ radiation ($h\nu$ = 1486.61 eV). UPS spectra were acquired using a He I ultraviolet light source (SPECS UVS 10/35, $h\nu$ = 21.22 eV) with a take-off angle of 45°. A negative bias of -7 V relative to the ground was applied to the sample. For STM and STS characterizations, the ML MoS_2 sample was grown on the HOPG substrate by the chemical vapor deposition (CVD) process. The MoS_2/HOPG sample was annealed in UHV chamber at 150 °C for 3 h before the STM/STS characterization. The tip state was calibrated on the Au(111) surface before STS measurement. All the STM/STS data were acquired at 77 K. STS spectra was acquired using a standard lock-in technique with a bias modulation of 10 mV at 963 Hz.

Single memtransistor fabrication and electrical characterization

FL MoS_2 or $MoTe_2$ flakes were mechanically exfoliated from the high-quality bulk crystals (HQ Graphene) onto polydimethylsiloxane (PDMS) and transferred onto 300 nm SiO_2/Si wafers. Then, the electrode patterns were defined using JEOL electron-beam lithography (JBX-6300FS). Ti/Au (5 nm/50 nm) metals were deposited by electron-beam evaporation followed by the standard lift-off process. The oxidized patterns were also defined using electron-beam lithography and exposed to oxygen plasma in a Vita-Mini RIE system. For the oxygen plasma treatment process, the etch power was set to 10 W and the gas flow rate was 10 sccm with a processing time of 5 s, 10 s and 20 s. After the standard lift-off process, the as-made devices were wire-bonded onto chip carriers and measured in an ambient environment. The electrical measurements were conducted using an Agilent 2192 A source measure unit.

Array fabrication and electrical characterization

ML and FL MoS_2 samples were grown on 300 nm SiO_2/Si substrate through the CVD process. MoO_3 (99.999 %) was used as the molybdenum source, and solid sulfur (99.999 %) was used as the sulfur source. Argon was used as the carrier gas. A dual-zone tube furnace with an 80 mm diameter quartz tube was employed. For ML MoS_2 growth, the temperature of the MoO_3 zone was raised to 650 °C, and the sulfur zone was heated to 180 °C. The growth was carried out under a pressure of 4000 Pa for 10 min on the substrate. For FL MoS_2 growth, the temperature of the MoO_3 zone was raised to 650 °C, and the sulfur zone was heated to 180 °C. The growth was carried out under a pressure of 1000 Pa for 20 min on the substrate. The electrode array patterns were defined using JEOL electron-beam lithography (JBX-6300FS). Ti/Au (5 nm/50 nm) metals were deposited by electron-beam evaporation followed by the standard lift-off process. Then, the channel patterns were defined using JEOL electron-beam lithography (JBX-6300FS) and etched using a Vita-Mini RIE system followed by the standard lift-off process. The oxidized patterns were also defined using electron-beam lithography and exposed to oxygen plasma in a Vita-Mini RIE system. For the oxygen plasma treatment process, the etch power was set to 10 W and the gas flow rate was 10 sccm with a processing time of 2 s/4 s. After the standard lift-off process, the arrays were measured in an ambient environment. The electrical measurements were conducted using a probe station connected to an Agilent 2192 A source measure unit.

ANN system fabrication and electrical measurement set-up for image processing

The 5 × 5 memtransistor array was made by the same array fabrication process for the ANN system. Electrical characterization was first performed on each individual memtransistor cell using both d.c. sweeps and pulsed voltage measurements to obtain the corresponding electrical responses. These collected signals from all array elements were then assembled and input into the image processing and recognition algorithm implemented within the ANN framework.

ANN algorithm

The input data were first preprocessed using max-pooling to reduce computational complexity. A dropout layer was used to minimize the risk of overfitting. A ReLU activation function was employed to regulate the nonlinear and asymmetric conductance updates, enhancing the contribution from LTP while suppressing the effect of LTD. To evaluate the influence of network capacity, models with different sizes (neurons) were tested. The results indicated that larger networks achieved higher recognition accuracy. The Adam optimizer was used to adaptively adjusts the learning rate and enhances convergence stability under noisy and non-ideal synaptic conditions. The optimizer's ability to manage sparse and unstable gradients helps mitigate the impact of non-ideal synaptic behavior, making it suitable for memristor-based neural network training.

Data availability

The Source data underlying the figures of this study are available with the paper. All raw data generated during the current study are available from the corresponding authors upon request. Source data are provided with this paper.

Code availability

Code for the memristor-based neural network is available from the corresponding authors upon request.

References

1. Mehonic, A. & Kenyon, A. J. Brain-inspired computing needs a master plan. *Nature* **604**, 255–260 (2022).
2. Aguirre, F. et al. Hardware implementation of memristor-based artificial neural networks. *Nat. Commun.* **15**, 1974 (2024).
3. Kudithipudi, D. et al. Neuromorphic computing at scale. *Nature* **637**, 801–812 (2025).
4. Pazos, S. et al. Synaptic and neural behaviours in a standard silicon transistor. *Nature* **640**, 69–76 (2025).
5. Jouppi, N. P. et al. In-datacenter performance analysis of a tensor processing unit. *Proc. Int. Symp. Comput. Archit.* **Part F1286**, 1–12 (2017).
6. Yan, X., Qian, J. H., Sangwan, V. K. & Hersam, M. C. Progress and challenges for memtransistors in neuromorphic circuits and systems. *Adv. Mater.* **34**, 1–18 (2022).
7. Sangwan, V. K. et al. Multi-terminal memtransistors from polycrystalline monolayer molybdenum disulfide. *Nature* **554**, 500–504 (2018).
8. Zhou, H., Li, S., Ang, K. W. & Zhang, Y. W. Recent advances in in-memory computing: exploring memristor and memtransistor arrays with 2D materials. *Nano-Micro Lett.* **16**, 1–30 (2024).
9. Song, W. et al. Programming memristor arrays with arbitrarily high precision for analog computing. *Science* **383**, 903–910 (2024).
10. Zhu, K. et al. Hybrid 2D–CMOS microchips for memristive applications. *Nature* **618**, 57–62 (2023).
11. Dang, B. et al. Reconfigurable in-sensor processing based on a multi-phototransistor–one-memristor array. *Nat. Electron.* **7**, 991–1003 (2024).
12. Wang, C. et al. Parallel in-memory wireless computing. *Nat. Electron.* **6**, 381–389 (2023).
13. Li, T. et al. Reconfigurable, non-volatile neuromorphic photovoltaics. *Nat. Nanotechnol.* **18**, 1303–1310 (2023).
14. Zhao, B. et al. Bioinspired gas-receptor synergistic interaction for high-performance two-dimensional neuromorphic devices. *Matter* **8**, 102044 (2025).
15. Wang, M. et al. Robust memristors based on layered two-dimensional materials. *Nat. Electron.* **1**, 130–136 (2018).
16. Jin, T. et al. Ferroelectrics-integrated two-dimensional devices toward next-generation electronics. *ACS Nano* **16**, 13595–13611 (2022).
17. Lemme, M. C., Akinwande, D., Huyghebaert, C. & Stampfer, C. 2D materials for future heterogeneous electronics. *Nat. Commun.* **13**, 2–6 (2022).
18. Hadke, S., Kang, M. A., Sangwan, V. K. & Hersam, M. C. Two-dimensional materials for brain-inspired computing hardware. *Chem. Rev.* **125**, 835–932 (2025).
19. Jiang, Y. et al. A scalable integration process for ultrafast two-dimensional flash memory. *Nat. Electron.* https://doi.org/10.1038/s41928-024-01229-6 (2024).
20. Jiang, J., Xu, L., Qiu, C. & Peng, L. M. Ballistic two-dimensional InSe transistors. *Nature* **616**, 470–475 (2023).
21. Jiang, J. et al. Yttrium-doping-induced metallization of molybdenum disulfide for ohmic contacts in two-dimensional transistors. *Nat. Electron.* **7**, 545–556 (2024).
22. Sangwan, V. K. et al. Gate-tunable memristive phenomena mediated by grain boundaries in single-layer MoS2. *Nat. Nanotechnol.* **10**, 403–406 (2015).
23. Wang, X. et al. Grain-boundary engineering of monolayer MoS2 for energy-efficient lateral synaptic devices. *Adv. Mater.* **33**, e2102435 (2021).
24. Jadwiszczak, J. et al. MoS2 memtransistors fabricated by localized helium ion beam irradiation. *ACS Nano* **13**, 14262–14273 (2019).
25. Yuan, J. et al. Reconfigurable MoS2 memtransistors for continuous learning in spiking neural networks. *Nano Lett.* **21**, 6432–6440 (2021).
26. Lee, H. S. et al. Dual-gated MoS2 memtransistor crossbar array. *Adv. Funct. Mater.* **30**, 1–12 (2020).
27. Feng, X. et al. Self-selective multi-terminal memtransistor crossbar array for in-memory computing. *ACS Nano* **15**, 1764–1774 (2021).

28. Liu, K. et al. An optoelectronic synapse based on α-In2Se3 with controllable temporal dynamics for multimode and multiscale reservoir computing. *Nat. Electron.* **5**, 761–773 (2022).
29. Zhu, X., Li, D., Liang, X. & Lu, W. D. Ionic modulation and ionic coupling effects in MoS 2 devices for neuromorphic computing. *Nat. Mater.* **18**, 141–148 (2019).
30. Rupom, R. H. et al. Ion-induced phase changes in 2D MoTe2 films for neuromorphic synaptic device applications. *ACS Nano* https://doi.org/10.1021/acsnano.4c13915 (2025).
31. Yan, X. et al. Moiré synaptic transistor with room-temperature neuromorphic functionality. *Nature* **624**, 551–556 (2023).
32. Badaroglu, M., Fukuzaki, Y. & Liu, R. The International Roadmap for Devices and Systems (IRDS) 2022—More Moore. 9 (2022).
33. Yang, S. T. et al. Submicron memtransistors made from monocrystalline molybdenum disulfide. *ACS Nano* **18**, 6936–6945 (2024).
34. Chang, W. H. et al. Defect-engineered room temperature negative differential resistance in monolayer MoS2 transistors. *Nanoscale Horiz.* **109**, 1533–1539 (2022).
35. Kim, I. S. et al. Influence of stoichiometry on the optical and electrical properties of chemical vapor deposition derived MoS2. *ACS Nano* **8**, 10551–10558 (2014).
36. Li, M. et al. Imperfection-enabled memristive switching in van der Waals materials. *Nat. Electron.* **6**, 491–505 (2023).
37. Huh, W. et al. Heterosynaptic MoS2 memtransistors emulating biological neuromodulation for energy-efficient neuromorphic electronics. *Adv. Mater.* **35**, 1–9 (2023).
38. Hou, X. et al. Surface-enhanced Raman scattering monitoring of oxidation states in defect-engineered two-dimensional transition metal dichalcogenides. *J. Phys. Chem. Lett.* **11**, 7981–7987 (2020).
39. Gao, J. et al. Aging of transition metal dichalcogenide monolayers. *ACS Nano* **10**, 2628–2635 (2016).
40. Budania, P. et al. Long-term stability of mechanically exfoliated MoS2 flakes. *MRS Commun.* **7**, 813–818 (2017).
41. Migliato Marega, G. et al. A large-scale integrated vector–matrix multiplication processor based on monolayer molybdenum disulfide memories. *Nat. Electron.* **6**, 991–998 (2023).
42. Sivan, M. et al. All WSe2 1T1R resistive RAM cell for future monolithic 3D embedded memory integration. *Nat. Commun.* **10**, 1–12 (2019).
43. Wang, L., Weng, L., Ang, K. W., Thean, A. V. Y. & Liang, G. A surface potential- and physics- based compact model for 2D polycrystalline-MoS2FET with resistive switching behavior in neuromorphic computing. In *Tech. Dig. - Int. Electron Devices Meet. IEDM* 2018-Decem, 24.5.1–24.5.4 (2018).
44. Wang, L., Wang, L., Ang, K. W., Thean, A. V. Y. & Liang, G. A compact model for 2-D poly-MoS2 FETs with resistive switching in postsynaptic simulation. *IEEE Trans. Electron Devices* **66**, 4092–4100 (2019).
45. Qiu, H. et al. Hopping transport through defect-induced localized states in molybdenum disulphide. *Nat. Commun.* **4**, 3–8 (2013).
46. Wang, L. et al. Artificial synapses based on multiterminal memtransistors for neuromorphic application. *Adv. Funct. Mater.* **29**, 1901106 (2019).
47. Jeon, Y. R. et al. Enhanced synaptic memory window and linearity in planar In2Se3 ferroelectric junctions. *Adv. Mater.* **37**, 1–10 (2025).
48. Jin, T. et al. Controlling native oxidation of HfS2for 2D materials based flash memory and artificial synapse. *ACS Appl. Mater. Interfaces* **13**, 10639–10649 (2021).
49. Li, Y. et al. In-memory computing using memristor arrays with ultrathin 2D PdSeOx/PdSe2 heterostructure. *Adv. Mater.* **34**, e2201488 (2022).
50. Kim, K. H. et al. Scalable CMOS back-end-of-line-compatible AlScN/two-dimensional channel ferroelectric field-effect transistors. *Nat. Nanotechnol.* **18**, 1044–1050 (2023).
51. Kang, J. H. et al. Monolithic 3D integration of 2D materials-based electronics towards ultimate edge computing solutions. *Nat. Mater.* **22**, 1470–1477 (2023).
52. Pendurthi, R. et al. Monolithic three-dimensional integration of complementary two-dimensional field-effect transistors. *Nat. Nanotechnol.* **19**, 970–977 (2024).

Acknowledgements

This work was supported by the Natural Science Foundation of China (62274118), Singapore National Research Foundation Investigatorship Program under Grant No. NRF NRFI08-2022-0009, and the SUSTech-NUS Joint Research Program. T.J. acknowledges support from the Science and Technology Commission of Shanghai Municipality, the Shanghai Venus Sailing Program (Grant No. 24YF2712800).

Author contributions

X.H. and W.C. conceived the idea for this work and designed the experiments. X.H., W.Z., S.D. and T.J. performed the experiments. S.D. performed the STM and STS measurements. X.G. performed the XPS and UPS measurements. M.L. performed the TEM and EDS measurements. Y.L. and J.M. assisted with sample preparation and the measurements. X.H. drafted the manuscript. T.J., Y.C., J.Z., J.L. and W.C. revised and refined the manuscript. All authors discussed the results and commented on the paper.

Competing interests

The authors declare no competing interests.

Additional information

Supplementary information The online version contains supplementary material available at https://doi.org/10.1038/s41467-025-64579-5.

Correspondence and requests for materials should be addressed to Xiangyu Hou, Tengyu Jin or Wei Chen.

Peer review information *Nature Communications* thanks Yonghun Kim, Yann-Wen Lan, and the other, anonymous, reviewers for their contribution to the peer review of this work. A peer review file is available.