Flip Chip Interconnects for Quantum Computing Application: A Comparison Between Tin-Silver & Indium Bump

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ABSTRACT

Recent efforts in packaging for qubit devices operating at cryogenic temperatures have focused on flip-chip assembly [1]. The key advantages of the flip-chip assembly technique include the capacity to enable heterogeneous integration and reduce the latency associated with present complex wirings. Flip chips employ solder bumps rather than conventional wire bonding, and to function best in cryogenic applications, solder bumps need to be superconductive, mechanically robust, and thermally stable at extremely low temperatures. [2].

Keywords: superconductivity, cryogenic application, critical temperature (Tc)

INTRODUCTION

In flip chip technology for quantum processor application, superconducting solder materials are essential for connecting bond pads of chips onto the interposer substrate using flip chip technology using bumps. The flip-chip method has been a crucial component of the semiconductor industry mostly because of its lower cost, high yield and superior performance [3,4]. Technology for fine pitch flip-chip bump interconnects is being developed for fast devices like application processors in smartphones and image processors in digital cameras to satisfy the needs for compact designs and reduced manufacturing expenses.

Currently, there are 27 superconducting pure materials. Some materials, including as indium, aluminium, and niobium, have already been employed in integrated circuit production. However, only a few displays intriguing properties that make them perfect for quantum, such as a high critical temperature Tc of more over 1K. The one essential criterion for cryogenic-grade solder material is high ductility at cryogenic temperatures. The ductility of indium alloys is largely independent of temperature due to the presence of several close pack structures in face-centered cubic (FCC) indium. Therefore, solder alloys based on indium have the potential to be used in extreme cold environments. Additionally, indium solders can function at temperatures that are extremely near to their melting point. Tin silver alloy is one of the most frequent solder compounds used for flip-chip bonding. This alloy exhibits stress rupture properties, resulting in increased ductility and enhanced creep resistance [5]. It is also corrosion and oxidation resistance and has lower tendency for electromigration due to higher thermal electrical conductivity. Tin silver alloys are common solders for immersion palladium, immersion gold (ENEPIG) surface finishes, electroless nickel (Ni), electroless nickel immersion gold (ENIG) and Ni-based under bump metallization (UBM). They are widely used in automotive and aerospace applications, as well as consumer and power electronics.

In this work, we demonstrated flip-chip bonding interconnection comparing indium (In) and tin-silver (SnAg) bump for cryogenic applications. Comparing the bonding quality of these 2 materials relative to flip chip process optimization, shear strength, critical temperature (Tc) and electrical testing measurement at room temperature 300K and after multiples thermal cycles from 300K to 100mK.

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EXPERIMENTAL

Top and Bottom Chip Design for Flip Chip

Daisy chain connecting the top and bottom chips is designed to evaluate the comparison between indium and tin-silver bumps for flip-chip bonding in cryogenic applications. The top chip has a dimension of 4.0mm by 4.0mm and 5.5mm by 5.5mm for the bottom chip as shown in Figure 1b. Both top and bottom chip having a bond pad size of 85µm and a pitch of 190µm with the chip thickness of 775µm as show in Figure 1c. The bond pad surface is gold (Au) bond pad surface. Both top chip and bottom chip are connected through a daisy chain to assess the solder ball connection. Stacked silicon module as the test vehicle is used in this study as shown in Figure 1.

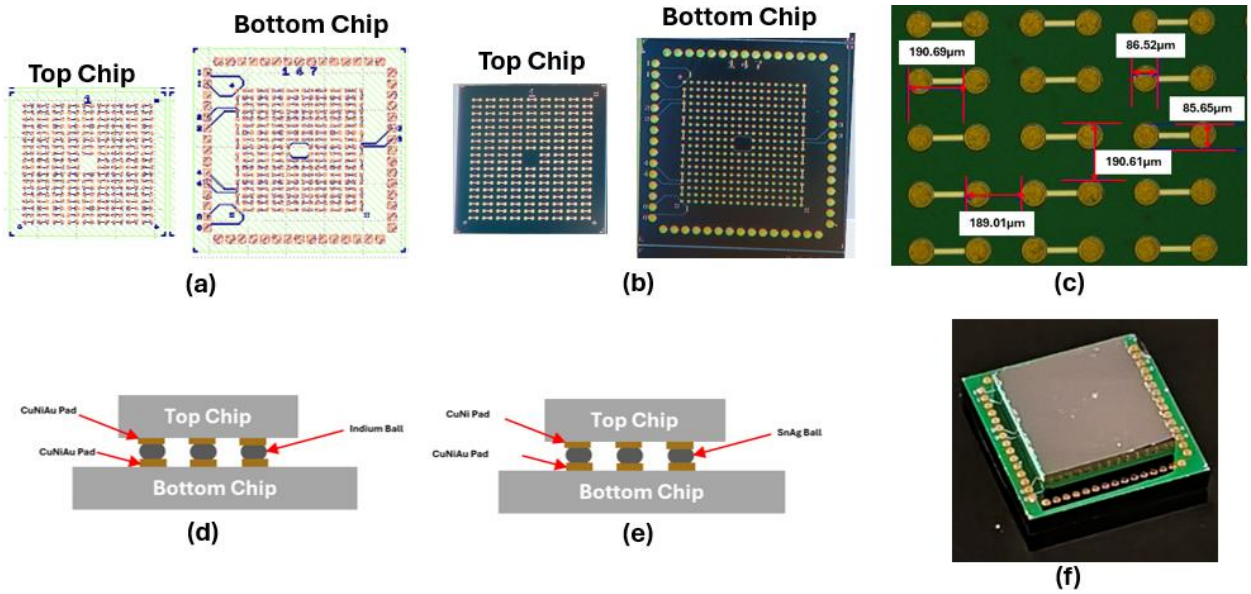


Figure 1: (a)2 silicon chips, top chip with dimension 4.0 mm by 4.0 mm and 5.5 mm by 5.5 mm for bottom chip. (b) Image of actual top and bottom chips after fabrication. (c) Dimension of the bond pad size and pitch. (d) Schematic diagram of flip chip using indium ball. (e) Schematic diagram of flip chip using tin silver bump. (d) Top and bottom chip after flip chip process

Indium ball and Tin Silver Bump for Flip Chip Assembly

A flux printing method is required before placing the indium solder ball on the chip. This involves applying flux through a personalized stainless-steel stencil. Custom design jigs are utilized to put indium solder balls of 100µm. Samples are then reflowed at 180-200°C to generate a solder bump on the pad. Whereas the process of tin silver bumping involves depositing the SnAg alloy onto the bond pads of a silicon wafer using electroplating. After deposition, the solder bumps are reflowed to create a uniform shape and improve the metallurgical bond with the underlying pad as illustrated in Figure 2 below.

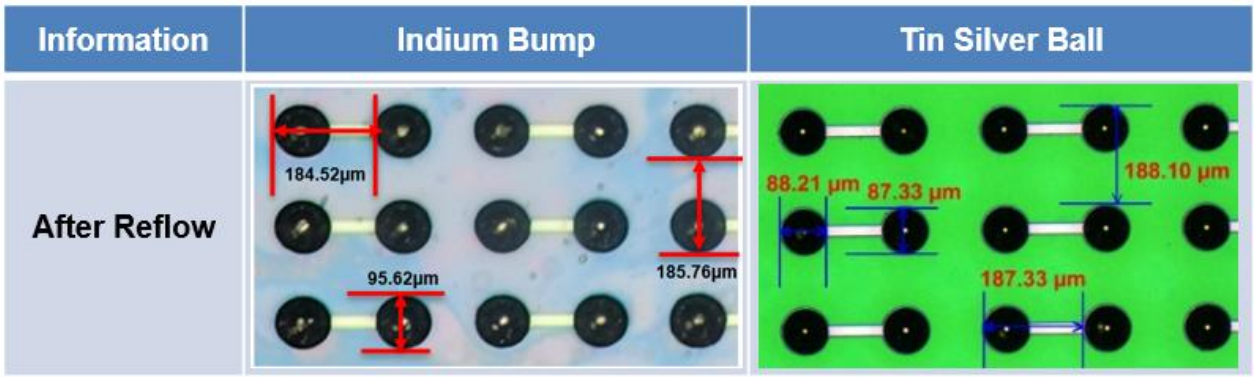


Figure 2: Indium Solder Ball vs Tin Silver Bump after Reflow

A bond force of 0.5N for 1 sec at temperature 145°C is applied during the flip-chip process using Panasonic FCB3 tool for indium solder ball and bond force for tin silver is 50N for 3 secs at temperature 220 °C. Different bonding conditions are required for indium and tin silver due to its Brinell hardness and melting temperatures. After bonding, X-ray imaging is utilized to inspect individual indium bumps for solder ball shorting and abnormalities. The solder joint quality will be checked using DAGE4000HS die shear tester. The failure mode that results from die shear will be addressed. Optical high-power scope will be used to analyze the failure mode.

RESULTS AND DISCUSSION

Gap Height After Flip Chip Process

The indium and tin silver bumps on solder balls quickly oxidize when exposed to vapor and oxygen. Pre-treatment is required prior to flip chip bonding. Argon plasma treatment combined with a 5% H_2 procedure is used before the flip chip to remove oxidation [7]. The ball height of the tin silver after reflow process is around 33.2µm, while the indium after reflow process is about 89.7µm. Flip chip optimization was performed to get the optimal gap height. The gap height achieved for indium following the flip chip technique is around 80.3µm, whereas for tin silver it is 24.8um as shown in Figure 8. This analysis shows that the flip-chip bonding approach produces well-formed indium bump interconnects while preserving top-to-bottom chip parallelism for both indium and tin silver.

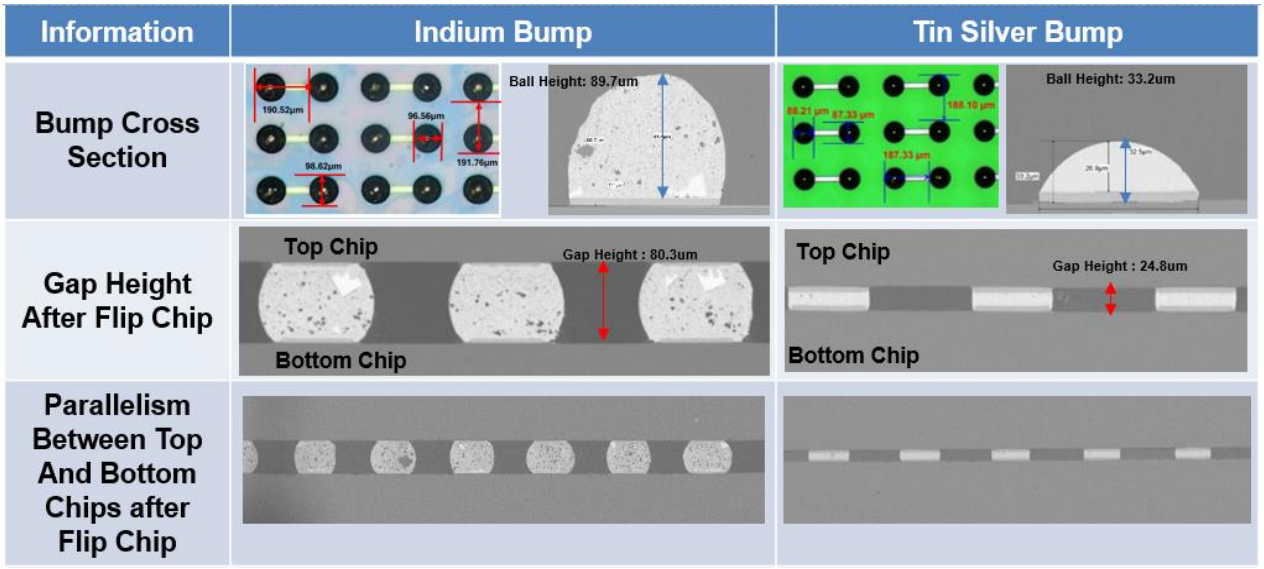


Figure 3: Indium Solder Ball vs Tin Silver Bump Cross Section after Flip Chip Process

Shear Test & Fracture

Both indium and tin silver exhibit bulk solder fracture during die shearing, showing that tin silver and indium have high adhesion to the bonding pad. The averages for tin silver and indium die shearing over 5 samples are 13.551kg and 1.523kg, respectively. Tin silver has a greater die shear measurement than indium because of its higher Brinell hardness of 0.9 while indium has a Brinell hardness of 15. When comparing the failure modes of indium and tin silver, indium has greater ductility and malleability under high power scope, as illustrated in Figure 4. Indium is exceptionally ductile as compared to tin silver due to its unique crystal structure and the way its atoms interact. Specifically, the face-centered tetragonal structure of indium allows for easy movement of atoms relative to each other under stress, making it highly malleable and able to deform significantly before fracturing. This is further enhanced by its softness and low melting point, which allows it to retain its ductility even at very low temperatures.

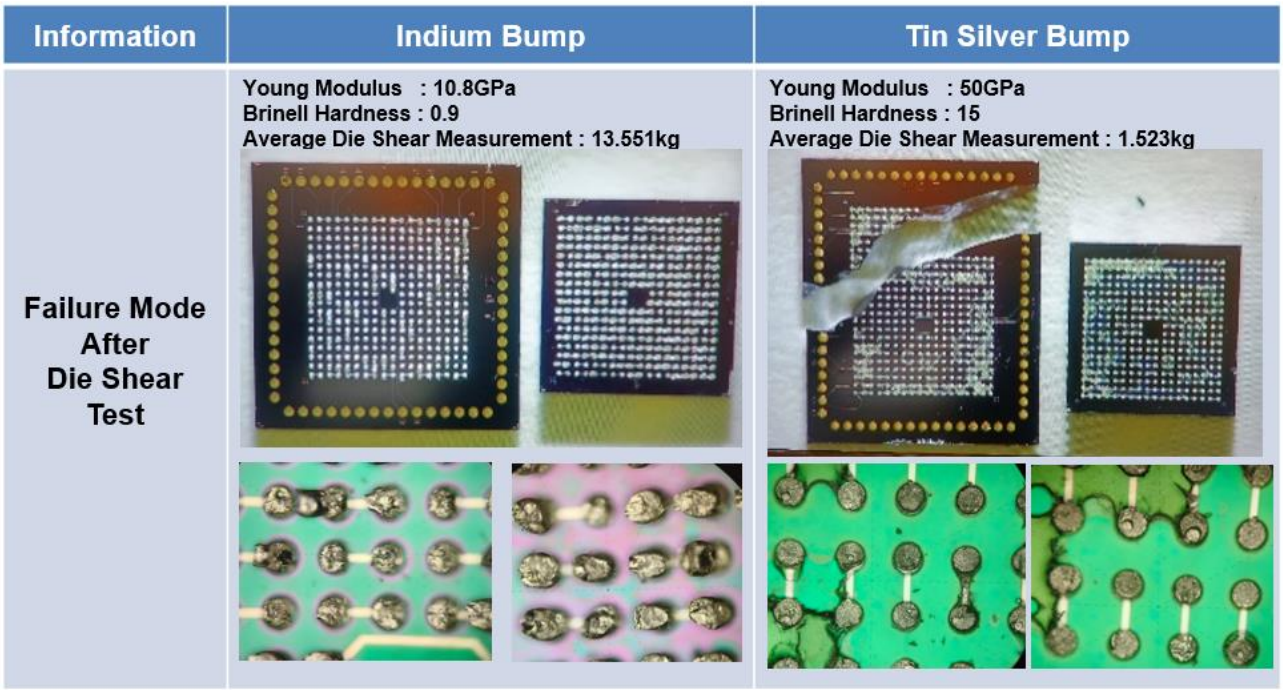


Figure 4: Indium Solder Ball vs Tin Silver bump After Die Shearing

Critical Temperature (Tc) & Thermal Cycles Results

The critical temperature (Tc) is the temperature below which a material transforms into a superconducting state with zero electrical resistance. Indium superconductivity occurs at around 3.2K, while tin silver superconductivity occurs at about 3.32K as shown in Figure 5 below.

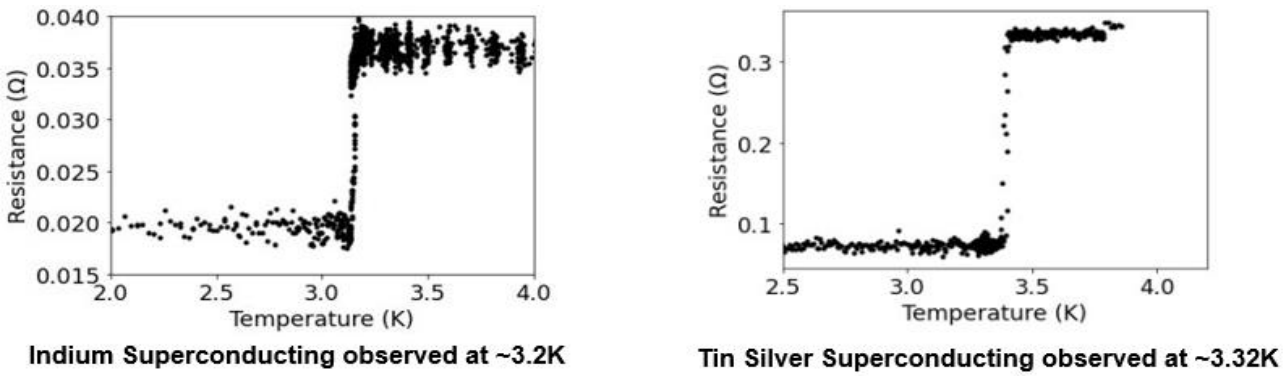
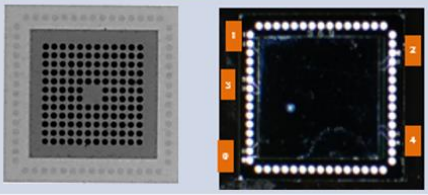
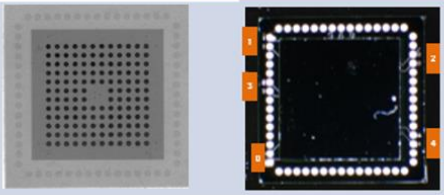


Figure 5: Critical Temperature for indium and tin silver

Cryogenic thermal cycling is a process in which materials are subjected to numerous cycles of extremely low temperatures, often below -150°C, and subsequently returned to ambient temperature. The underlying mechanism is related to the material's response to temperature changes. At very low temperatures, materials tend to contract, and at higher temperatures, materials expand, creating internal stresses. These stresses, when repeatedly applied, can rearrange the material's microstructure, leading to the observed changes in properties. Both tin silver and indium can withstand up to 10 thermal cycles from 300K to 100mK, with no significant resistance difference. Resistance measurement before and after each thermal cycle is illustrated in Figure 6.

Information	CuNiAu/In	CuNiAu / CuNiSnAg
X-Ray after FC / Optical Image		

Measurement

Measurement Point	Before TC	After 1st TC	After 2nd TC	After 3rd TC	After 4th TC	After 5th TC
0-4	17.0Ω	16.1Ω	19.7Ω	19.3Ω	21.0Ω	20.6Ω
0-3	22.6Ω	23.1Ω	24.3Ω	23.3Ω	24.3Ω	24.3Ω
0-2	29.7Ω	30.5Ω	31.9Ω	30.5Ω	32.2Ω	31.8Ω
0-1	36.5Ω	38.0Ω	38.5Ω	38.1Ω	40.1Ω	38.8Ω

Measurement Point	After 6th TC	After 7th TC	After 8th TC	After 9th TC	After 10th TC
0-4	19.8Ω	20.1Ω	20.3Ω	20.9Ω	22.6Ω
0-3	25.1Ω	26.1Ω	26.5Ω	25.2Ω	27.7Ω
0-2	30.8Ω	29.8Ω	31.8Ω	34.1Ω	37.1Ω
0-1	37.1Ω	36.1Ω	38.1Ω	42.0Ω	45.3Ω

Measurement Point	Before TC	After 1st TC	After 2nd TC	After 3rd TC	After 4th TC	After 5th TC
0-4	10.3Ω	11.4Ω	10.1Ω	11.5Ω	11.7Ω	12.9Ω
0-3	17.4Ω	18.4Ω	18.5Ω	19.0Ω	19.3Ω	20.3Ω
0-2	23.6Ω	25.6Ω	25.6Ω	24.7Ω	26.0Ω	26.9Ω
0-1	31.3Ω	31.8Ω	30.2Ω	30.8Ω	30.8Ω	31.9Ω

Measurement Point	After 6th TC	After 7th TC	After 8th TC	After 9th TC	After 10th TC
0-4	13.0Ω	10.9Ω	11.1Ω	13.1Ω	12.9Ω
0-3	20.6Ω	18.9Ω	18.1Ω	20.3Ω	21.3Ω
0-2	27.0Ω	24.9Ω	23.4Ω	26.2Ω	26.4Ω
0-1	33.2Ω	33.9Ω	31.2Ω	39.2Ω	38.7Ω

Figure 6: Indium and Tin silver Thermal Cycle up to 10 cycles

SUMMARY AND CONCLUSION

- ✓ With flip chip parameters optimization, both SnAg and indium bump interconnects generate a well-formed structure and preserve parallelism between the top and bottom chips without solder bump short.
- ✓ Both indium & SnAg show bulk solder fracture upon die shearing indicating SnAg and indium have good adhesion to the bonding pad. SnAg shearing average measurement is 13.551kg while indium average shearing measurement is 1.523kg. SnAg is having higher die shear measurement due to higher hardness properties as compared to indium.
- ✓ Experimental reveal SnAg critical temperature (Tc) is 3.32K while indium Tc is 3.2K.
- ✓ Both SnAg and indium survive thermal cycling for up to 10 rounds with electrical shown no significant resistance different before and after Thermal Cycles (TC). Testing for TC to beyond 10 cycles for SnAg and indium are still ongoing.

Indium is generally preferred over SnAg for cryogenic applications due to its superior ductility and malleability at extremely low temperatures, which allows it to maintain a reliable seal and resist cracking. Indium remains soft and pliable at cryogenic temperatures, allowing it to deform and fill imperfections in mating surfaces, creating a hermetic seal.

✓ ACKNOWLEDGEMENTS

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