Testing Multiple High-Speed Channels using Automated Test Equipment (ATE), SOC 93K, in parallel

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ABSTRACT

High Bandwidth Memory (HBM) requires high speed data transfer between IO chips and IO to Memory stacks mounted on an interposer. KGD HBM stacks and IO chips from different vendors are mounted on high data rate/bandwidth interposer. In a multichiplet device packaging process, moving tests from final test, to be done at wafer level entails high equipment cost [4] such as prober, probecard, but has lower scrap cost. Lower scrap cost means higher yield, with respect to the current packaging technologies such as 2.5D/3D and Chiplets. Once a KGD is mounted on the interposer (and substrate) it cannot be removed if the interposer is tested faulty, wasting full package [4]. This paper discusses test methodology to test high speed data rate interconnections on the interposer prior to mounting the KGD HBM, IO chips and other chips (see Fig1 below). High end DSO(Digital Storage Oscilloscopes) can test from 1 to 4 channels with relative ease. However, when the number of channels is in groups of 8,16-bit bus etc, using an ATE becomes more advantageous. One of the major advantages is, ATE can test multiple channels simultaneously, hence testing multiple channels becomes more feasible using an ATE. The different channels results can be overlaid on a single plot. The final overlay plot provides important information on which channel output is affecting the overall performance of the high-speed bus. Eye diagram [2] is an important signal integrity test to understand the quality of the communication channel in a digital system, the eye diagram provides information on the quality of the transmission line and the bandwidth of the channels. This paper discusses how an ATE could be effectively used to construct an eye diagram using shmoo plot feature of an ATE, appropriately termed Eye Diagram shmoo plot. Furthermore, as ATE can test multiple channels simultaneously, it speeds up testing on a large scale, such as testing an entire wafer. The test methodology developed herewith is a part of a fine pitch high speed channel project, where a wafer test was built with 24 high speed channels to emulate a HBM (High Bandwidth Memory) application with a bump pitch of 55um, to demonstrate the fine pitch [3] probing and functionality using ATE. For the 24 channels simultaneously tested the result showed that 2 traces had smaller eye-width and eye-height compared to the rest of the traces, however the focus of this paper are not those results but rather how the eye diagram was implemented in the ATE level testing. The current setup uses an Advantest 93K tester coupled with a 12" Tel prober. The ATE consists of 3x PS1600 cards with a max data rate of 1.6Gbps. For higher data rates upto 9G, PS9G card can be used. With the PS1600 card, we were able to test upto 1Gbps and eye diagram plotted for all 24 traces. A fine pitch,55um, probe card was built with 24 HBW channels, to test the HBM wafer and validate the test methodology.

Fig 1. below shows an eye diagram plotted for one of the channels, P9, using shmoo plot. The basic parameters such as eye width and height can be extracted from the shmoo [1] plot shown herewith.

I. Introduction:

As shown in fig 1. below, the test is moved from final assembly of 2.5D/3DICs to location after wafer fabrication.

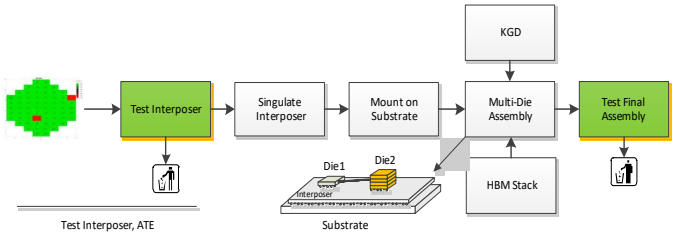

Figure 1 : Moving the test point from final assembly to test after wafer fabrication.

To facilitate high data rate testing of HBM interposer, the setup required is shown below in Fig 2. The setup includes an ATE (Automated Test Equipment) Advantest SOC 93K, ATE software SmarTest v8.3.5, TEL prober WDF 12DP+, HBM wafer is used. The ATE is a tool which can be programmed using smartest v8.3.5 to output test PRBS (pseudo random binary sequence) pattern @ 1Gbps.

The TEL prober is a tool which will load the HBM wafer for test. Fig 2. below show the setup using SOC 93K and TEL prober was used for testing.

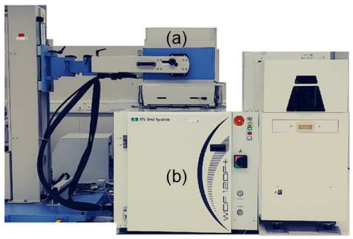

Figure 2 ATE setup to test HBM interposer. a) ATE b) Prober

HBM wafer was fabricated with 24 pair of IO lines to simulate high speed interconnection between IOs mounted at final assembly, to validate the test methodology. Each of the 24 lines was fabricated with input+ and GND line.

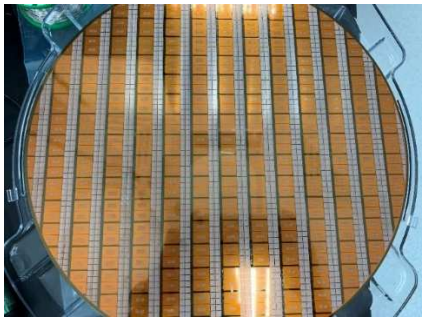

Figure 3 HBM wafer fabricated with 24 IO Lines

A total of 96 bumps were fabricated on the die, 48 bumps on tx side and 48 on the rx side. Each of the bump pair (tx+, rx+, GND) are connected via traces. Fig. 4 below shows bump layout for simulation of interconnections between high speed KGDs, such as memory to memory, IO-IO, Memory-IO connections

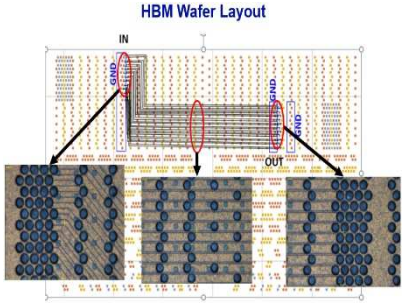

Figure 4 . Bump layout on a HBM interposer.

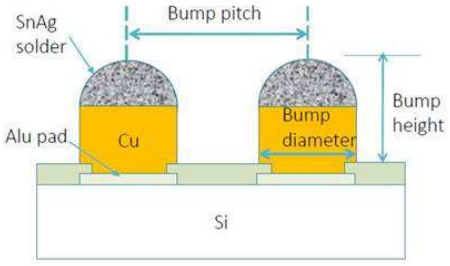

Figure 5. Copper pillar bump

Due to fine pitch of 55um, copper pillar bump were fabricated as shown in Fig 5 above.

II. Probe card:

To test the interposer, probe card design consideration such as fine pitch probe head design, probecard pcb suitable for high data rate application, able to perform better than 3Gbps. The probecard was designed to be a vertical probe card with 25um flat probe tip so that the surface contact is maximized when contact with the copper pillar bump. This is depicted in Fig 6 below. The probe tips were designed to have lower contact resistance and lower inductance, more suitable for high data rate application.

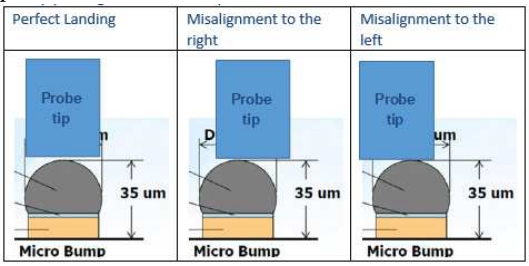

Figure 6. Flat probe tip position w.r.t to the ubump on HBM wafer

Fig 7 below shows HBM probecard built to test the HBM interposer discussed previously. The probe head was modified from a standard HBM layout probe head to include only 24 IO lines. Rest of the connections on the probe head were unpopulated. Top view of the probe-head pin layout is shown in Fig 8 below. The layout, in Fig 8, shows, signal is injected into left portion and output is observed at the receiving end, at the right portion of the probe card

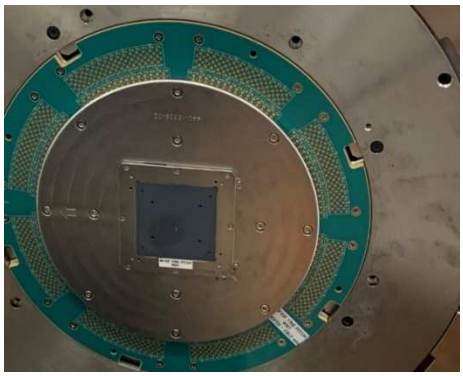

Figure 7: HBM probe card suitable for high-speed applications

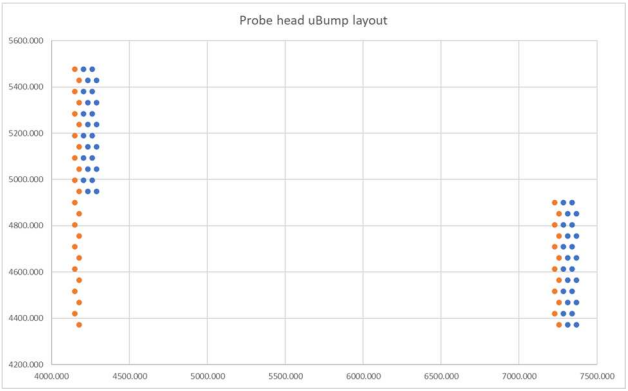

Figure 8. Probe head uBump layout

III. Test Methodology:

To test the interposer, first all 24 IO lines were checked for continuity, data for the 24 IO lines is show below in Table 1. Resistance is calculated for each of the 24 IO trace, by dividing 1mA injected current by voltage measured. As shown from Table 1 below, the trace resistance ranges from 30 – 39 ohms. Simulation performed on some IO lines showed that the simulated resistance value, 33.5 ohm was very close to the average measured value of ~34.5 ohms

Pin Name/Die Location	X5Y3	X6Y9	X1Y9	X12Y9	X7Y16
P1p	33.9849705	36.2357735	32.8258197	33.3807897	33.3889415
P2p	32.3083704	34.0167175	31.1792057	31.7439266	31.1639123
P3p	37.3960614	39.6624328	36.2620706	36.8160777	36.8073774
P4p	33.9573785	35.6534463	32.2362938	32.7834985	32.8072551
P5p	30.3825452	32.1119422	28.6976132	29.2620549	28.6762245
P6p	34.541272	36.8265102	32.8758049	33.9699618	33.9783079
P7p	36.2516237	37.965382	34.5294653	35.092046	35.1091174
P8p	33.9316393	36.2056144	32.7981746	33.344999	33.344999
P9p	34.3896261	36.7014981	33.2631495	34.4313432	33.2631495
P10p	34.0226248	35.7481191	32.9029011	33.4671525	32.3060588
P11p	31.5921094	32.1483625	28.7158837	29.3099881	28.7230787
P12p	35.1711171	36.3156274	33.4379399	34.0266069	33.4461438
P13p	34.9652296	36.6793368	33.2511202	33.8306602	33.267187
P14p	34.5903003	36.3066409	33.4542033	33.4623373	33.4623373
P15p	37.8261277	38.9401475	36.1029248	36.6832678	36.1029248
P16p	32.2681349	34.5798222	31.1327912	31.6966185	31.1327912
P17p	36.2486698	38.5521445	35.1317926	35.6947583	35.7034074
P18p	34.0076345	35.7234582	32.3154182	33.4275558	32.847757
P19p	37.4249961	39.7020923	36.2726014	36.8623694	36.2994645
P20p	36.2999424	36.8191525	33.9550829	34.5426268	33.9794067
P21p	37.425883	38.5787451	35.7106727	35.6933013	35.7193661
P22p	35.6875357	37.4016396	33.3855518	34.5362605	33.9818366
P23p	33.3768686	35.0467685	32.2192237	32.7898794	32.2034646
P24p	37.9938692	39.1561736	35.7417323	36.8683471	36.2876089

Table 1. Resistance measured for each of the 24 IO fabricated on the HBM interposer

Table 1 shows the resistance measured for each of the 24 IO lines range from 28 to 39 ohms. Wafer maps plotted for these

IOs are shown in Fig 9 to 11. Wafer maps below depicts resistance distribution pattern for all 24 IO lines across the entire wafer. As seen for P3, P15, P20 and P22 traces, the reddish portion in the centre depicts shows high resistance compared to the rest of the wafer area.

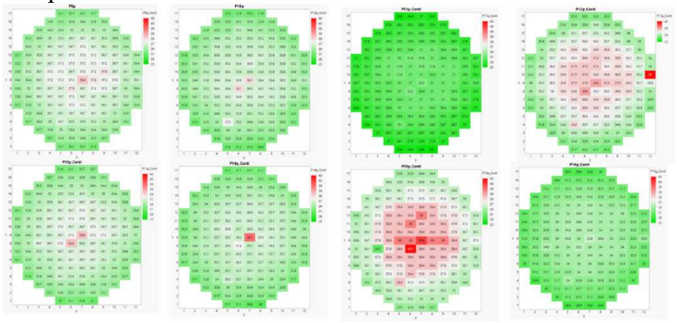

Figure 9 :Full Wafer HBM Channel Resistance Test (P1p to P8p)

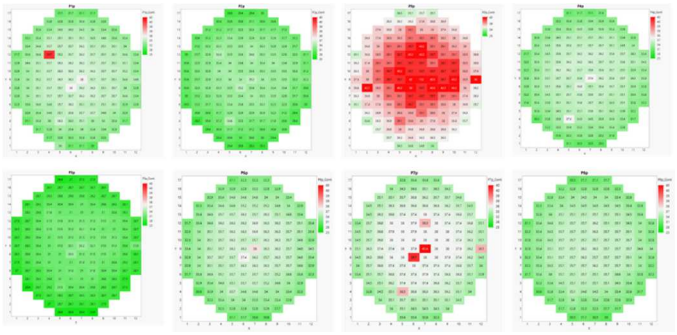

Figure 10. Full Wafer HBM Channel Resistance Test (P9p to P16p)

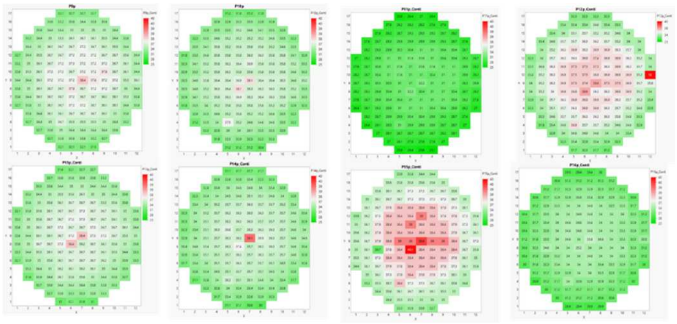

Figure 11 Full Wafer HBM Channel Resistance Test (P17p to P24p)

IV. Eye diagram shmoo plots:

Eye diagrams are used to characterize high speed digital signal in the time domain such as rise and fall time, jitter, attenuation etc. SOC 93K ATE doesn't have the capability of displaying eye diagram directly and is created using shmoo plot feature of ATE Only P9G digital cards from Advantest can create and display eye diagram without using shmoo plot feature of SmarTest software. The technique very similar to how eye diagrams are displayed on a DSO. The eye is derived by folding parts of the waveform (as a 3bit sequence) over the entire duration of the pattern. Eye diagram requires a PRBS pattern. A sample of which is shown below in Fig 12. The pattern was hand coded for all 24 IO lines for vector length of 255. P1p refers to the input where as P1m refers to the received digital pattern, input to the ATE pin electronics.

Signal
X-Mode: x3
Site Memory Sharing: OFF

Vector#	Instruction	Comment	P12m	P12p	P11m	P11p	P10m	P10p	P9m	P9p	P8m	P8p	P7m	P7p	P6m	P6p	P5m	P5p	P4m	P4p	P3m	P3p	P2m	P2p	P1m	P1p
0			H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L
1			H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L
2			L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H
3			L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H
4			H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L
5			L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H
6			H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L
7			H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L
8			H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L
9			H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L
10			L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H
11			L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H
12			L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H
13			L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H
14			H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L
15			L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H
16			H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L
17			H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L

Figure 12: Pattern for creating eye-diagram using shmoo plot feature of ATE

Eye diagrams shmoo plots are created by assigning one of the device parameters on one axis and another device parameter on y-axis. This is referred to as 2-D shmoo plot. x-axis is assigned the t-parameter (time parameter) whereas the y-axis is assigned the output swing parameter. When both the variables' values are swept within a certain range, eye is created as shown in Fig 14 below. At each intersection of x and y values, functional test is run. A red dot/square is plotted if the test fails, or else it will plot it as a green dot/square. The green portion (Fig 14) shows the passing area of the device, which incidentally is also the eye-height. The eye-width is the max horizontal distance between any two passing points. The distance is also equal to 1UI. As the probe head design is confidential and not disclosed by the vendor/supplier, simulation with MLO line spacing of 10um show results very close to the measured eye diagram. Comparison is shown below in Fig 13 and Fig 14.

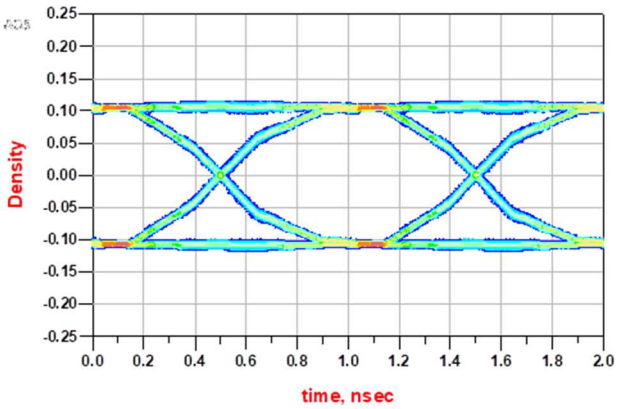

Figure 13. Eye diagram created using shmoo plot of an ATE

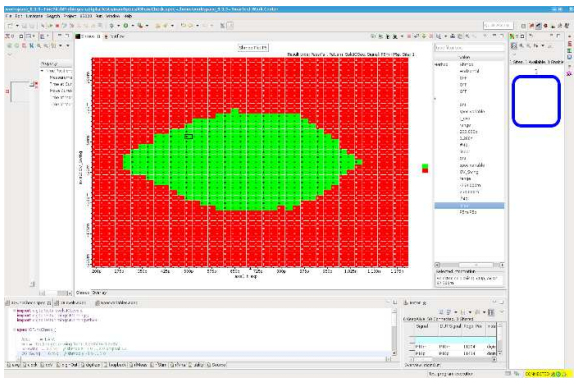

Figure 14. Eye diagram of P5 HBM trace line

Eye diagrams were plotted for all hbm trace lines, 1-24 as shown in Fig 16 and Fig 17 below. As noted from the eye diagram from Fig 16 and 17, it was seen that P21 and P23 have the worst performance from the rest of the trace lines. The eye height and width measured from the good and bad trace lines are shown in Table 2. This was verified by doing near end xtalk measurement by probe card vendor and is depicted in Fig 15 below. The near end xtalk measurement shows that cross talk is worse for P21 and P23.

Channel # (Die 1)	Eye Width (ps)	Eye Height (mV)
P5	787 (78.7% UI)	225 (45% EA)
P9	840 (84% UI)	225 (45% EA)
P21	761 (76.1% UI)	137 (27.4% EA)
P23	709 (70.9% UI)	112 (22.4% EA)

Table 2 : P5 and P9 are good hbm trace lines, P21 and P23 are bad trace lines.

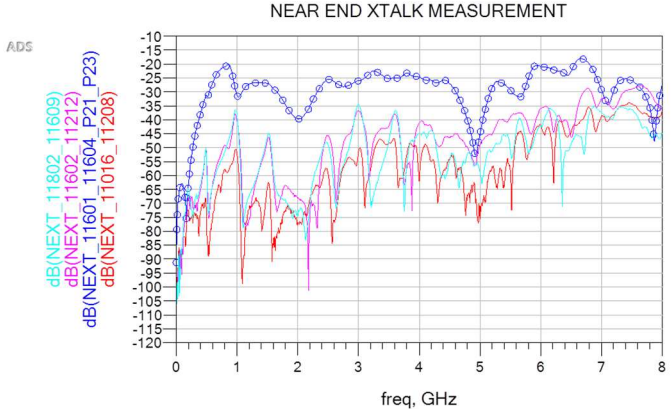

Figure 15 : Near end xtalk measurement

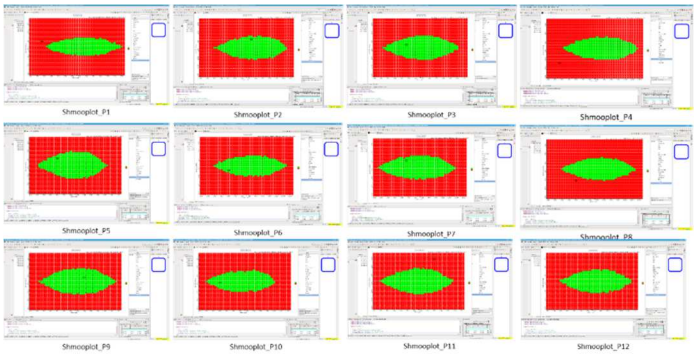

Figure 16. Eye Diagram Measurement of 24 HBM Channels (Channels 1 to 12)

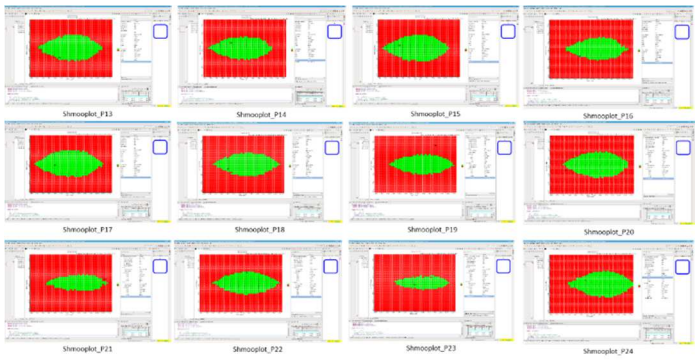

Figure 17. Eye Diagram Measurement of 24 HBM Channels (Channels 13 to 24)

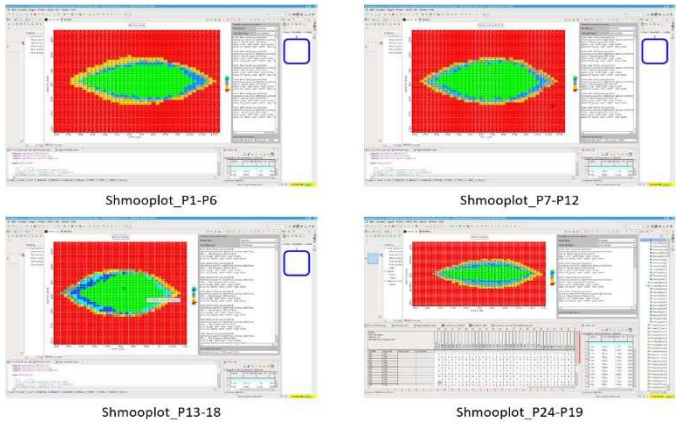

Figure 18. Overall eye diagram shmoo overlay for a group of channels such as P1-P6, P7-P12, P13-P18 and P19-P24

V. Conclusion:

ATE can perform simultaneous eye measurements of a group of HBM traces/channels using shmoo plot feature of ATE, unlike DSO which is restricted to a few channels. Critical eye parameters such as eye-height and width can be extracted from the eye diagram shmoo plots. The tests identified defective channels P21 and P23, which was later confirmed by performing near end xtalk measurement, at the supplier factory. With the overlap feature of shmoo plots, it is possible to determine which channel contributes to performance degradation. ATE is a powerful tool to characterize high bandwidth connections.

VI. Acknowledgment:

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