

Embedded Micro-Pin Fin Heat Sink of Two-Phase Liquid Cooling for High Heat Flux 3D ICs

Huicheng Feng
*Institute of Microelectronics,
 Agency for Science, Technology
 and Research (A*STAR)*
 Singapore
 fenghc@ime.a-star.edu.sg

Gongyue Tang
*Institute of Microelectronics,
 Agency for Science, Technology
 and Research (A*STAR)*
 Singapore
 tangg@ime.a-star.edu.sg

Xiaowu Zhang
*Institute of Microelectronics,
 Agency for Science, Technology
 and Research (A*STAR)*
 Singapore
 xiaowu@ime.a-star.edu.sg

Boon Long Lau
*Institute of Microelectronics,
 Agency for Science, Technology
 and Research (A*STAR)*
 Singapore
 laubl@ime.a-star.edu.sg

Ming Ching Jong
*Institute of Microelectronics,
 Agency for Science, Technology
 and Research (A*STAR)*
 Singapore
 mcjong@ime.a-star.edu.sg

Keng Yuen Jason Au
*Institute of Microelectronics,
 Agency for Science, Technology
 and Research (A*STAR)*
 Singapore
 jason_au@ime.a-star.edu.sg

King Jien Chui
*Institute of Microelectronics,
 Agency for Science, Technology
 and Research (A*STAR)*
 Singapore
 chuikj@ime.a-star.edu.sg

Jing Lou
*Institute of High Performance
 Computing, Agency for Science,
 Technology and Research
 (A*STAR)*
 Singapore
 loujing@ihpc.a-star.edu.sg

Hongying Li
*Institute of High Performance
 Computing, Agency for Science,
 Technology and Research
 (A*STAR)*
 Singapore
 lih@ihpc.a-star.edu.sg

Duc Vinh Le
*Institute of High Performance
 Computing, Agency for Science,
 Technology and Research
 (A*STAR)*
 Singapore
 ledv@ihpc.a-star.edu.sg

Abstract— This paper presents a novel two-phase liquid cooling solution of high-power integrated circuit (IC) chips using embedded micro-pin fin heat sink (MPFHS). A titanium thin film heater and two resistance temperature detectors (RTDs) are deposited on the active surface of a silicon chip, to simulate the functional dice and measure chip temperature, respectively. The backside surface of silicon chip is etched to form the embedded MPFHS, and then bonded to a silicon cap. Printed circuit board (PCB) is designed and fabricated to power the heater and collect signals from RTDs. The coolant (deionized water) is fed and collected through the thin side openings of the chip. Manifolds are 3D printed with stainless steel to properly match the openings. Experimental setup of two-phase liquid cooling loop is built for testing and characterization. A wide range of coolant flowrate and heat flux of heater is tested. Heat flux up to 188 W/cm^2 is achieved with small coolant flowrates experimentally. Chip temperature and temperature gradient linearly increase as heat flux increases, which can be reduced by increasing coolant flowrate. In two-phase regime, chip temperature and pressures at inlet and outlet are highly fluctuated, which is not preferable in chip cooling. Further investigations are to be carried out for a more stable cooling.

Keywords—embedded heat sink, micro-pin fins, two-phase cooling, high heat flux, IC chips

I. INTRODUCTION

The footprint of transistors keeps reducing as their number in a single integrated circuit (IC) chip increases in the past decades following the Moore's Law. This is leading to the scaling limit of semiconductor process technology. By stacking IC chips vertically, three-dimensional (3D) ICs can increase the number of IC chips without further shrinking the footprint,

hence can circumvent the scaling limit accordingly [1,2]. The high integration of 3D ICs leads to increased performance and lowered cost, and correspondingly a much higher heat flux. Therefore, heat dissipation becomes a bottleneck in the development of 3D ICs and requires high-efficient cooling solutions. Liquid cooling is a promising one and widely used in electronics cooling [3-8], among which two-phase liquid cooling can achieve a higher heat flux as it utilizes latent heat of coolant [9-14]. Thus, it shows a great potential for 3D IC cooling. However, the phase change of coolant in small, confined channels makes it a complex phenomenon. The temperature and pressure of the channels are highly fluctuated [15-18], which is not preferable for good chip performance.

Therefore, we aim to develop a novel embedded two-phase liquid cooling solution for 3D ICs. As the first step, this paper studies the single-layer case to facilitate our next step on multiple-layer ICs. A chip containing a thin film heater, two thin film resistance temperature detectors (RTDs), and an embedded micro-pin fin heat sinks (MPFHS) is designed and fabricated. It is tested in a two-phase liquid cooling testing setup with wide ranges of coolant flowrate and heater heat flux. High heat fluxes are achieved at small flowrates.

II. METHODS

The testing sample is composed of a silicon cap, a silicon chip, and a PCB (Fig. 1(a)). The silicon chip contains a titanium thin film heater and two RTDs on the active surface (Fig. 1(b)). Its backside surface is etched for micro-pin fins (Fig. 1(c)), and then bonded to the cap using our in-house high-temperature non-conductive epoxy adhesive, forming the embedded MPFHS.

The coolant is feed and collected through the side openings of the MPFHS (Fig. 1 (d)). The MPFHS is bonded to PCB using solder balls. The assembled testing sample is shown in Fig. 2.

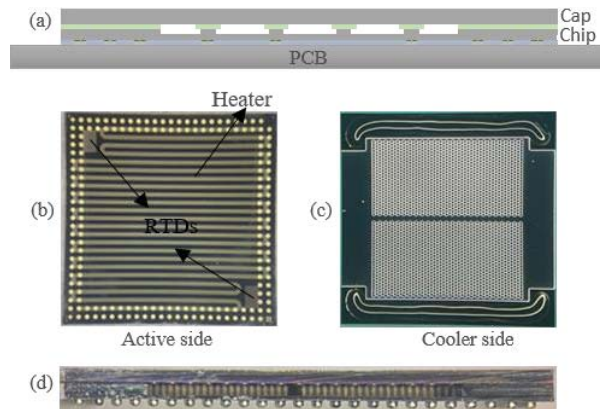


Fig. 1. (a) Schematic of the testing sample. (b) Chip bottom surface (active side) containing a heater and two RTDs with resistances 380Ω and 620Ω , respectively. (c) Chip top surface (cooler side) with etched micro-pin fins in staggered arrangement, of diameter $100 \mu\text{m}$, pitch $150 \mu\text{m}$, and height $250 \mu\text{m}$. (d) Side view of the chip bonded with cap. Chip footprint is $10 \text{ mm} \times 10 \text{ mm}$.

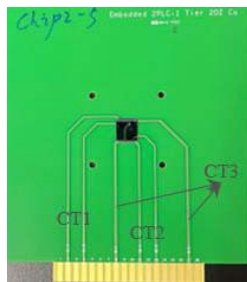


Fig. 2. Testing sample. CT: copper trace. CT1, CT2, CT3 are used to collect signals from RTD1, RTD2, and supply power to heater, respectively.

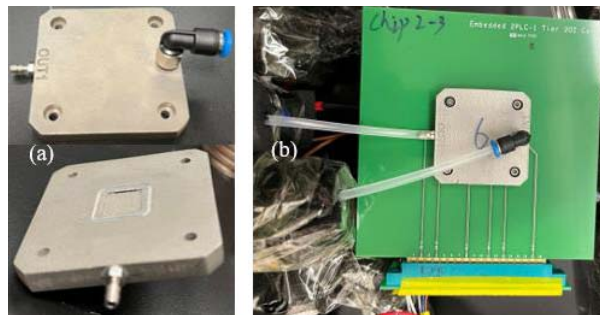


Fig. 3. (a) 3D printed manifold (EOS M 290, EOS Stainless Steel 316L). (b) Testing sample with manifold.

To properly feed and collect coolant from MPFHS, the manifold is 3D printed using stainless steel (Fig. 3(a)). Its bottom surface has a cavity to hold MPFHS. The cavity side walls are printed with openings to match that of chip. An O-ring surrounds the cavity for coolant sealing. The manifold is

mounted on the testing sample and eventually connected to the testing setup (Fig. 3(b)).

The testing setup is designed and built (Fig. 4). It is majorly composed of a coolant reservoir, a gear pump, a condenser, a degas module, a data logger, a power source, sensors, valves, etc. Besides the two RTDs inside testing sample for chip temperature, we use thermo couples and pressure transducers to measure coolant temperatures and pressures, respectively, at both inlet and outlet of testing section (i.e., the testing chip). The coolant flowrate is measured by a flowrate sensor.

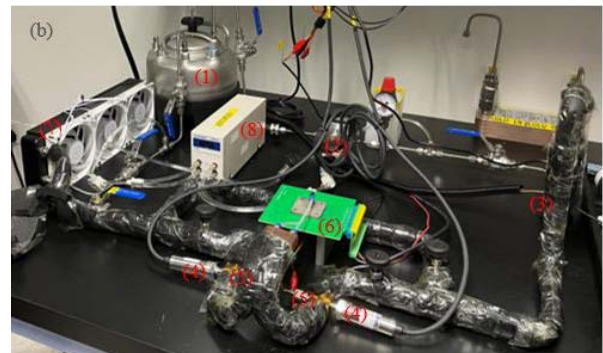
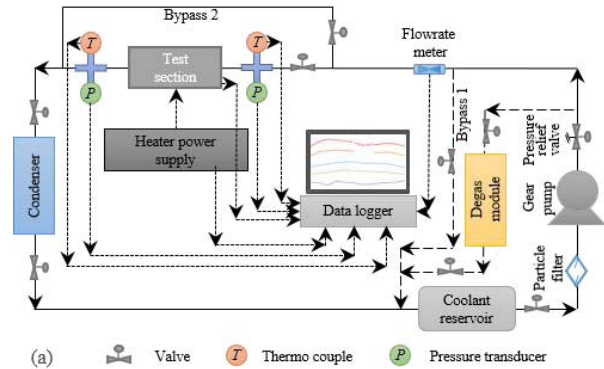


Fig. 4. Testing setup. (a) Schematic illustration. (b) Photo. (1) Coolant reservoir, (2) gear pump, (3) flowrate sensor, (4) pressure transducers, (5) thermo couples, (6) testing sample, (7) condenser, (8) degas module.

III. RESULTS AND DISCUSSION

We use deionized (DI) water as coolant and carried out testing by fix a DI water flowrate and increasing the heat flux of heater. Bypass 1 in Fig. 4(a) is used to adjust the flowrate of DI water going through the testing sample. The inlet temperature of DI water is room temperature, 24°C . The chip footprint is $1 \text{ cm} \times 1 \text{ cm}$.

Fig. 5 shows the testing results at DI water flowrate $73.3 \pm 1.8 \text{ mL/min}$, where 73.3 and 1.8 are the average and standard deviation, respectively. This applies to the whole paper unless otherwise mentioned. The heat flux of heater is increased step by step, up to 188 W/cm^2 . As the chip footprint is $1 \text{ cm} \times 1 \text{ cm}$, the heater power is also up to 188 W. During the testing, the DI

water flowrate slightly increases as heat flux increases (Fig. 5(a)). The reason is that DI water viscosity reduces as temperature increases. As heat flux increases, the DI water temperature at outlet increases, hence DI water viscosity reduces. This makes it easier to flow in the cooling loop. Thus, the flowrate slightly increases.

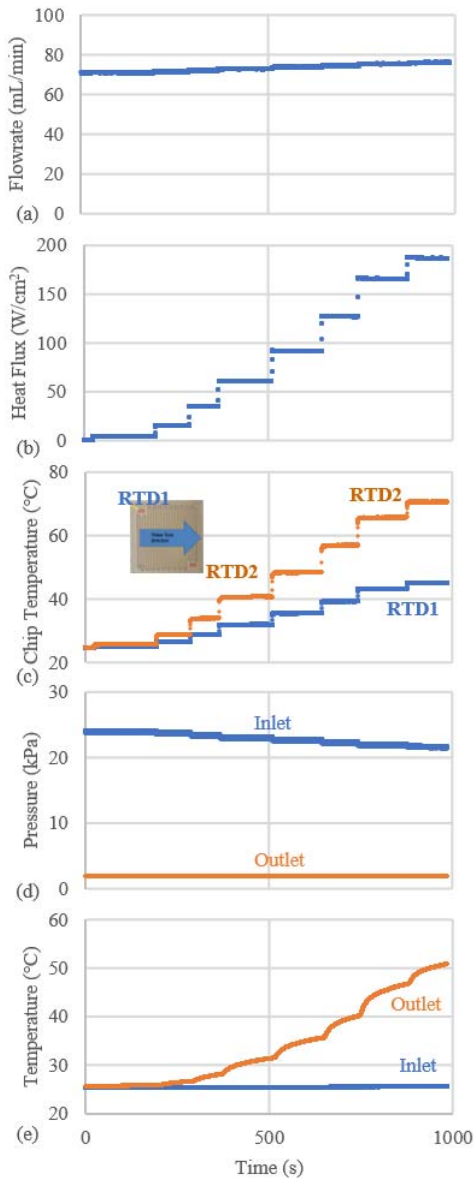


Fig. 5. Cooling results over time at DI water flowrate 73.3 ± 1.8 mL/min. (a) DI water flowrate, (b) heat flux, (c) chip temperatures, and (d) pressures and (e) temperatures of DI water at inlet and outlet.

Clearly, the chip temperature as well as the chip temperature gradient increase as heat flux increases (Figs.5 (b, c)). The two RTDs are located at the inlet and outlet of MPFHS. The

difference of RTD readings shows the temperature gradient of chip. As shown in Fig. 5(e), the outlet temperature of DI water increases as heat flux increases; the inlet temperature of DI water remains constant as the condenser sufficiently cooled the DI water down.

We reduced the flowrate to 32.3 ± 1.3 mL/min and ran another cooling testing as shown in Fig. 6. Same as Fig. 5, the chip temperature and temperature gradient increase as heat flux increases. The pressure drop (i.e., pressure difference between inlet and outlet) across the testing sample is smaller compared to that in Fig. 5(d). This is reasonable as pressure drop is proportional to flowrate. A higher flowrate needs a larger pressure drop. As heat flux increases to 160 W/cm², phase change occurs. The chip temperature is highly fluctuated, as well as the pressures.

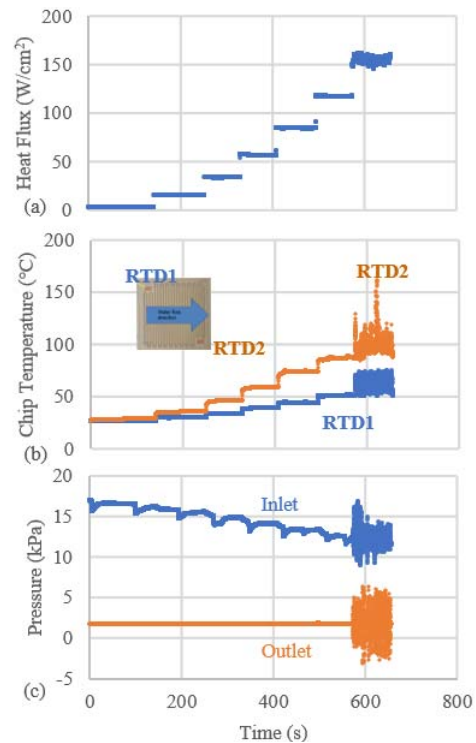


Fig. 6. Cooling results over time at DI water flowrate 32.3 ± 1.3 mL/min. (a) Heat flux, (b) chip temperatures, and (c) pressures of DI water at inlet and outlet.

A clearer picture of two-phase fluctuations can be taken from Fig. 7. We can see that the chip temperature is highly fluctuated (Fig. 7(a)). RTD1 and RTD2 readings are $60.0 \pm 5.9^\circ\text{C}$ and $98.5 \pm 9.3^\circ\text{C}$, respectively. RTD2 generally shows the maximum chip temperature as it is located at the corner of MPFHS outlet. Although the average temperature of RTD2 is below 100°C , i.e., the boiling point of ID water, the transient temperature of RTD2

can be higher and initiate boiling. The highly fluctuated chip temperature is not preferable in chip cooling as chip may be damaged due to the temporal high temperature. This is a common issue in two-phase liquid cooling [19-20] and needs to be studied further for a more stable cooling effect.

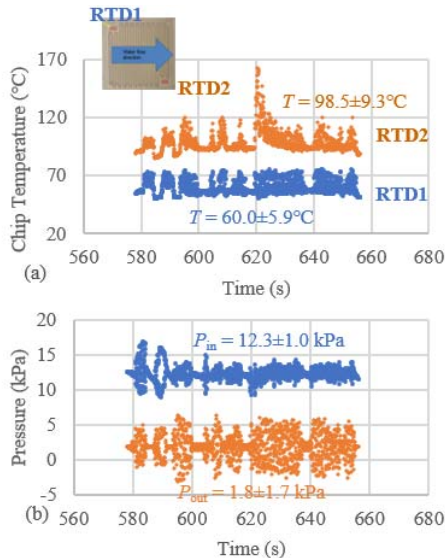


Fig. 7. (a) Chip temperature and (b) pressure fluctuations in two-phase regime at DI water flowrate 32.3±1.3 mL/min and heat flux 160 W/cm².

The pressures are also highly fluctuated in two-phase regime (Fig. 7(b)). This shows a strong boiling in the MPFHS. Vapor bubbles departure from the MPFHS walls and escape through the outlet. The outlet pressure varies more significantly and can even temporarily become negative. This may cause localized backflow. That is the reason of pressure fluctuation at the inlet. The DI water flowrate in two-phase regime is also more fluctuated than that in single-phase regime. The standard deviations of flowrate in two-phase and single-phase are 1.9 mL/min and 1.2 mL/min, respectively.

From Figs. 5(c) and 6(b), we can see that chip temperature increases as heat flux increases at fixed DI water flowrate. To draw a clearer picture, we plot the variation of chip temperature as heat flux increases in Fig. 8. It shows that chip temperatures linearly increase as heat flux increases. As RTD readings are linear to heat flux, the chip temperature difference is also linearly increasing as heat flux increases, as well as the chip temperature gradient. In present experiments, the inlet temperature of DI water is kept to room temperature. To reduce the chip temperature gradient, we can increase the inlet temperature of DI water or increase the flowrate. We can see that both chip temperature and temperature gradient are much smaller in Fig. 8(a) compared to that in Fig. 8(b). For heat flux of 160 W/cm² in Fig. 8(b), it enters two-phase regime. The temperature fluctuates stronger compared to that in single-phase regime as indicated by the error bars.

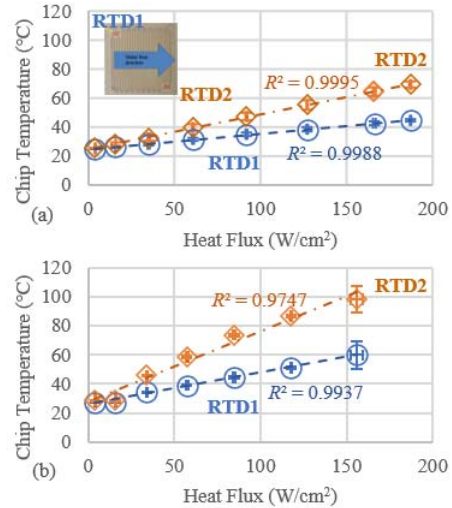


Fig. 8. Variation of chip temperature as heat flux increases at DI water flowrate (a) 73.3±1.8 mL/min and (b) 32.3±1.3 mL/min. Symbols are experimental data. Error bars indicate the standard deviations. Curves are obtained through linear fitting. R^2 is the fitting goodness.

IV. CONCLUSION

In this paper, we experimentally studied two-phase liquid cooling of high-power of IC chips using embedded MPFHS. An IC chip containing a thin film heater, two RTDs, and the MPFHS is designed and fabricated. It is attached to a PCB for electrical connections of heater and RTDs. An experimental setup is built for two-phase liquid cooling of the IC chips. The chip is tested under different coolant flowrates and heater heat fluxes. The results showed that heat fluxes up to 188 W/cm² are achieved at small coolant flowrates. The chip temperature and temperature gradient are linearly increasing as heat flux increases. They can be reduced by increasing coolant flowrate. Chip temperature and coolant pressure at inlet and outlet are highly fluctuated in two-phase regime, which is not preferable in chip cooling. Further studies are underway to achieve a more stable cooling.

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