Nonlinear Thermal Stress/Strain Analyses of Through SiC Via

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Abstract

This paper presents the stress and strain analysis of silicon carbide (SiC) interposer as an alternative to the commonly used silicon interposer or through silicon via (TSV) to utilize the greater thermal conductivity of SiC over Si. The radial stresses and axial strains at the interface during temperature loading are examined as an indication to delamination and cracking failures, due to the difference in coefficient of thermal expansion (CTE) of the copper via, dielectric layer and the Si/SiC. Finite element analysis is performed to investigate the effect of via diameter, via ratio (height/diameter), copper pad, and partial-filled via on the stresses and strains. The Si and SiC interposer impact on the solder joint reliability of SAC solders subjected to thermal cycling is also determined by monitoring the creep strain energy density per cycle (ΔW) of the solders. It is surmised from the simulation results that (1) via diameter 10 µm and below is recommended for low radial stress and axial strain in fully Cu-filled SiC interposer and (2) replacing Si with SiC in interposer results in 39% increase in the maximum ΔW in SAC solders.

Introduction

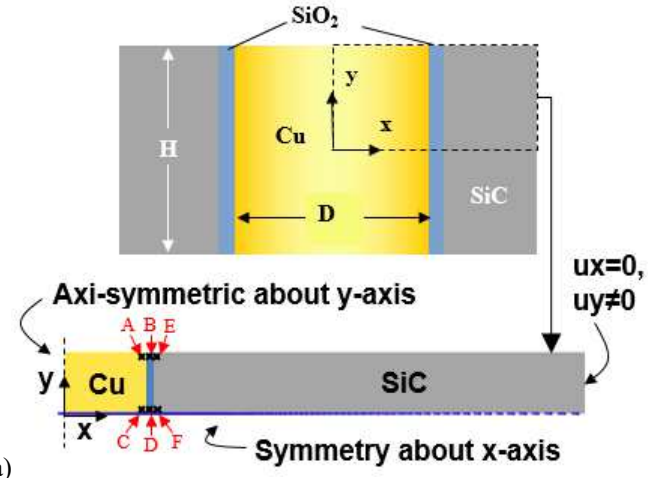
Improvements in Silicon Carbide (SiC) processing has led to higher SiC wafer yields, resulting in greater use of SiC in semiconductor devices. Single-crystal SiC has intrinsic thermal conductivity of ~5X that of single-crystal Silicon. Poly-crystalline SiC thermal conductivity is ~3X for crystalline Si. With this high thermal conductivity and its high electrical resistivity properties, SiC interposer is an ideal choice for very high power and high frequency applications. However, to date, very little work has been performed on non-linear stress/strain of through SiC via. The higher elastic modulus of SiC may induce higher stresses and strains at interfaces, causing detrimental effects to surrounding materials such as copper. During fabrication, cracking and delamination at the interfaces due to the large difference in coefficient of thermal expansion (CTE) between copper and silicon under temperature loading is a concern [1]. This mismatch in CTE also leads to copper protrusion during the annealing process, thus affecting back-end-of-line processing and reliability [2]. An extensive review was done, covering areas in fabrication, electrical test characterization, thermal management and thermo-mechanical analysis on through silicon interposer [3]. Thermo-mechanical analysis is necessary to investigate the impact of SiC on the copper via which affects the reliability of the interposer. Also, the warpage of the SiC interposer and its impact on the rest of the package will be different. Package modelling will be needed to assess the impact of the interposer on the solder joint reliability. A wide range of studies were done on the thermo-mechanical reliability of TSV [1,4-6], the same needs to be done for through SiC via.

In this paper, parametric study on a single via is performed using finite element analysis to investigate the radial stresses and axial strains at the interface under temperature loading. The parameters considered are the via diameter, via ratio (height/diameter), presence of copper pad, and partial-filled copper via compared to fully-filled copper via. Finally, a 3D slice model of an interposer attached to a chip is modeled for both Si and SiC interposer to analyze the interposer impact on the creep strain energy density per cycle (ΔW) of the SAC solder bumps as an indicator to solder joint reliability.

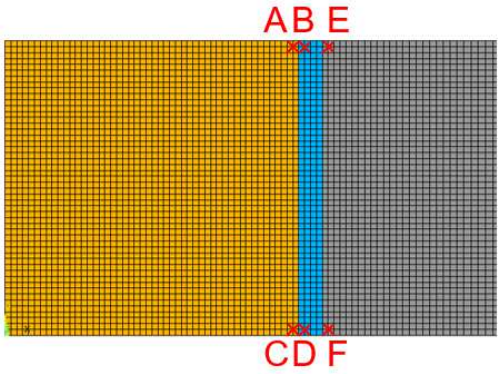
Single via analysis

1.1. Fully Cu-filled through SiC via model

The single via analysis for a fully copper-filled through SiC via is performed using a simple 2D axisymmetric model obtained from one quarter of a single via, consisting of SiC, 1 µm silicon dioxide (SiO_2) layer and the copper via. Figure 1 shows the diagram of the via and finite element model with the applied boundary conditions and the mesh. Critical points of failure are identified at points A, B and E where delamination at the interface of copper, SiO_2 and SiC may occur, and at points C, D and F where mid-plane cracking may occur [1]. Radial stress is monitored at points A, B and E while axial strain is monitored at points C, D and F. A static temperature ramp down is conducted from 125 ºC to -40ºC. The following assumptions were made for the simulation: (1) The barrier (tantalum) layer is negligible, (2) All materials are strained within the elastic zone except for copper, where elastic and plastic relation is used, (3) Stress free temperature is set at 125 ºC, (4) Temperature change is uniform throughout the interposer, (5) Perfect adhesion is assumed at all material interfaces. The via diameter D used in the model ranges from 5 to 25 µm while the via ratio H/D ranges from 1 to 60. Table 1 shows the modelling matrix for the corresponding dimensions. The material properties used are listed in table 2.



(a)



(b)

Fig. 1. Diagram of via and Finite element model (a) and mesh (b)

Table 1. Modelling Matrix

D (µm)	H/D										
5	1	2	3	4	5	10	15	20	30	40	60
10	1	2	3	4	5	10	15	20	30		
15	1	2	3	4	5	10	15	20			
20	1	2	3	4	5	10	15				
25	1	2	3	4	5	10					

Table 2. Material Properties

Material	Silicon	SAC387	Copper	SiO_2	SiC
Young's Modulus (GPa)	131	54.4 @ -40ºC 44.4 @ 25ºC 30.7 @ 75ºC 18.8 @ 125ºC	117	70	466
Poisson's Ratio	0.28	0.4	0.34	0.16	0.21
CTE (ppm/ºC)	2.8	21	17	0.6	2.2
Plastic properties (MPa)		Creep Law A=32000/s B=0.037/MPa n=5.1 Q/R=6530.8	117 @ 0.001 ε 186 @ 0.004 ε 217 @ 0.01 ε 234 @ 0.02 ε 248 @ 0.04 ε		

Shown in Figure 2, the deformation of the via (D=25µm, H/D=1) after cooling from 125 ºC to -40ºC is exaggerated 50X for better visualization. The contraction of copper is larger than SiO_2 and SiC due to its much larger CTE, smaller Young's modulus and higher Poisson's ratio.

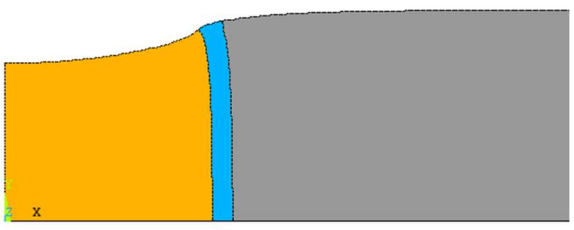
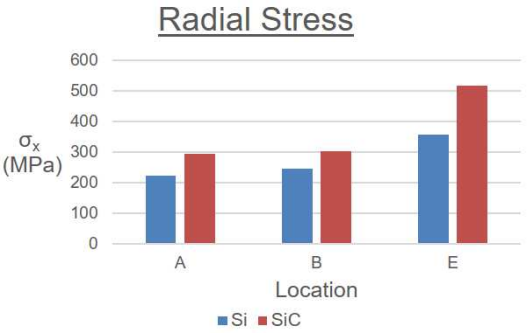


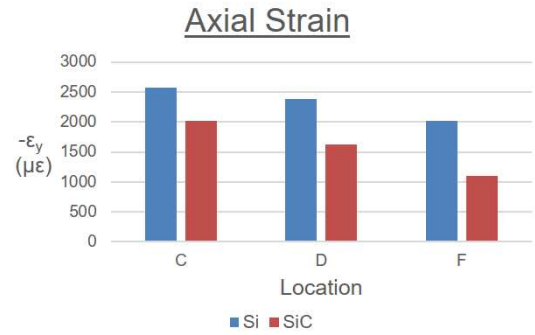
Fig. 2. Deformation of via exaggerated 50X after cooling

1.2. Fully Cu-filled through SiC via model results

The radial stresses and axial strains between Si interposer and SiC interposer (D=25µm, H/D=1) are compared in Figure 3. The SiC interposer experiences greater radial stress at A, B and E by 33%, 23% and 44% respectively due to higher Young's modulus of SiC and a slightly larger CTE difference between SiC and Cu compared to Si and Cu. Axial strain at C, D and F are smaller for SiC interposer by 22%, 32% and 45% respectively possibly due to smaller CTE and Poisson's ratio of SiC. However, it was observed that axial strain in SiC interposer is greater towards the center and surface of Cu via than at the interface (C, D and F) compared to Si interposer.



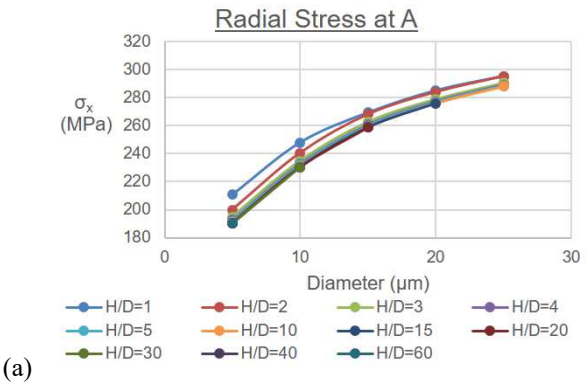
(a)



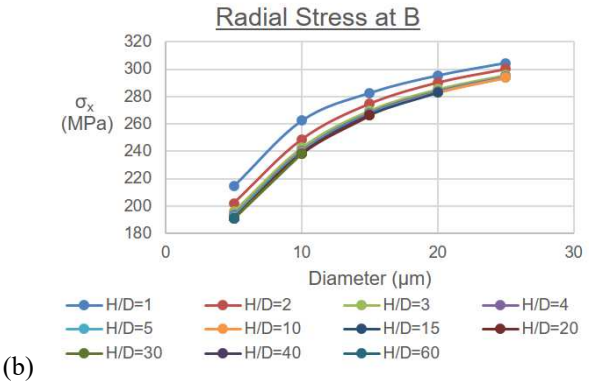
(b)

Fig. 3. Radial Stress (a) and Axial Strain (b) of Si and SiC interposer

The effect of via diameter is illustrated in Figure 4 where increasing via diameter increases radial stresses at a decreasing rate. There is a slight decrease in radial stress at A and B with higher via ratio. Via ratio has minimal effect on radial stress at E. The radial stress of SiC at E exceeds the flexural strength (415 MPa) for D>10 µm. The effect of via ratio is shown in Figure 5 where increasing via ratio generally reduces axial strains with decreasing rate. The axial strains at C and D are much lower than the elongation limits of 2% ($2x10^4$ µε) and 30% ($3x10^5$ µε). At F, the axial strains are lower but caution should be exercised considering the brittleness of SiC. There is lower axial strain for smaller via diameter at F, opposite for C and D. The close proximity of critical points to the constrained boundaries may be a possible reason for the trend reversal at D=5µm & H/D=1 for F. Figure 6 illustrates the axial strain contours of D=10 at various via ratio (deformation 50X) showing greatly reduced axial strain at mid-plane as via ratio increases.



(a)



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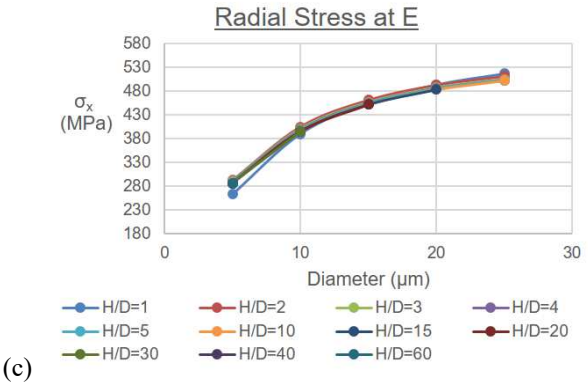
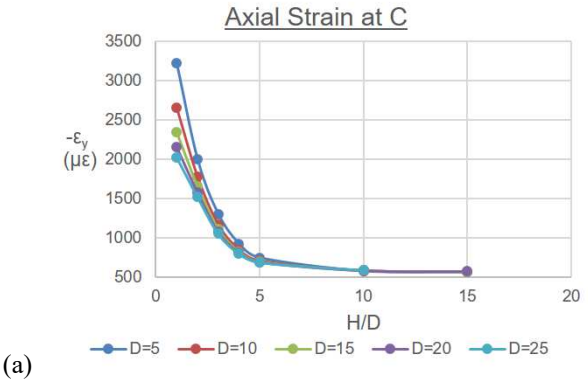
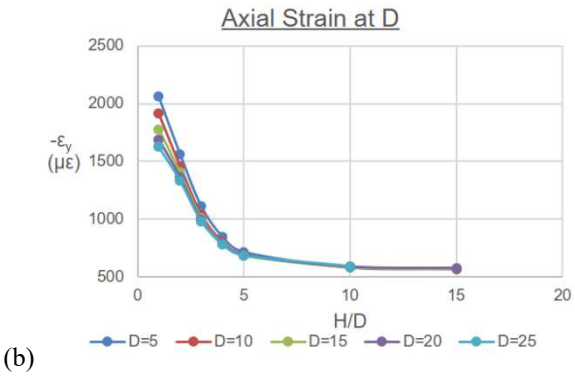


(c)

Fig. 4. Radial Stress at A (a), B (b) and E (c) for fully Cu-filled SiC interposer



(a)



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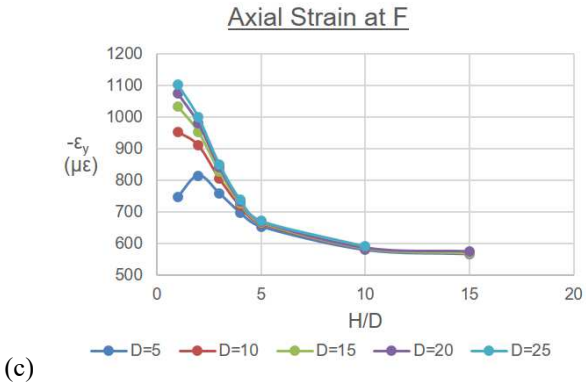


(c)

Fig. 5. Axial Strain at C (a), D (b) and F (c) for fully Cu-filled SiC interposer

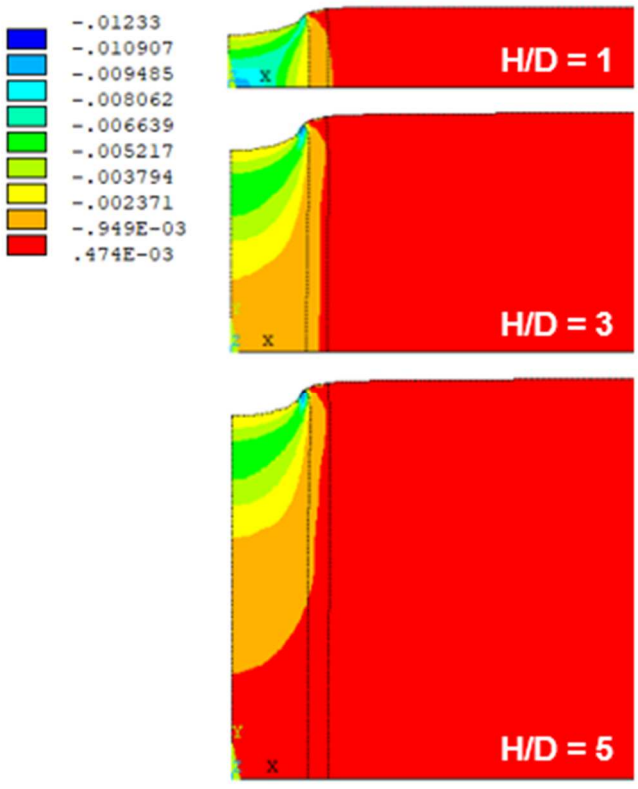


Fig. 6. Axial strain contours of D=10μm at various H/D (deformation 50X)

2.1. Partially Cu-filled through SiC via model

Partial filled via is an alternate design for reducing stress. Figure 7 shows the diagram of a partially copper-filled through SiC via and finite element model with the applied boundary conditions. The copper is plated at the side wall with 2µm thickness. The dimensions, critical points of radial stress and axial strain monitored and the assumptions were the same as those used in the fully copper-filled via model.

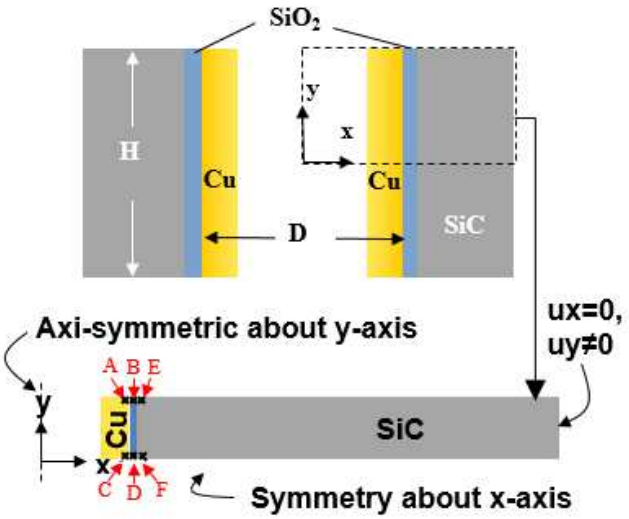
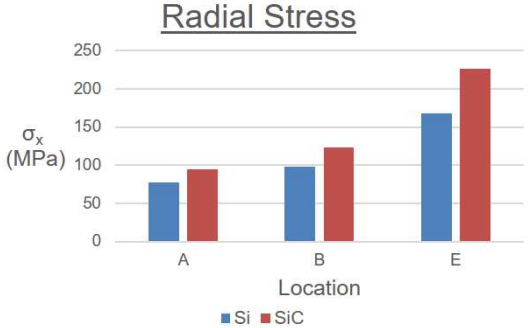


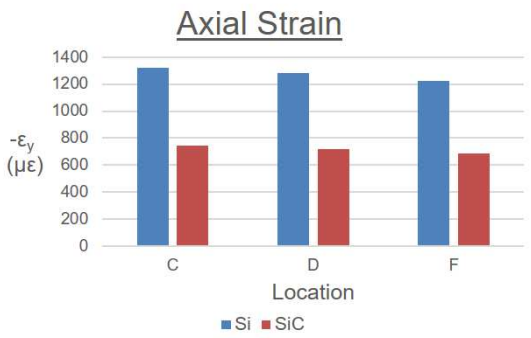
Fig. 7. Diagram of partially filled via and Finite element model

2.2. Partially Cu-filled through SiC via model results

Figure 8 compares the radial stresses and axial strains of partial Cu-filled via of Si interposer and SiC interposer (D=25µm, H/D=1). Radial stress at A, B and E are greater for SiC interposer by 22%, 25% and 35% respectively due to its higher Young's modulus and slightly larger CTE mismatch. Axial strain at C, D and F are smaller for SiC interposer by 44% likely due to smaller CTE and Poisson's ratio of SiC.



(a)

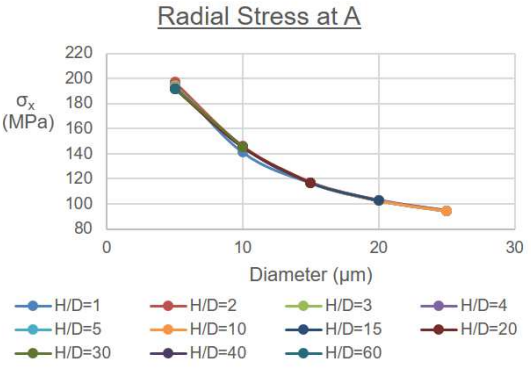


(b)

Fig. 8. Radial Stress (a) and Axial Strain (b) of partially Cu-filled Si and SiC interposer

The effect of partial-filled via diameter is shown in Figure 9 where increasing via diameter decreases radial stresses at a decreasing rate. Via ratio has negligible effect on the radial stress. Trend reversal is observed at D=5µm & H/D=1 for E. The effect of partial-filled via ratio is shown in Figure 10 where increasing via ratio decreases axial strains significantly with small via ratio and via diameter. Similar with fully-filled via, trend reversal is observed at D=5µm & H/D=1 for F. Figure 11 illustrates the copper axial strain contours of H/D=1 with increasing diameters (deformation 50X) which shows peak axial strain shifting from middle to top with greater via diameter and with less axial strain overall, due to taller height of SiC constraining the copper.

In general, compared to fully-filled via, radial stresses and axial strains are smaller for partial-filled via, but becomes close at D=5µm. Given the fixed thickness of Cu (2 µm) for all via diameters, there is smaller unfilled Cu volume in proportion for smaller diameters, hence the stress reduction is lowered.



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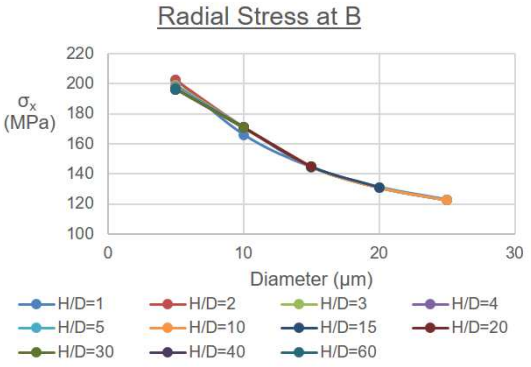

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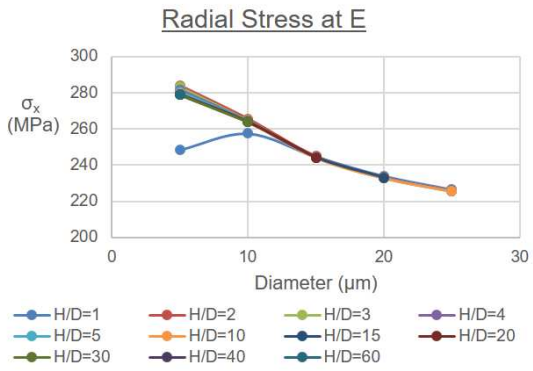
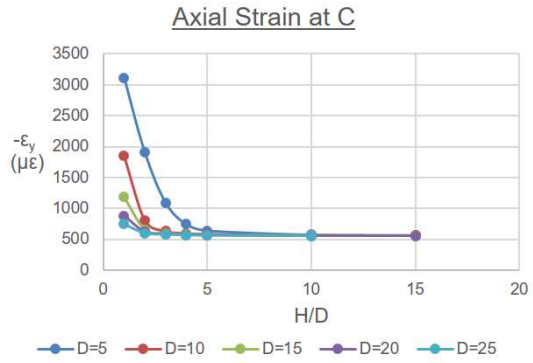
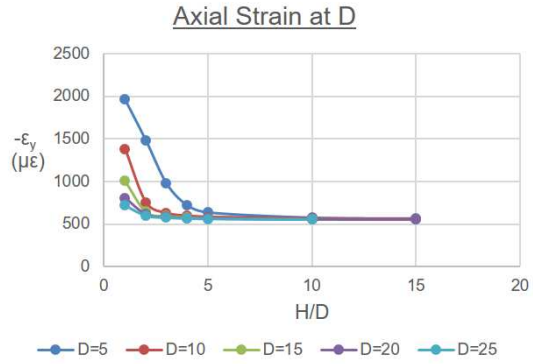


(c)

Fig. 9. Radial Stress at A (a), B (b) and E (c) for partially Cu-filled SiC interposer



(a)



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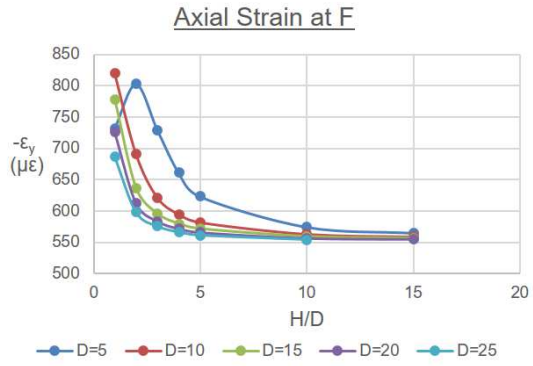

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Fig. 10. Axial Strain at C (a), D (b) and F (c) for partially Cu-filled SiC interposer

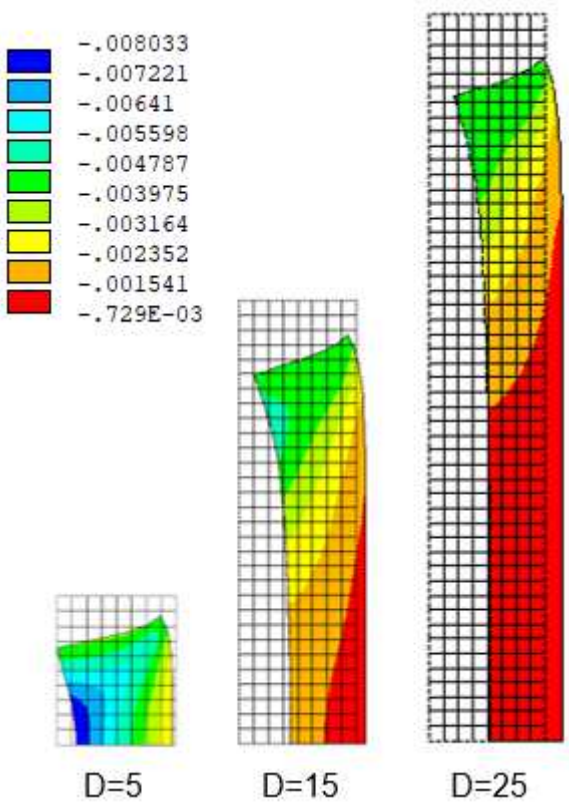


Fig. 11. Cu axial strain contours of H/D=1 at various diameters of partial-filled via (deformation 50X)

3.1. Fully Cu-filled through SiC via with Cu pad model

Figure 12 shows the diagram of a fully copper-filled through SiC via with copper pad and the finite element model with the applied boundary conditions. Copper pad thickness T is 3μm and the copper pad diameter D_P is 1.5 times the via diameter. The SiO_2 top layer thickness is the same as side layer at 1μm. The dimensions, critical points of radial stress and axial strain monitored and the assumptions are the same.

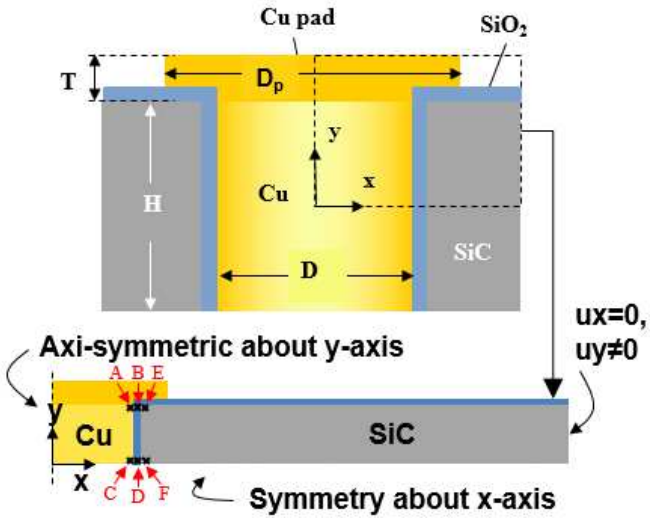
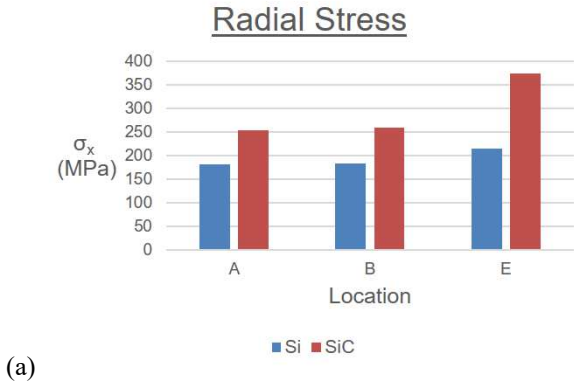


Fig. 12. Diagram of fully Cu-filled via with Cu pad and Finite element model

3.2. Fully Cu-filled through SiC via with Cu pad model results

The radial stresses and axial strains between Si interposer and SiC interposer both with copper pad (D=25µm, H/D=1) are compared in Figure 13. The SiC interposer experiences greater radial stress at A, B and E by 39%, 42% and 75% respectively due to higher Young's modulus of SiC and slightly larger CTE difference. Axial strain at C, D and F are smaller for SiC interposer by 21%, 30% and 42% respectively likely due to smaller CTE and Poisson's ratio of SiC. Similar to fully-filled via without pad, axial strain in SiC interposer is greater towards the center and surface of Cu via than at the interface (C, D and F) compared to Si interposer.

Figure 14 compares between SiC interposer with and without copper pad. With copper pad, radial stress at A, B and E decreased by 14%, 15% and 27%. The reason may be the negative radial stress observed at top of the copper pad, being further away and less strained by SiC. The axial strain at C, D and F are slightly greater with pad by 1%, 4% and 7% respectively. Since only the copper pad and top layer of SiO_2 is modeled, the results may differ when including the dielectric or polymer material used to fill the rest of the routing layer, depending on the routing pattern, dimension and material properties. However, it is expected for these materials to be much less stiff than SiC, hence reducing impact on stress and strain at the interface.



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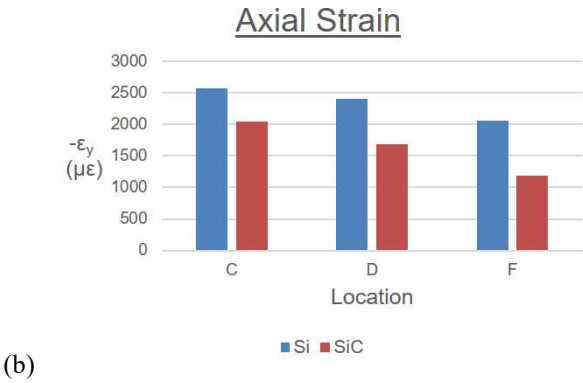
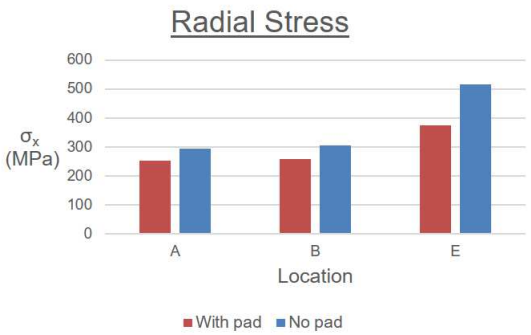
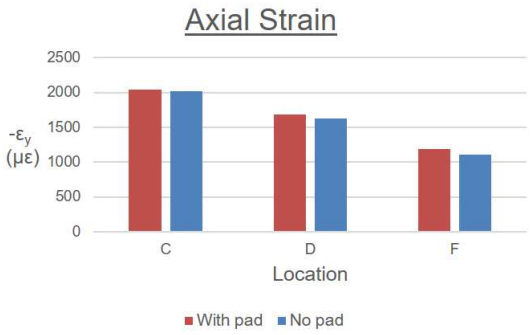


(b)

Fig. 13. Radial Stress (a) and Axial Strain (b) of Si and SiC interposer both with Cu pad



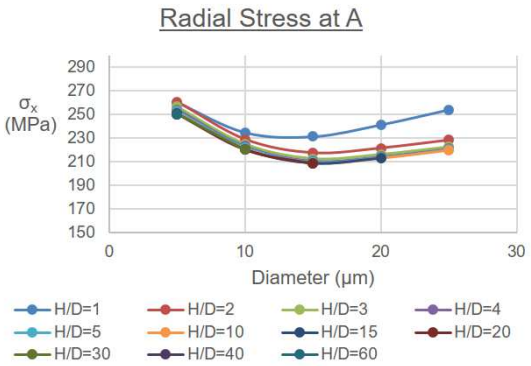
(a)



(b)

Fig. 14. Radial Stress (a) and Axial Strain (b) of SiC interposer with and without Cu pad

The effect of via diameter and via ratio on SiC interposer with copper pad is shown in Figures 15 and 16 respectively. The radial stress at A and B shows a convex trend and appears lowest at D=15µm. There is a decrease in radial stress as via ratio is increased, negligible for larger via ratios and small via diameters. For E, radial stress increases fairly linearly with increasing via diameter, with minimal impact of via ratio at higher via ratio. Axial strain C, D and F decreases with increasing via ratio at a decreasing rate. As the axial strains are at mid-plane, they are mostly minimally affected by the Cu pad at the top, with only slight differences for small via ratio (H/D=1) and small via diameter which makes the fixed Cu pad thickness (3µm) proportionally larger to affect the axial strains.



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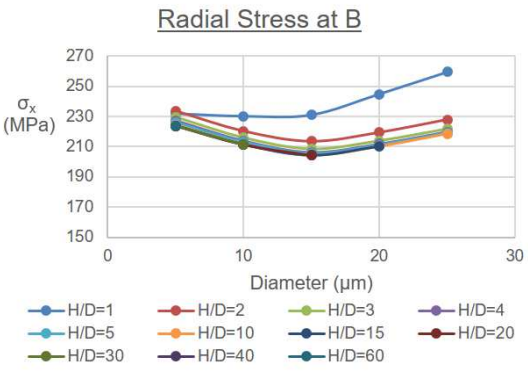

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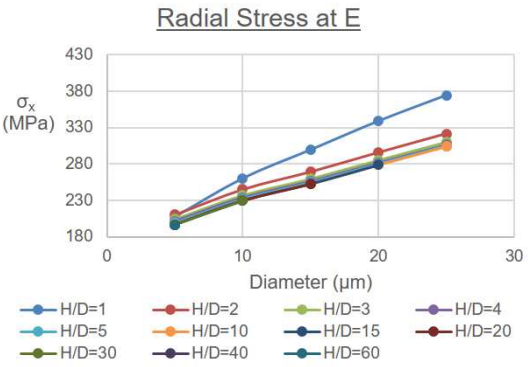
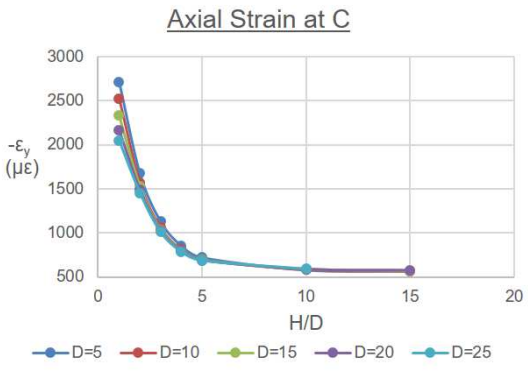


(c)

Fig. 15. Radial Stress at A (a), B (b) and E (c) for fully Cu-filled SiC interposer with Cu pad



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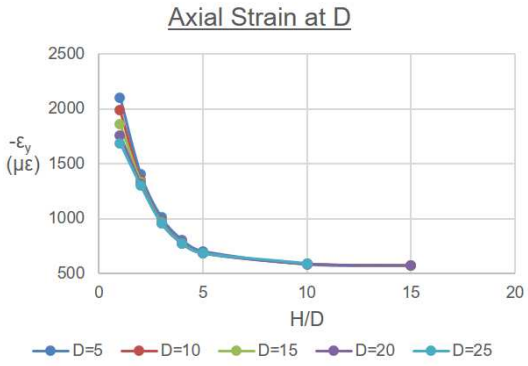

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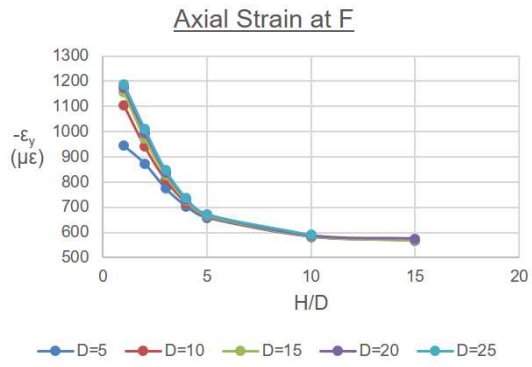

(c)

Fig. 16. Axial Strain at C (a), D (b) and F (c) for fully Cu-filled SiC interposer with Cu pad

Solder Joint Reliability

1. 3D slice model

The impact of the SiC interposer on the solder joint reliability is compared with that of Si interposer by monitoring the creep strain energy density per cycle (ΔW) of the solder bumps. The interposer is attached to the chip by 95.5Sn3.8Ag0.7Cu solder bumps with an I/O configuration of 29x29. A 3D slice model is created and Figure 17 shows a schematic of the basic geometry of the model. Figure 18 and 19 shows the finite element model with the applied boundary conditions and the mesh. 3 thermal cycles were conducted from 125 ºC to -40ºC. The heights of the interposer, solder and chip are 300, 100 and 50 μm respectively. The Garofalo-Arrhenius creep equation (1) was used to model solder creep. The constants used are included in table 2.

$$\dot{\varepsilon} = A[\sinh(B\sigma)]^n \exp(-\frac{Q}{RT}) \quad (1)$$

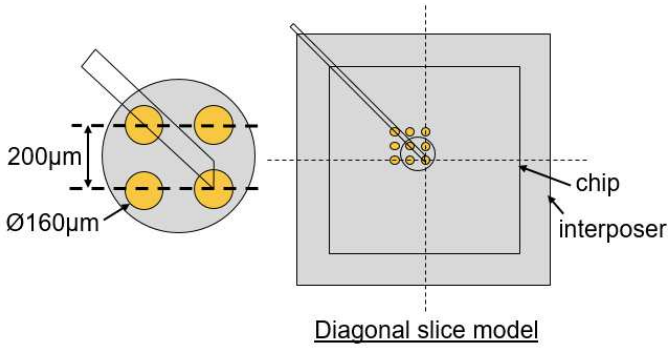

Fig. 17. Basic Geometry of Model

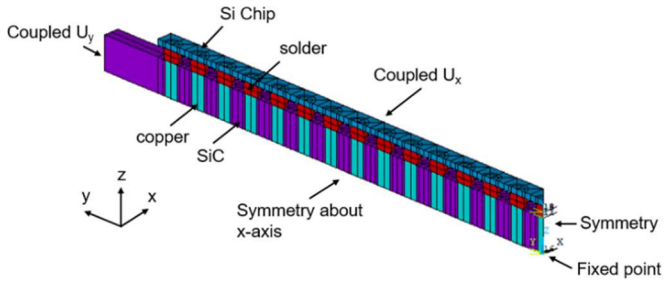

Fig. 18. Finite element model with applied boundary conditions

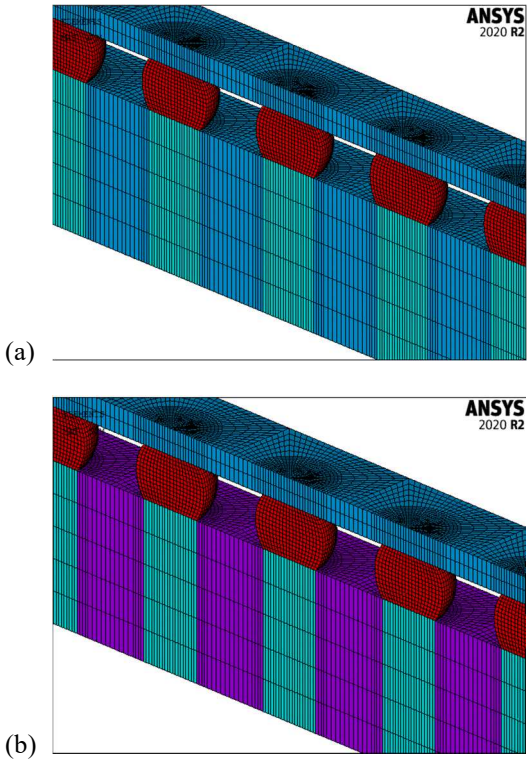

Fig. 19. Mesh of Si (a) and SiC (b) interposer

2. 3D slice model results

Modelling results have indicated that replacing Si interposer with SiC interposer results in 39% increase in maximum ΔW as shown in Figure 20. The ΔW is calculated based on the average of the 2nd and 3rd thermal cycles as the values in the 2nd and 3rd cycles are similar (i.e. stable) while the 1st cycle is much larger. The maximum ΔW occurs at the outermost solder at the bottom corner. A combination of factors such as the higher elastic modulus, greater CTE mismatch and smaller deformation with lower Poisson's ratio causing stress buildup are likely contributors to the increase in ΔW. Thus, solder joint reliability is reduced.

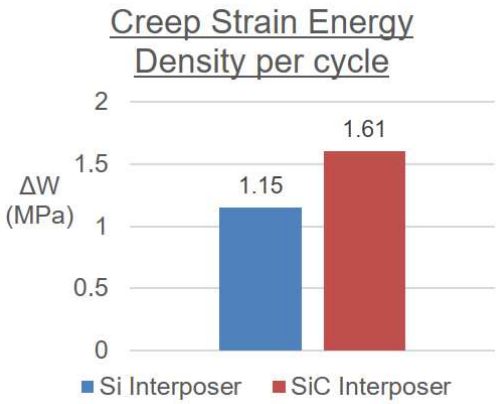

Fig. 20. Creep Strain Energy Density per cycle of Si and SiC interposer

Conclusion

Finite element analysis on single through SiC via and 3D sliced model on solder bump reliability were conducted in this paper. The findings from the modelling results are summarized below:

1. SiC interposer has higher radial stress and smaller axial strain than Si interposer at the interface.
2. Increasing via diameter increases radial stresses for fully Cu-filled via and decreases for partially Cu-filled via.
3. Increasing via ratio reduces axial strains for both fully and partially Cu-filled via.
4. Copper pad with fully Cu-filled SiC interposer decreases radial stress than without copper pad at the top interface.
5. Via diameter 10 µm and below is recommended for low radial stress and axial strain in fully Cu-filled via.
6. Replacing Si with SiC in interposer results in 39% increase in the maximum creep strain energy density per cycle in SAC solders.

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