Growth-Dominant SuperLattice-Like Medium and Its Application in Phase Change Memory

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Abstract

Ideal growth-dominant (GD) phase change material is needed for lateral Phase change memory (PCM). We propose the concept of GD superlattice-like (SLL) phase change structure. GeTe and Sb_7Te_3 were selected to form the GD SLL structure. Through detailed thin film studies, it was found that the crystallization temperature and resistivity of GeTe and Sb_7Te_3 were thickness dependent. The crystallization behavior of GeTe/Sb_7Te_3 SLL phase change structure shows a single-threshold and growth-dominant, indicating that it is an ideal candidate for lateral PCM. It was found that the crystallization and melting temperatures of GeTe/Sb_7Te_3 SLL phase change structure could be tuned by thickness ratio. The crystallization temperature of GeTe/Sb_7Te_3 SLL phase change structure increase with increasing thickness ratio of GeTe/Sb_7Te_3. GeTe/Sb_7Te_3 SLL structure built with a thickness ratio of 1.6:1 (GeTe to Sb_7Te_3) exhibited the lowest melting temperature compared to other thickness ratio. For a typical lateral PCM employing such GeTe/Sb_7Te_3 SLL phase change structure, stable SET/RESET operations with a low RESET current of 1.5mA, high programming speed of 30 nanoseconds, a good endurance above 10^5 cycles and a high RESET/SET resistance ratio window of 20 were achieved, demonstrating strong potentials in next generation non-volatile memory application.

I. INTRODUCTION

As one of the most promising candidates for the next-generation nonvolatile memory (NVM), phase change memory (PCM) has received enormous interest.[1-3] Typically, a conventional PCM adopts a vertical structure whereby the phase change material is sandwiched between two electrodes. Relying on the principle of having substantially different electrical resistances between its amorphous and crystalline states, which can be reversibly and reliably switched by electrical pulses, vertical PCM has demonstrated various attractive properties such as high speed, high endurance, long data retention and high density. [1-5] However, one major limitation that may hinder the eventual widespread application of vertical PCM perhaps lies with the relatively large RESET current required to melt the phase change material.

To solve this problem, lateral PCM with lower currents has been proposed as an alternative to its traditional vertical counterparts.[6-9] A typical lateral PCM device employs a horizontal structure in which the two electrodes are placed at each side of phase change material. Phase change materials were classified into two types: nucleation-dominant (ND) and growth-dominant (GD). ND phase change materials, such as $Ge_2Sb_2Te_5$, are mainly used for OUM[6,11] while GD phase change materials, such as doped SbTe,[6] doped GeSb[7] and doped Sb_2Te,[8] are mainly applied in lateral PCM. Compared ND phase change material, GD phase change materials provide fast growth speeds and low threshold fields. Despite having above mentioned properties, GD materials have their own weaknesses. For instance, the lower melting point, a shorter crystallization time and high programming speeds of SbTe cause data instability and the small resistivity difference between the two phases result in a small resistance ON/OFF ratio. Hence, intensive research is still ongoing to search for an ideal GD phase change material for lateral PCM. In addition to the immense effort in searching for new phase change materials with better

properties, researchers are also investigating the possible improvement in PCM performance from a structural approach, e.g. by adopting an artificial superlattice-like (SLL) structure. It has been demonstrated, both theoretically and experimentally, that SLL structure can achieve significantly lower thermal conductivities in both the in-plane and cross-plane directions.[12,13] Also, the electrical properties of SLL are found to be dependent on the periods and thickness of the constituent materials,[14,15] allowing more freedom in designing a PCM device with tailor-made performance parameters. In fact, ND SLL phase change structure consisting of alternating layers of GeTe and Sb_2Te_3 has been successfully applied in OUM and demonstrated both low power consumption and good stability.[16] The ND GeTe/Sb_2Te_3 SLL structure, however, cannot be applied directly onto a lateral PCM due to the difficulties in achieving stable amorphization or crystalization.[17]

In this article, we propose the concept of GD superlattice-like (SLL) phase change structure which is incorporated with two GD binary phase change materials. The schematic of GD SLL phase change structure is shown in Figure 1(a). Different GD phase change materials can be utilized to form the GD SLL structure and GD GeTe and Sb_7Te_3 were selected to form the GD SLL structure in this work. Detailed thin film studies of GeTe, Sb_7Te_3 and GeTe/Sb_7Te_3 SLL phase change structure were conducted. A typical lateral PCM employing such GeTe/Sb_7Te_3 SLL phase change structure was also fabricated and tested.

II. EXPERIMENT

In this work, GD GeTe and Sb_7Te_3 were selected to form the GD SLL structure. Hence, film study of individual GeTe and Sb_7Te_3 has been conducted firstly. And GeTe and Sb_7Te_3 of film thickness from 2.5 nm to 50 nm covered with 100nm SiO_2 were deposited. For all the cases, thim

film was deposited on Si wafer with 1-μm-thick thermal oxide layer using Balzers DC magnetron sputtering system with a base pressure of 10^{-6} mbar and a working pressure of 10^{-3} mbar. All the thin films were deposited at room tempreature. The crystallization behavior of these samples were investigated with an exothermal resistance measurement (ETTM).

Also, GeTe/Sb_7Te_3 SLL structure was achieved by alternating the deposition of the GeTe and Sb_7Te_3 repeatedly. The thickness of each layer was determined as the product of the sputtering rate and the sputtering duration, while the number of periods (one period consists of one GeTe layer and one Sb_7Te_3 layer) was controlled by the number of cycles of the alternation. To allow a comprehensive study of the SLL phase change structure, the thickness ratio of GeTe and Sb_7Te_3 was varied from 1:1, 1.4:1, 1.6:1, 2:1, 3:1, and 4:1, respectively. The thickness (i.e. GeTe + Sb_7Te_3) of each period and the number of the periods were fixed to be 12.5 nm and 4, respectively, for meaningful comparison. In other words, the total thickness of the entire SLL structure was kept at 50 nm covered with 100 nm SiO_2. A typical GeTe/Sb_7Te_3 SLL fabricated in this work is shown in Figure 1(b). In this case, the GeTe/Sb_7Te_3 consists of 4 periods, with each period having a GeTe layer of ~8.3 nm and a Sb_7Te_3 layer of ~4.2 nm. A phase change temperature tester based on the phase change film reflectivity was employed to investigate the crystallization and melting behavior.

For lateral PCM devices with the GeTe/Sb_7Te_3 SLL phase change structure(Figure 1(c)), titanium tungsten (TiW) electrodes of 100 nm thickness and with a separation distance of 0.5 μm were first deposited. This was followed by the formation of the GeTe/Sb_7Te_3 SLL with the above mentioned approach, but with the final step which involved the depostion of a 200-nm-thick ZnS-SiO_2 as a protective layer to prevent the possible ambient oxidation of the underlying SLL structure. The fabricated lateral PCM devices were tested with self-built PCM tester.

III. RESULTS AND DISCUSSION

a) Individual crystallization behavior of homogeneous GeTe and Sb_7Te_3 films

As the crystallization temperature of a phase change material is highly dependent on the film thickness, detailed investigations on the crystallization behavior of the respective individual homogeneous GeTe and Sb_7Te_3 films of thickness ranging from 2.5 nm to 50 nm were first carried out using an exothermal resistance measurement(ETTM) at a constant heating rate of 5 ^oC/min. The values of electrical resistance versus temperature are presented in Figure 2. As the temperature increases, the resistance will decrease for all the films. The gradual decrease of resistance can be attributed to the temperature-dependent ionization in the semiconductor material.[18] At the crystallization temperature (T_x), a sharp drop in resistance is generally observed. The abrupt resistance decline is due to the rearrangement of atomic structures. As shown in Figure 2, both GeTe and Sb_7Te_3 show a single-threshold behavior, indicating that both of them have only one crystallization state which makes them an ideal candidate for lateral PCM.[6] It can be seen that both materials display similar trends of having higher T_x for smaller thicknesses. Such observation of higher T_x with decreasing film thickness has also been reported in $Ge_2Sb_2Te_5$ measurements.[19] At a film thickness of 2.5 nm, both GeTe and Sb_7Te_3 show negligible change in resistivity even at a high temperature of 320 ^oC. This indicates the absence of phase transition and implies that the critical thickness is thinner than 5nm and thicker than 2.5nm. Below the critical thickness, no phase change can be induced for GeTe and Sb_7Te_3 film sandwiched by SiO_2. The absence of phase change is that the effective interface energy for the film below critical thickness is too high to maintain a stable nucleus for the crystallization to occur.[20] Such critical thickness for phase transition is in fact not uncommon and has been reported previously. For instance, Raoux reported that 3.6 nm is the size limitation of $Ge_2Sb_2Te_5$ thin films capped by Al_2O_3.[21]

Upon close examination, it can be seen from Figure 2(a) that the resistivity of GeTe at both the amorphous and the crystalline states remains fairly similar for different film thicknesses, as indicated by the almost overlapping curves at the two states. The resistivity of Sb_7Te_3, on the other hand, increases with the decrease in film thickness at both states. Such increase in the resistivity with decreasing film thickness is especially prominent at the crystalline state for the single homogeneous Sb_7Te_3 film (Figure 2(b)). This, coupled with the fact that Sb_7Te_3 having a lower resistivity in the amorphous state as compare to GeTe, would mean that the resistivity differences of Sb_7Te_3 between the amorphous state and crystalline state at decreasing film thickness would be increasingly smaller as compared to those of GeTe. As shown in Figure 2(c), the resistivity ratio of GeTe is around 10^4 at a thickness of 50 nm while that of SbTe at the same thickness is 10^3. At 5-nm-thickness, the resistivity ratio remains at approximately 10^4 for GeTe but has decreased to only 10^2 for Sb_7Te_3. The different resistivity ratios for GeTe and Sb_7Te_3 in this case are beneficial for SLL application in lateral PCM as it can allow more freedom in designing the overall ON/OFF of the memory device. If higher ON/OFF resistance of the memory device is needed, the SLL structure can be incorporated with thinner GeTe and thicker Sb_7Te_3. If lower ON/OFF resistance of the memory device is needed, the SLL structure can be incorporated with thicker GeTe and thinner Sb_7Te_3.

Figure 3 summarizes the dependence of the T_x of both GeTe and Sb_7Te_3 on the film thickness. It can be seen that T_x of both GeTe and Sb_7Te_3 in general gives an increasing trend with decreasing film thickness. In particular, while the small increments in T_x are observed for relative thick films (> 10 nm), the changes in the T_x are much more prominent at thickness below 10 nm for both GeTe and Sb_7Te_3 as evident by the much stepper slopes of the two curves. Also, at each thickness, the T_x of GeTe is higher than that of Sb_7Te_3. The difference in T_x, however,

gradually becomes smaller as the thickness decreases. For example, the gap between the two T_x is about 40 ^oC at a film thickness of 50 nm, and it decreases to approximately 35 ^oC at 5 nm.

b) Growth-dominant SLL structure properties

The crystallization temperature (T_x) and melting temperatures (T_m) of the SLL structures are important since they have strong influences on the SET speed and RESET currents respectively. To measure the T_x and T_m of GeTe/Sb_7Te_3SLL structure, a phase change temperature tester based on the phase change film reflectivity was employed. The basic mechanism is to heat up the sample in a vacuum chamber. A laser beam is directed onto the surface of the sample and the reflected laser is detected by a sensor. When the sample crystallizes (or melts), the reflectivity of phase change material will increase (or decrease) abruptly and this produces a corresponding increase (or decrease) in the measured reflected signal at the same time. Figure 4(a) shows reflected laser signal at different temperature for SLL at a thickness ratio (GeTe to Sb_7Te_3) of 2.0 at a constant heating rate of 30^oC/min. The corresponding T_x and T_m in this case are 155^oC and 551^oC respectively. It can be observed that the crystallization behavior of GeTe/Sb_7Te_3SLL structure is GD as the signal changed abruptly when T_x was met.

Using the same measurement, the crystallization and melting temperatures of the GeTe/Sb_7Te_3 SLL of other thickness ratios were obtained and plotted in Figure 4(b). As depicted in Figure 4(b), the crystallization temperature first increases gently from 153^oC to 159^oC with increasing thickness ratio from 1.0 to 3.0 before the sudden increase to 185^oC at the corresponding thickness ratio of 4.0. As higher crystallization temperature leads to better data retention[22], thickness ratio of GeTe/Sb_7Te_3 SLL had better to be selected above 3.0 to achieve longer data retention time. Interestingly, as compared to the monotonous increasing trend of the crystallization temperature, the melting temperature exhibits a local minimum of 535^oC at the

thickness ratio of 1.6. The melting temperature is of particular interest here since it determines the RESET current. Not surprisingly, a corresponding lowest RESET current of 1.5 mA is observed for the GeTe/Sb_7Te_3 SLL phase change structure with a thickness ratio of 1.6 as compared to other thickness ratio (Figure 5).

c) Growth-dominant SLL application in lateral PCM

Since the GeTe/Sb_7Te_3 SLL phase change structure with a thickness ratio of 1.6 produces the lowest RESET current, it was employed in our lateral PCM devices for further investigation. Figure 6 shows the I-V curves of GeTe/Sb_7Te_3 SLL lateral PCM obtained by a DC current sweep. In this case, the SLL lateral PCM demonstrates a resistance value of 800 kΩ at the amorphous state. The switching current from amorphous state to crystalline state, which gives a resistance of 10 kΩ, is only 12 μA (static "SET").

Figure 7 shows the typical U-shaped SET and S-shaped RESET curves for our GeTe/Sb_7Te_3 SLL lateral PCM obtained using square pulses. The pulse width (i.e. the SET speed) in this case is 30 nanoseconds, which is faster than the previous reported values[6] even though our cell size is 20 times larger. The fast switching speed may be attributed to the fact that both GeTe and Sb_7Te_3 have very fast crystallization speeds. The SET and RESET current are 1.0 mA and 1.5 mA, respectively. Compared with other published results, it was found that our lateral PCM with the proposed SLL structure show comparable RESET current despite the much larger cell size.[6, 7] The possible reason for the low RESET current is that the phase change medium with SLL structure possesses lower thermal conductivity and T_m for the phase change material. In other words, less power is needed to achieve the lower T_m due to the more efficient heating. As mentioned in the earlier section, a clear advantage of our GeTe/Sb_7Te_3 SLL structure is that it allows precise tuning of the resistivity ratio (through the thickness of the constituent layers) and

thus a possible control over RESET current. While our current results indicates that a thickness ratio of 1.6 gives the optimal RESET current and endurance, further investigation (with a larger ratio range with finer steps, other total film thickness and/or different periods) may yield even lower RESET currents. The energy for the RESET process is much higher than that for SET process, which is possibly caused by entropy effect[23].

It is important to note that, unlike the lateral PCM with ND GeTe/Sb_2Te_3 SLL structure, all our GD GeTe/Sb_7Te_3 SLL lateral PCM devices across the whole wafer show stable SET/RESET operations with an endurance above 10^5 and a consistent On/OFF ratio of close to 20 (Figure 8). The stable operation may be attributed to the intrinsic material properties of the carefully chosen GD GeTe and Sb_7Te_3. On the other hand, an overall GD characteristic of the GeTe/Sb_7Te_3 SLL structure making it suitable for stable lateral PCM operation.

IV. CONCLUSION

In conclusion, the concept of GD superlattice-like (SLL) phase change structure incorporated with two GD binary phase change materials was proposed and realized by incorporation of GD GeTe and Sb_7Te_3. Through detailed thin film studies, it was found that the crystallization temperature and resistivity of GeTe and Sb_7Te_3 were thickness dependent. No phase change was observed when film thickness is less than 2.5nm. Both the crystallization and melting temperatures of GeTe/Sb_7Te_3 SLL phase change structure were measured. The crystallization behavior of GeTe/Sb_7Te_3 SLL phase change structure shows a single-threshold and growth-dominant, indicating that it is an ideal candidate for lateral PCM. It was found that the T_x and T_m of GeTe/Sb_7Te_3 SLL phase change structure could be tuned by thickness ratio. The crystallization temperature of GeTe/Sb_7Te_3 SLL phase change structure increase with increasing thickness ratio of GeTe/Sb_7Te_3. GeTe/Sb_7Te_3 SLL structure built with a thickness ratio of 1.6:1

(GeTe to Sb_7Te_3) exhibited the lowest melting temperature 535 ^oC compared to other thickness ratio. By incorporating the GeTe/Sb_7Te_3 SLL phase change structure of the abovementioned optimal ratio thickness into a lateral PCM, stable SET/RESET behavior was demonstrated. The stable operations may be explained by the overall growth-dominant characteristics of the SLL structure. The low RESET current of 1.5 mA and fast SET pulse with of 30 ns, which is on-par with other published results even though our cell was significantly larger by 20 times, and the reliable endurance above 10^6 cycles with a consistent ON/OFF ratio of 20 demonstrated by the SLL lateral PCM also suggest strong potentials for next generation non-volatile memory.

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Figure captions

Figure 1 (a) Schematic of GD SLL phase change structure. (b)TEM image of a typical $GeTe/Sb_7Te_3$ SLL structure. (c) Schematic of the lateral PCM with the $GeTe/Sb_7Te_3$ SLL structure.

Figure 2 Temperature dependent resistivity of as-deposited phase-change film compositions of (a) GeTe films of various thicknesses. (b) Sb_7Te_3 films of various thicknesses. (c) GeTe and Sb_7Te_3 for thicknesses of 50 nm and 5 nm, respectively. An exothermal resistance measurement (ETTM) at a constant heating rate of 5 ^{o}C/min

Figure 3 Dependence of crystallization temperature for GeTe and Sb_7Te_3 on different film thickness, ranging from 5 nm to 50 nm.

Figure 4 (a) Measurement reflectivity of SLL at thickness ratio 2.0 dependent on temperature (b) Measured c crystallization and melting temperature of SLL varying on thickness ratio

Figure 5 RESET current of a lateral PCM with GD SLL varying on thickness ratio

Figure 6 I-V curve of lateral PCM with GD SLL at thickness ratio 1.6

Figure 7 RESET and SET R-I curve of lateral PCM with GD SLL at thickness ratio 1.6

Figure 8 Typical endurance performance of lateral PCM with GD SLL at thickness ratio 1.6

Figure 1

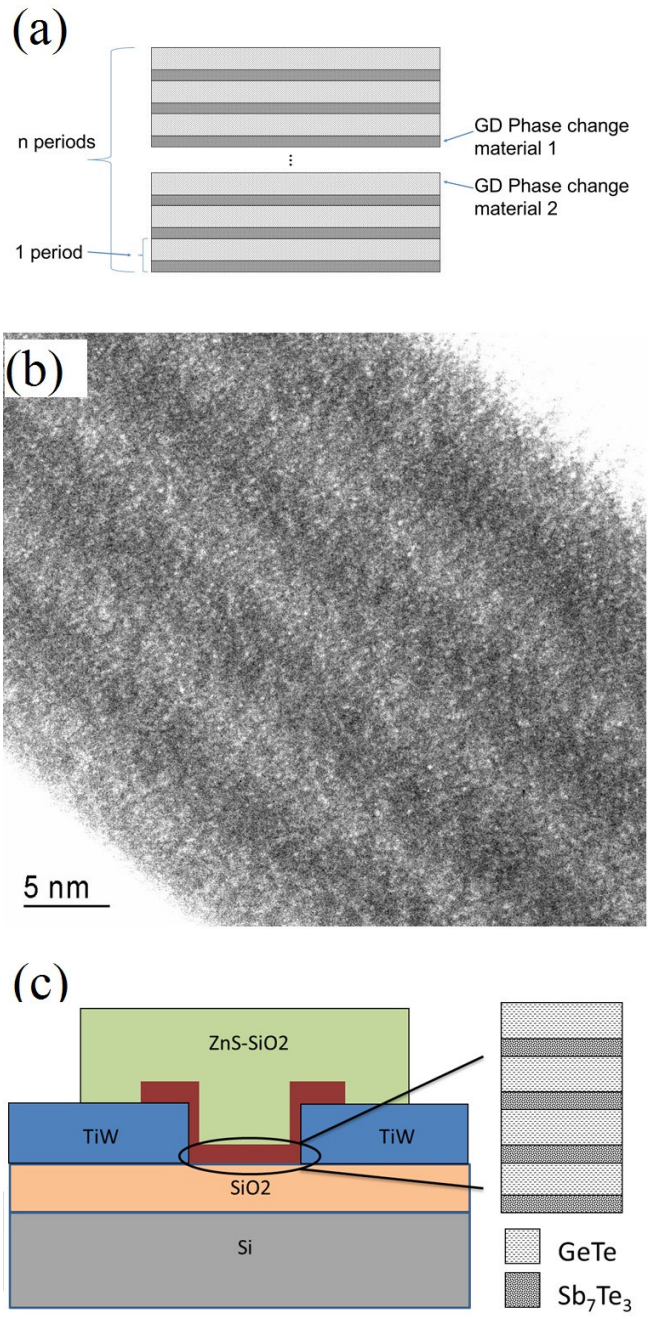

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Figure 2

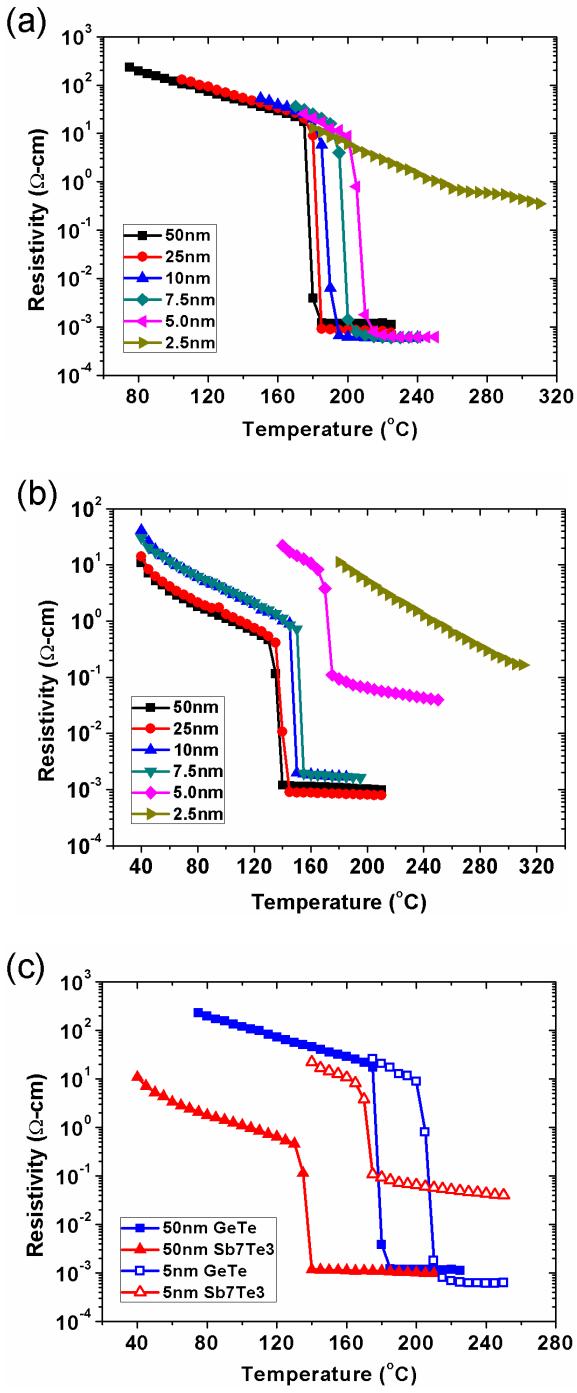

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Figure 3

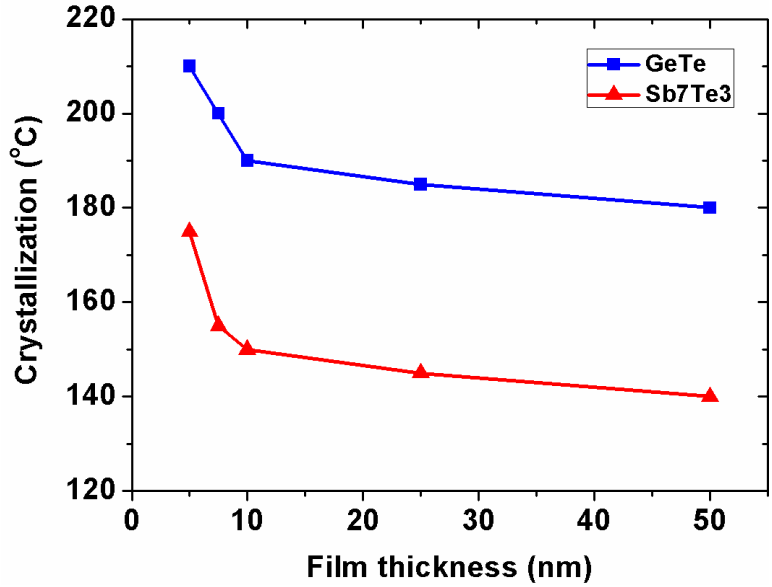

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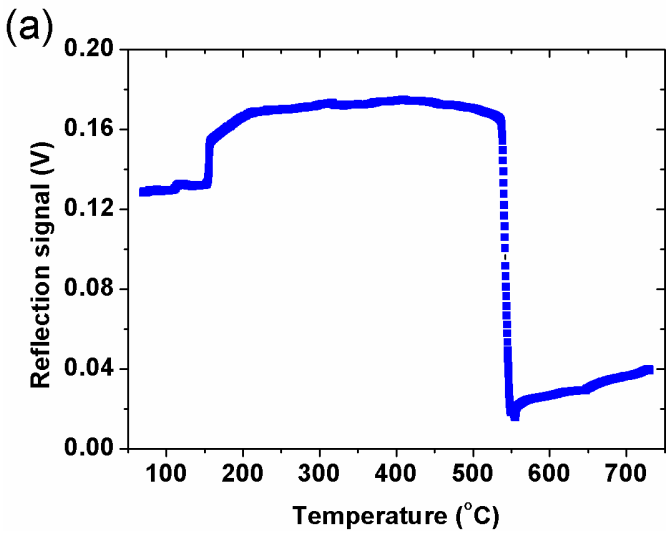
Figure 4



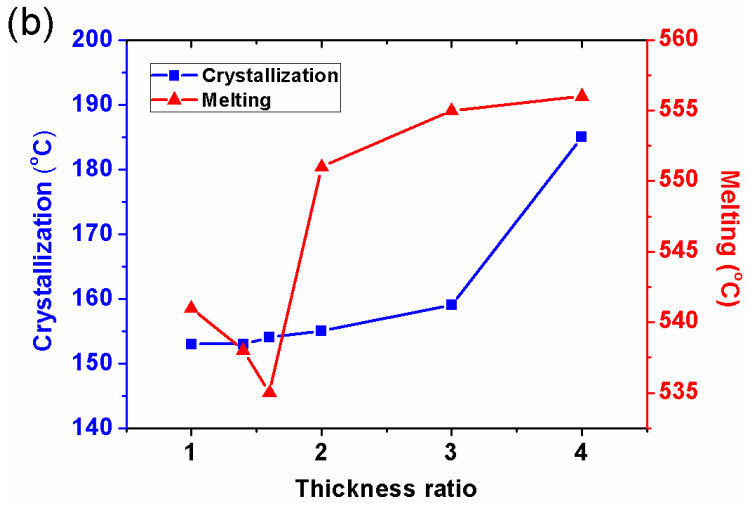


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Figure 5

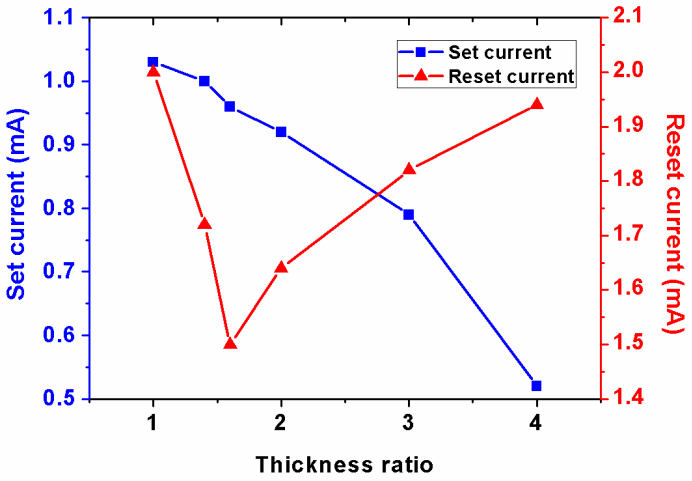

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Figure 6

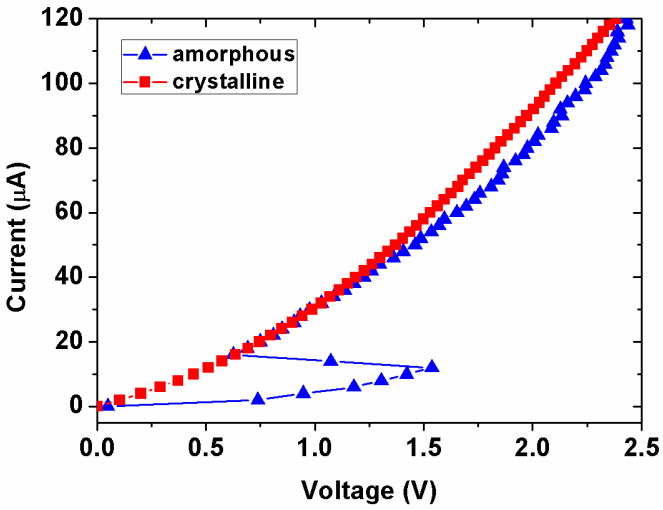

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Figure 7

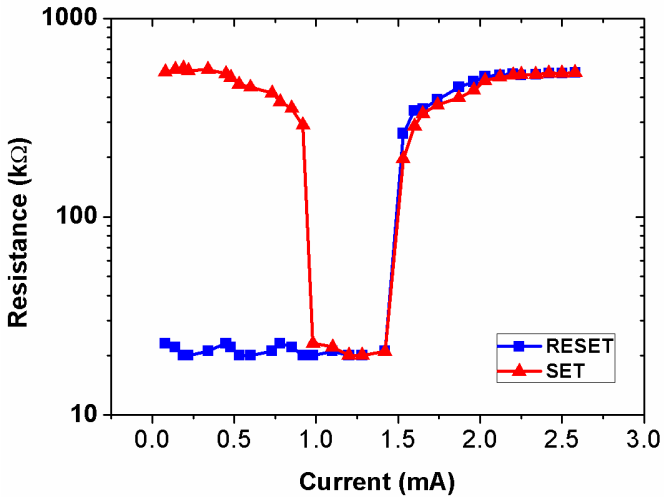

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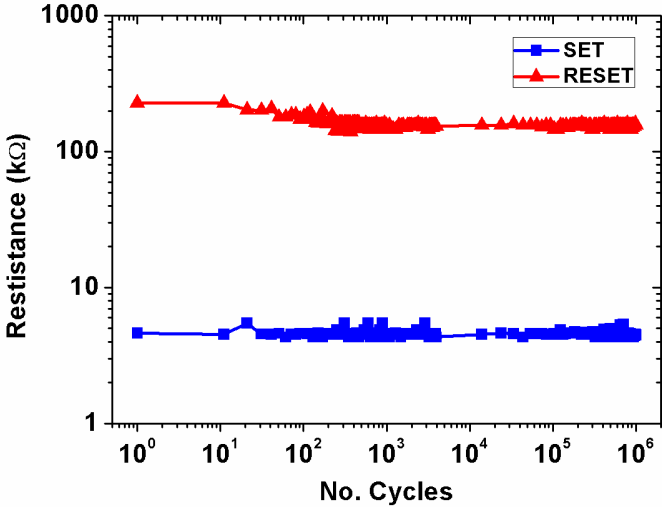
Figure 8



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