Designs of Silicon Metal-Insulator-Semiconductor Phase Modulator with a Deposited AlN Film as the Gate Dielectric

Shiyang Zhu and Guo-Qiang Lo
*Institute of Microelectronics, A*STAR, 11 Science Park Road, Science Park-II, 117685, Singapore*

***Abstract* — We propose and analyze a silicon metal-insulator-semiconductor phase modulator based on a poly-Si/AlN/Si horizontal slot waveguide. The AlN gate dielectric exhibits an inherent Pockels effect, which can provide additional phase modulation besides that provided by the free-carrier plasma dispersion effect of Si. The proposed modulator with an optimized geometry offers a high modulation efficiency of 0.95 V·cm for the 1.55-μm transverse magnetic (TM) light even the electro-optical coefficient of AlN (r_{33}) is only 1 pm/V, which is ~40% better than the SiO_2 counterpart with the same equivalent oxide thickness. The modulation efficiency increases quickly with r_{33} increasing, reaching 0.2 V·cm when r_{33} is 10 pm/V.**

***Index Terms* — Waveguide modulators, electro-optic materials, integrated optics devices, CMOS compatibility.**

I. INTRODUCTION

Silicon metal-oxide-semiconductor (MOS) modulator has been well-developed since 2004 [1-6]. Its modulation efficiency can be improved by thinning down its gate oxide thickness but at the expense of reduced modulation speed. Moreover, the thinnest oxide thickness is limited by its breakdown electric field (E_b). Thus, improving the modulation efficiency without scarifying the other performance metrics remains an open challenge for Si MOS modulators. Meanwhile, alternative Si modulators are also developed, e.g., employing an electro-optic (EO) polymer with a large EO coefficient of ~60–700 pm/V as the active material [7]. A common issue for these EO modulators is complementary MOS (CMOS) compatibility.

Recently, deposited AlN is emerging as an alternative waveguide material in integrated photonics because of its transparency over broad wavelength spectrum [8-9]. AlN is commonly used as a functional material for sensing or actuating purpose in micro-electromechanical system due to its large piezoelectric effect [10] and also used as a high-dielectric-constant (high-κ) material in microelectronics due to its excellent dielectric properties such as $\kappa \sim 10$ and $E_b \sim$ 2-3 MV/cm [11-13]. Moreover, AlN deposited on SiO_2 offers a second-order nonlinearity (χ^2) of ~4.7 pm/V and a linear EO coefficient (r_{33}, r_{13}) of ~1 pm/V, thus enabling to realize active functionalities such as second harmonic generation [14] and EO modulation [9]. However, the demonstrated AlN EO modulator has a low modulation efficiency and requires a very large driving voltage because its two electrodes are placed far from the AlN core to avoid disturbing the optical mode [9].

Here, we propose a Si metal-insulator-semiconductor (MIS) modulator using a deposited AlN as the gate dielectric between Si and solid-phase-crystallized polycrystalline Si (poly-Si) layers. The Pockels effect of AlN provides additional modulation besides that provided by the free-carrier plasma-dispersion effect of Si/poly-Si. Since the voltage applied between the Si and poly-Si layers is mostly dropped across the AlN layer, the Pockels effect induced modulation is very effective. Moreover, since AlN deposition has been developed as a mature technology and the deposited AlN film is thermally and chemically stable [11-13], the proposed modulator is CMOS-compatible and can be fabricated as the conventional Si MOS modulators.

II. MODULATOR DESIGNS

Two typical configurations for state-of-the-art Si MOS modulators are considered [2,6], as shown in Fig. 1 schematically. Here, the gate dielectric sandwiched between the Si and poly-Si layers is a thin deposited AlN layer. The whole structure is embedded in a thick SiO_2 cladding layer. The refractive indices of Si, poly-Si, AlN, and SiO_2 are set as: $n_{Si} = n_{poly\text{-}Si} = 3.45$, $n_{AlN} = 2.0$, and $n_{SiO2} = 1.44$, respectively. Since n_{AlN} is much smaller than n_{Si}, the structure actually forms a poly-Si/AlN/Si horizontal slot waveguide.

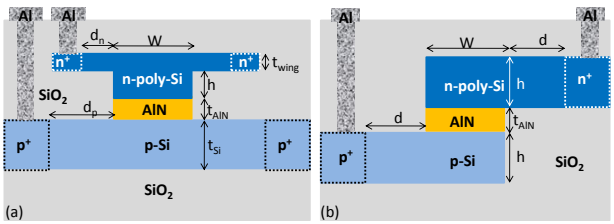

Fig. 1. Schematic cross-sectional views of two typical Si MOS capacitor phase modulators: (a) a design reported by Intel [2] and (b) a design reported by Lightwire [6].

The effective mode index (n_{eff}) of the slot waveguides is calculated using the eigenmode expansion (EME) method. Fig. 2 shows the calculated electric field intensity distributions in these two structures for the transverse electric (TE) and transverse magnetic (TM) modes at 1550 nm. For the type-1 modulator shown in Fig. 1(a), we set the Si thickness (t_{Si}) to 220 nm, the poly-Si rib height (h) to 100 nm, the thickness of the poly-Si wing (t_{wing}) to 100 nm, the AlN thickness (t_{AlN}) to 50 nm, and the poly-Si rib width (W) to 500 nm. For the type-2 modulator shown in Fig. 1(b), we set W = 600 nm, t_{AlN} = 50 nm, and the Si and poly-Si layers having the same thickness of h = 175 nm. The influences of the n- and p-dopants in the Si and poly-Si layers, the highly doped regions for contacts, and the absorption/scattering in the Si, poly-Si, and AlN layers are neglected at first for simplicity. They will be considered later to estimate the insertion loss. Due to the Pockels effect, n_{AlN} changes linearly with an electric field applied on the AlN layer, which in turn changes n_{eff}. Fig. 2(e) shows that n_{eff} depends on n_{AlN} almost linearly. The $\Delta n_{eff}/\Delta n_{AlN}$ value is an indicator of the modulation efficiency induced by the Pockels effect of AlN. Since the TM mode has much larger $\Delta n_{eff}/\Delta n_{AlN}$ than the TE mode, the proposed modulator is valid only for the TM mode.

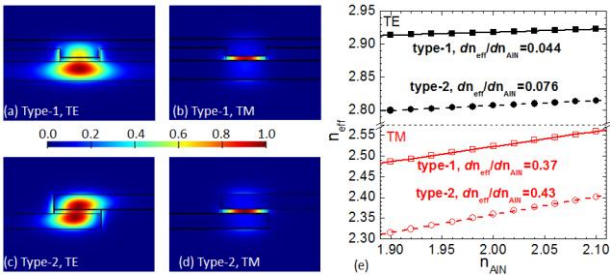

Fig. 2. Calculated electric field distributions for the TE and TM modes at 1550 nm in these two modulators: (a) type-1, TE, (b) type-1, TM, (c) type-2, TE, and (d) type-2, TM. (e) Effective mode index (n_{eff}) as a function of the AlN refractive index (n_{AlN}).

For the type-1 modulator, we fix t_{Si} = 220 nm, which is the typical thickness for a single-mode Si channel waveguide. The poly-Si wing is necessary to reduce the contact-induced optical loss [2]. Here, we fix t_{wing} = 100 nm. The other three structural parameters of t_{AlN}, h, and W are optimized. We first scan t_{AlN} from 20 to 100 nm with different W and h values. The results are plotted in Fig. 3(a). One sees $\Delta n_{eff}/\Delta n_{AlN}$ reaches maximum at a certain t_{AlN}, at which the ratio of the optical intensity contained in the $W \times t_{AlN}$ AlN slot is also maximized, as shown in Fig. 3(b). The electric field strength (E) in AlN under voltage (V) depends on t_{AlN} as $E = (V - V_{FB})/t_{AlN}$, where V_{FB} is the flat-band voltage. The values of $\Delta n_{eff}/\Delta V$ are also plotted in Fig. 3(a). One sees they decrease monotonously with t_{AlN} increasing. It indicates that the modulator with thinner t_{AlN} can provide higher modulation efficiency, the same as the conventional Si MOS modulators. However, E increases with t_{AlN} decreasing. In real applications, E is usually set to be much smaller than E_b to ensure sufficient reliability. Since E_b = ~2-3 MV/cm for the AlN film deposited on Si [11-13], E is set to 1 MV/cm here and the driving voltage swing ($V - V_{FB}$) is set to 5 V accordingly, then an optimal t_{AlN} is chosen to 50 nm.

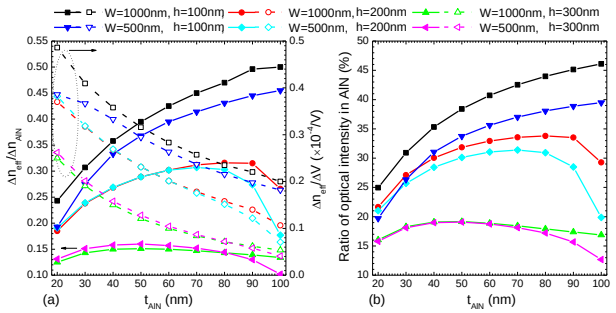

Fig. 3. Type-1 modulator: (a) $\Delta n_{eff}/\Delta n_{AlN}$ and $\Delta n_{eff}/\Delta V$ and (b) ratio of optical intensity contained in the $W \times t_{AlN}$ AlN slot as a function of t_{AlN} for modulators with different W and h values.

In order to optimize W and h, we scan W from 200 to 1000 nm with h = 100 nm and scan h from 60 to 3000 nm with W = 500 nm. The results are plotted in Fig. 4. Since $\Delta n_{eff}/\Delta n_{AlN}$ and $\Delta n_{eff}/\Delta V$ have the same trend at a fixed t_{AlN}, only $\Delta n_{eff}/\Delta n_{AlN}$ values are shown. From Fig. 4(a), one sees that $\Delta n_{eff}/\Delta n_{AlN}$ increases with W increasing quickly at first and then approaches to saturation when W is larger than ~500 nm. On the other hand, in the view point of the modulation speed, a smaller W is better because it leads to a smaller capacitance. Therefore, the optimal W is chosen to be 500 nm. From Fig. 4(b), one sees that $\Delta n_{eff}/\Delta n_{AlN}$ reaches maximum at h ~ 100 nm, indicating this is the optimal h value. Overall, the type-1 modulator may have the optimal geometry as t_{AlN} = 50 nm, W = 500 nm, and h = 100 nm. It gives $\Delta n_{eff}/\Delta n_{AlN}$ = 0.368 and $\Delta n_{eff}/\Delta V = 2.94 \times 10^{-5}$ /V.

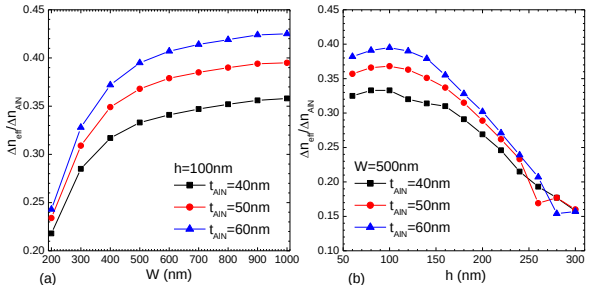

Fig. 4. Type-1 modulator: (a) $\Delta n_{eff}/\Delta n_{AlN}$ in dependence of W, and (b) $\Delta n_{eff}/\Delta n_{AlN}$ in dependence of h.

For the type-2 modulator, we set the Si and poly-Si layers to have the same thickness (h) to make the TM mode being centered along the slotted AlN layer. The dependence of $\Delta n_{eff}/\Delta n_{AlN}$ on the structural parameters of t_{AlN}, h, and W are calculated and the results are plotted in Fig. 5. Similar to the type-1 modulator, $\Delta n_{eff}/\Delta n_{AlN}$ reaches maximum at a certain t_{AlN} whereas $\Delta n_{eff}/\Delta V$ decreases monotonously with t_{AlN} increasing. When we set $V - V_{FB}$ = 5 V and E = 1 MV/cm as the type-1 modulator, the optimal t_{AlN} is 50 nm. From Fig. 5(b), one sees that the maximum $\Delta n_{eff}/\Delta n_{AlN}$ reaches to ~0.43 at the condition of W = 600–800 nm and h = 150–175 nm. Since the type-2 modulator provides larger maximum $\Delta n_{eff}/\Delta n_{AlN}$ than the type-1 modulator with the same t_{AlN}, the type-2 modulator is therefore chosen for further investigation.

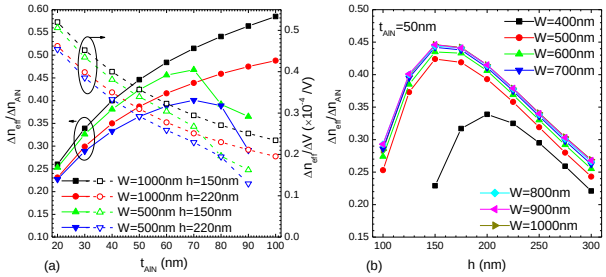

Fig. 5. Type-2 modulator: (a) $\Delta n_{eff}/\Delta n_{AlN}$ and $\Delta n_{eff}/\Delta V$ in dependence of t_{AlN} and (b) $\Delta n_{eff}/\Delta n_{AlN}$ in dependence of h with W ranging from 400 to 1000 nm.

Another structural parameter of the modulator is the distance (d) between the waveguide ridge and the highly doped region for Ohmic contact, as shown in Fig. 1. A smaller d leads to a smaller resistance (hence a higher speed) but probably a larger propagation loss due to optical absorption in the highly doped region. Assuming both the n- and p-type doping concentrations for Ohmic contact is 1×10^{20} cm^{-3}, the contact-induced propagation losses for the type-2 modulators with different dimensions of $W\times h$ (t_{AlN} = 50 nm) are plotted in Fig. 6 as a function of d. As expected, the propagation loss decreases quickly with d increasing. However, the decreasing slope depends on both W and h significantly due to the different optical mode distributions in the different-dimension waveguides. From Fig. 6, one sees that the waveguide with $W\times h$ of 500-nm×150-nm or 600-nm×175-nm have the steepest slope, indicating these two dimensions are better in the view point of the tradeoff between the insertion loss and the speed. Moreover, since the 600-nm-W modulator has a slightly larger $\Delta n_{eff}/\Delta n_{AlN}$ than the 500-nm-W modulator, as read from Fig. 5(b), the optimal parameters for the type-2 modulator are therefore chosen as t_{AlN} = 50 nm, W = 600 nm, h = 175 nm, and d = 600 nm. It gives $\Delta n_{eff}/\Delta n_{AlN}$ = 0.433, $\Delta n_{eff}/\Delta V = 3.46\times10^{-5}$ /V, and the contact-induced propagation loss = 0.35 dB/cm.

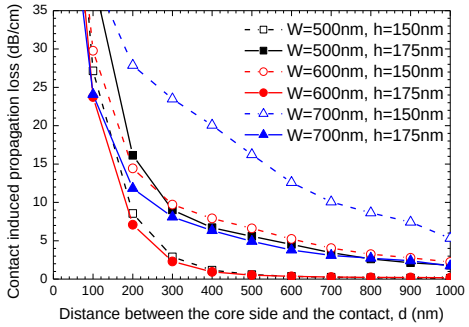

Fig. 6. Calculated propagation loss induced by optical absorption in the highly doped contact region as a function of the electrode spacing d for the type-2 modulator with t_{AlN} = 50 nm.

Next, the doping type of Si/poly-Si should be chosen to make Δn_{eff} induced by the carrier density variation have the same sign as that induced by Δn_{AlN}. The sign of Δn_{AlN} depends on the sign of the driving voltage applied on the AlN layer. It has been experimentally observed that n_{AlN} increases when a positive voltage is applied on the top of the deposited AlN layer and *vice versa* [9]. Since the sign of Δn_{eff} induced by the carrier accumulation is negative, it thus requires a negative voltage to be applied on the poly-Si layer to provide a negative Δn_{AlN}. Therefore, the Si layer should be p-type and the poly-Si layer should be n-type for carrier accumulation. The doping concentration is chosen based on the tradeoff

between the insertion loss and the speed since larger doping concentration leads to higher speed (due to smaller resistance) and larger propagation loss. Here we simply assume that both the p-type Si and the n-type poly-Si have the same uniform doping concentrations of $N_A = N_D = 1\times10^{17}$ cm^{-3} for simplicity.

III. MODULATOR PERFORMANCES

The performance of the type-2 modulator with the abovementioned optimal geometry and doping concentrations is estimated by taking the effects of doping, electrode, and absorption/scatting loss in the poly-Si/Si layers into account. The AlN film is assumed to be lossless because the fabricated AlN waveguides exhibit a very low propagation loss of ~0.6 dB/cm [8-9]. We also assume that the roughness-induced loss at the interfaces between Si (poly-Si) and AlN is similar to that at the interfaces between Si (poly-Si) and SiO_2 because the Si waveguide with the AlN cladding exhibits similar propagation loss as that with the SiO_2 cladding. Upon a voltage applying between the Si and poly-Si layers, carrier densities (ΔN_e for electrons and ΔN_h for holes) near the gate dielectric vary as $\Delta N_e = \Delta N_h = \frac{\varepsilon_0 \kappa}{e t_{AlN} t}(V - V_{FB})$, where ε_0 is the vacuum permittivity, $\kappa = 10$ [11-13], e is the electron charge, and t is the effective charge layer thickness. The accumulated carriers are located near the AlN/poly-Si and AlN/Si interfaces and the carrier density decays quickly away from the interfaces. Here the thin nonuniform charge layer on either side is simply approximated by a uniform layer with $t = 10$ nm [2]. The error due to this approximation is less than 8% as compared with the simulation results obtained from more complex device models. The un-doped Si and poly-Si wire waveguides have typical propagation losses of ~2 and ~10 dB/cm, respectively [15]. These losses, together with that induced by the 1×10^{17}-cm^{-3} doping, are modeled by the imaginary part of n_{Si} and $n_{poly\text{-}Si}$, which are then determined to be $3.4497+i1.31\times10^{-5}$ and $3.4499+i3.90\times10^{-5}$, respectively. Meanwhile, n_{AlN} changes due to the Pockels effect as $n_{AlN}(V) = n_{AlN} - \frac{1}{2} r_{33} n_{AlN}^2 \frac{V - V_{FB}}{t_{AlN}}$. r_{33} is experimentally determined to be ~1 pm/V for AlN deposited on SiO_2 [8-9]. Unfortunately, r_{33} for AlN deposited on Si is still unknown. It has been argued that optical properties of AlN depend on its crystallinity degree [16]. Since AlN deposited on Si has higher crystallinity degree than that deposited on SiO_2, it may have larger r_{33}. Moreover, other CMOS-compatible dielectrics, e.g. GaN or GaN/AlGaN superlattices, are also adoptable for our modulator, whose r_{33} is experimentally determined to be 8.94-19.2 pm/V [17]. Here, we set $r_{33} = 1$ pm/V as the lower limit for our modulator.

By comparing the complex mode indices of the modulator at $V - V_{FB} = 0$ V and 5 V, Δn_{eff} for the 1.55-μm TM mode is calculated to be 4.02×10^{-4}, in which 43% is contributed by the Pockels effect of AlN and 57% is contributed by the free-carrier plasma dispersion effect of poly-Si/Si. For comparison, Δn_{eff} for the 1.55-μm TE mode is 3.60×10^{-4}, in which 8% is contributed by the Pockels effect and 92 % is contributed by the free-carrier plasma dispersion effect. The $V_\pi \cdot L_\pi$ value for the TM mode is 0.95 V·cm. When $V - V_{FB} = 5$ V, the required length (L_π) is 1.9 mm. The insertion loss (including that induced by the highly doped contact region) is 1.2 dB/L_π, the voltage-dependent-loss (VDL) [2] is 1.2 dB/π-radian, and the modulation speed is 47 GHz, determined from the RC constant as $f_{\max} = \frac{1}{2\pi \cdot RC}$, where the capacitance C approximately equals to the dielectric capacitance as $C \approx L_\pi W \frac{\varepsilon_0 \kappa}{t_{AlN}}$ because it works at the accumulation mode. The resistance R is mainly contributed by the n-type poly-Si whose mobility is assumed to be 100 cm^2/V·s. The rf power consumption per bit estimated using the $\frac{1}{4} C \cdot V^2$ criterion is ~13 pJ/bit. The type-1 modulator with the abovementioned optimal dimensions offers faster speed of 64 GHz because it can be contacted from both sides, but with smaller $V_\pi \cdot L_\pi$ of 1.07 V·cm, in which 32% is contributed by the Pockels effect of AlN.

For comparison, the Si modulators with the same dimensions of $W = 600$ nm, $h = 175$ nm, and $d = 600$ nm and with the SiO_2 gate dielectric are calculated and the results are summarized in Table 1. In one case, the SiO_2 gate dielectric has the same equivalent oxide thickness (EOT) of 19.5 nm as the AlN modulator, thus they both have the same modulation speed. From Table 1, we can see that the modulation efficiency is improved by ~40% for the TM light by using the AlN gate dielectric. As the abovementioned, the modulation efficiency of the Si MOS modulator can be improved by thinning down the gate oxide thickness. The calculated modulation efficiency for the TE light is ~0.48 V·cm for the Si MOS modulator with 10-nm SiO_2 gate dielectric, close to the experimental result [4], but with a reduced speed of 24 GHz.

Table 1: Comparison of performances for Si modulators with AlN and SiO_2 gate dielectrics

Gate dielectric [a]		$V_\pi \cdot L_\pi$ (V·cm)	L_π (mm)[b]	Loss (dB/L_π)	VDL (dB/π)	Speed (GHz)	power (pJ/bit)
50-nm AlN	**TM**	**0.95**	**1.9**	**1.2**	**1.2**	**47**	**13**
	TE	1.08	2.2	2.0	2.0		15
19.5-nm SiO_2	TM	1.65	3.3	2.2	2.2	47	23
	TE	0.98	2.0	1.9	2.2		14
10-nm SiO_2	TM	0.68	1.4	1.1	2.4	24	19
	TE	0.48	0.96	0.93	2.3		13

[a] All modulators have the configuration as shown in Fig. 1(b) with the same geometry of $W = 600$ nm, $h = 175$ nm, and $d = 600$ nm and the same doping concentrations of $N_A = N_D = 1\times10^{17}$ cm^{-3}.

[b] L_π when the driving voltage swing $V - V_{FB} = 5$ V.

The modulator's performance will be significantly improved if r_{33} becomes larger. Fig. 7 plots Δn_{eff} and $V_\pi \cdot L_\pi$ as a function of r_{33} for the type-2 modulator. One sees Δn_{eff} increases almost linearly with r_{33} increasing. The contribution of the Pockels effect prevails over that of the carrier plasma dispersion effect when r_{33} is larger than 1.3 pm/V. When r_{33} = 10 pm/V, $V_\pi \cdot L_\pi$ reaches 0.2 V·cm and the modulator at 5-V voltage swing has L_π = 400 μm, *rf* power consumption = 2.7 pJ/bit, and speed = 47 GHz. If the voltage swing is reduced to 1 V, we can reduce t_{AlN} to 10 nm to keep E = 1 MV/cm. In this case, the contribution of the Pockels effect prevails over that of the carrier plasma dispersion effect when r_{33} is larger than 6.1 pm/V, and when r_{33} = 10 pm/V, the modulator at 1-V voltage swing has $V_\pi \cdot L_\pi$ = 0.083 V·cm, L_π = 830 μm, *rf* power consumption = 1.1 pJ/bit, and speed = 9.4 GHz. Moreover, when the sign of the driving voltage is reversed to positive, the sign of Δn_{AlN} is also reversed and the carriers near the gate dielectric are depleted to provide a positive Δn_{eff}. This feature can be utilized to realize a push-pull Mach-Zehnder modulator whose modulation length can be reduced by a factor of two.

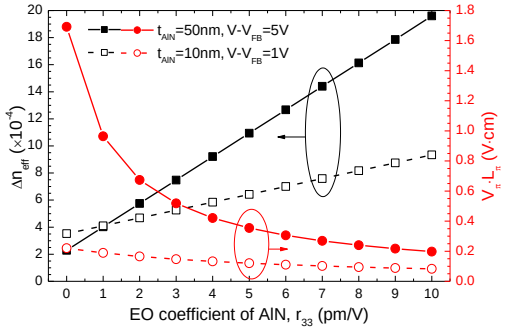

Fig. 7. Calculated Δn_{eff} and $V_\pi \cdot L_\pi$ as a function of the EO coefficient of the gate dielectric for the type-2 modulators with t_{AlN} = 50 nm at 5-V voltage swing or t_{AlN} = 10 nm at 1-V voltage swing.

In our laboratory, high-quality AlN films have been deposited on both SiO_2 and Si substrates for passive photonic devices [18] and the EO coefficient of ~1 pm/V has been measured. The fabrication of the proposed modulators is on-going and will be reported elsewhere.

In summary, a concept for designing Si MIS modulators on the silicon-on-insulator platform is introduced, in which a dielectric with inherent Pockels effect (here, AlN) is utilized as the gate dielectric. The modulation efficiency can be substantially improved even its EO coefficient is relatively low (~1 pm/V). The benefit is that this improvement does not sacrifice other performances. The modulator will be more attractive and useful if the EO coefficient of the gate dielectric can be further improved.

REFERENCES

[1] A. Liu, R. Jones, L. Liao, D. Samara-Rubio, D. Rubin, O. Cohen, R. Nicolaescu, and M. Paniccia, "A high-speed silicon optical modulator based on a metal-oxide-semiconductor capacitor," Nature, vol. 427, pp. 615-618, 2004.

[2] L. Liao, A. Liu, R. Jones, D. Rubin, D. S.-Rubio, O. Cohen, M. Salib, and M. Paniccia, "Phase modulation efficiency and transmission loss of silicon optical phase shifters, " IEEE J. Quantum. Electron., vol. 41, pp. 250-257, 2005.

[3] G. T. Reed, G. Mashanovich, F. Y. Gardes, and D. J. Thomson, "Silicon optical modulators," Nat. Photon., vol. 4, pp. 518-526, 2010.

[4] J. Fujikata, J. Ushida, T. Nakamura, M. Yu, S. Zhu, L. Ding, G. Q. Lo, and D. L. Kwong, "25 GHz operation of silicon optical modulator with projection MOS structure," in *Optical Fiber Communication Conf*. OSA, page OMI3, 2010.

[5] V. M. N. Passaro and F. Dell'Olio, "Scaling and optimization of MOS optical modulator in nanometer SOI waveguides," IEEE Trans. Nanotechnol., vol. **7**, pp. 401-408, 2008.

[6] R. K. Montgomery, M. Ghlron, P. Gothoskar, V. Patel, K. Shastrl, S. Pathak, and K. A. Yanushefski, "High-speed silicon-based electro-optical modulator," US Patent, US6845198B2, 2005.

[7] X. Zhang, B. Lee, C. Lin, A. X. Wang, A. Hosseini, and R. T. Chen, "Highly linear broadband optical modulator based on electro-optic polymer," IEEE Photon. J., vol. 4, pp. 2214-2228, 2012.

[8] C. Xiong, W. H. P. Pernice, and H. T. Tang, "Low-loss, silicon integrated, aluminum nitride photonic circuits and their use for electro-optic signal processing," Nano Lett., vol. 12, pp. 3562-2568, 2012.

[9] C. Xiong, W. H. Pernice, X. Sun, C. Schuck, K. Y. Fong, and H. X. Tang, "Aluminum nitride as a new material for chip-scale optomechanics and nonlinear optics," New J. of Phys., vol. 14, art. 095014, 2012.

[10] N. Sinha, G. E. Wabiszewski, R. Mahameed, V. V. Felmetsger, S. M. Tanner, R. W. Carpick, and G. Piazza, "Piezoelectric aluminum nitride nanoelectromechanical actuators," Appl. Phys. Lett., vol. 95, art. 053106, 2009.

[11] M. Schneider, A. Bittner, and U. Schmid, "Temperature dependent dielectric breakdown of sputter-deposited AlN thin films using a time-zero approach," Microsyst. Technol., vol. 20, pp. 751-757, 2014.

[12] S. Simeonov, S. Bakalova, E. Kafedjiiska, A. Szekeres, S. Grigorescu, F. Sima, G. Socol, and I. N. Mihailescu, "Al/AlN/Si MIS structures with pulsed-laser-deposited AlN films as gate dielectrics: electrical properties," Romanian J. of Information Sci. and Technol., vol. 10, pp. 251-259, 2007.

[13] K. Vijayalakshmi and V. V. Pillay, "Influence of deposition time on the microstructure and dielectric properties of AlN/Si thin films for enhanced hydrogen sensing application," Microelectron. Eng., vol.113, pp. 29-34, 2014.

[14] W. H. P. Pernice, C. Xiong, C. Schuck, and H. X. Tang, "Second harmonic generation in phase matched aluminum nitride waveguides and micro-ring resonators," Appl. Phys. Lett., vol. 100, art. 223501, 2012.

[15] S. Zhu, Q. Fang, M. B. Yu, G. Q. Lo, and D. L. Kwong, "Propagation losses in undoped and n-doped polycrystalline silicon wire waveguides," Opt. Exp., vol. 17, pp. 20891-20899, 2009.

[16] M. C. Larciprete, A. Bosco, A. Belardini, R. Li Voti, G. Leahu, C. Sibilia, E. Fazio, R. Ostuni, M. Bertolotti, A. Passaseo, B. Poti, and Z. Del Prete, "Blue second harmonic generation from aluminum nitride films deposited onto silicon by sputtering technique," J. Appl. Phys, vol. 100, art. 023507, 2006.

[17] P. Chen, X. G. Tu, S. P. Li, J. C. Li, W. Lin, H. Y. Chen, D. Y. Liu, J. Y. Kang, Y. H. Zuo, L. Zhao, S. W. Chen, Y. D. Yu, J. Z. Yu, and Q. M. Wang, "Enhanced Pockels effect in GaN/$Al_xGa_{1-x}N$ superlattice measured by polarization maintaining Mach-Zehnder interferometer," Appl. Phys. Lett., vol. 91, art. 031103, 2007.

[18] S. Zhu and G. Q. Lo, "Back-end integration of multilayer photonics on silicon," will be presented in Optical Fiber Comm. Conf. and Expo. (OFC), California, USA, Th1F.1, 2015.