Design and Analysis of 3D Heterogeneous Chiplet Stack for RF Front-End Module Minituarization

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***Abstract*—This paper presents the design, simulation, analysis and characterization of a heterogenous 3D integration approach for miniaturization of RF front-end modules. The 3D integrated stack consists of two dies using different technologies. The first die is a low-noise amplifier (LNA), designed and fabricated in 130nm 8SW RF SOI Global Foundries technology. The second die is a duplexer built using Qorvo's BAW technology. The first die is used as a base on which the second die is mounted. To achieve this integration a redistribution layer (RDL) has been designed and built on the backside of the first die. Through silicon vias (TSV) have also been designed and built to allow the top die to be routed and interconnected to the bottom die as well as to the outside world. The final size of the integrated module is 1x1.4x0.45 mm^3. This paper discusses in detail the design process of the module, the simulation models with the associated simulation results. It also presents measurement results obtained from a test vehicle design to extract the parasitics and equivalent circuit of the TSV through the SOI wafer. The signal losses measured through the test structures, that emulates the 3D stack environments, are below 0.2dB at 2GHz. These results are promising and give us confidence for the final functional module testing.**

Keywords—RDL, SiP, RF Front End, heterogenous integration, SOI, TSV.

I. Introduction

Mobile computing products continue to expand while data intensive applications keep growing exponentially without any signs of slowing down. The COVID-19 crisis has further accelerated the use of the internet on portable devices with hefty increases for video rich services such as Netflix, TikTok, or Youtube as well as video communication services such as Zoom, Teams, or Google Meet. All these devices and services require wireless connectivity and hence Radio Frequency (RF) and Front-End Modules (FEM) which provide wireless connectivity are essential. The wearable and portable nature of these devices has driven towards smaller form factors, thinner profiles, and better electrical and thermal performances for IC components and packaging technologies. The stringent requirements are achieved via 3D stacking for multi-function integration using a System-in-Package (SiP) approach. With multiple design topologies and technologies available for the different components necessary in a FEM module, miniaturization of individual components and their seamless integration in packaged devices and systems is essential to meet the growing demand of smart communication and entertainment devices. This trend will become more important for 5G devices and infrastructure. As discussed in [1] the smartphone world has aggressive specifications for power consumption, formfactor and integration. The major packaging challenge in smartphone applications is integrating the existing 4G LTE module with the upcoming 5G modules. For base stations, the challenge is less significant. One packaging technology that has shown potential for further formfactor reduction with improved electrical performance is fan-out wafer level packaging (FOWLP) [2,3,4]. Another extensively studied and discussed technology for RF SiP integration is high resistive silicon interposer and the associated through silicon vias [5]. Here we are exploring the use of both FOLWP RDL technology as well as TSV technology to further reduce the formfactor while conserving the electrical performance.

In this work, the electrical design of a heterogeneous 3D integration between an LNA built on 130nm 8SW RF SOI process and a duplexer built using BAW technology is discussed. The duplexer used in this study is designed for UMTS IMT with the uplink band between 1920-1980 MHz and downlink band between 2110-2170 MHz while the LNA is designed to work for the downlink band at 2100 MHz.

II. 3D Stack Configuration

The 3D heterogeneous stack consists of two dies an LNA die, and a duplexer die. The size of the individual duplexer and LNA dies are as follows: 1175 um x 525 um for the duplexer and 985 um x 750 um for the LNA respectively (Fig. 1) After analyzing the possible ways in which the two dies could be assembled in a 3D fashion, it was decided that the LNA die will be the bottom die while the duplexer will be attached on top. When the electrical connectivity is considered, it can be noted

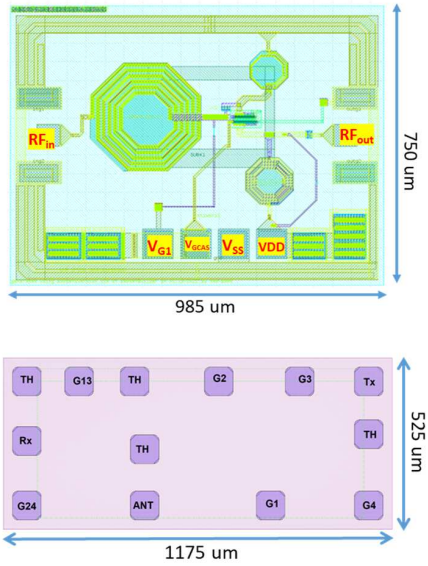


Fig. 1. Size and IO arrangement of the LNA die (top) and duplexer die (bottom).

that Rx port of the duplexer need to be connected to RF_{in} port of the LNA (Fig.1.) Further the Tx port and Ant port of the duplexer need to be available through 50-ohm connection to the outside world to be connected to power amplifier and antenna respectively. Similarly, the RF_{out} port and the power and ground connections (V_{G1}, V_{GCAS}, V_{ss} and V_{dd}) need to be available for next level of connection (e.g. on PCB).

A placement study of the two dies, including possible bump maps was done to figure out a realistic footprint of the 3D stack. When a realistic 350 um bump pitch, to the outside world, is considered, several possible scenarios were generated. Fig. 2 shows the two footprints that were chosen for further analysis and simulation. While during our analysis and study, the face to face and face to back topologies were considered, the final arrangement (Fig. 3.) was to attach the duplexer to the back of the LNA. The main reason of this face to back connection choice was guided by the placement of the LNA inductors. As these inductors can be detuned by large metal structures, they should not be near the RDL metal structure required to route the duplexer Tx and Ant ports, hence the LNA inductors will be

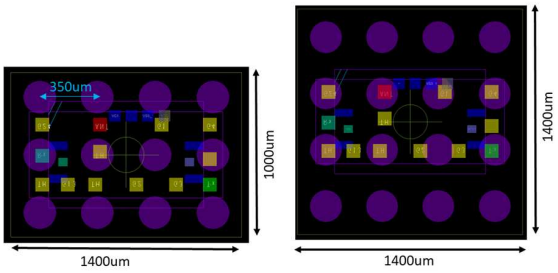


Fig. 2. Footprints of the considered stack. The relative position of the duplexer IOs and LNA IOs is shown as well as the position of the 350um pitch solder pads (purple).

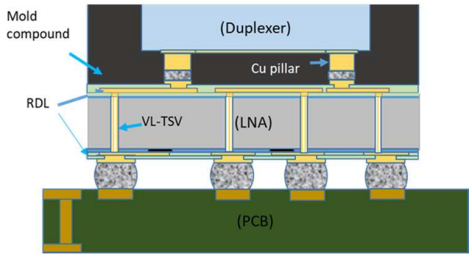


Fig. 3. Schematic diagram of the 3D heterogeneous RF chiplet integration.

facing the PCB side while the RDL will be placed on the back of the LNA die.

As it can be noted from Fig. 2, when the 350 um pitch pads are included in the footprint the size of the package becomes 1400 um x 1000 um, this being the smallest feasible footprint. For completeness of our study an alternative slightly larger footprint stack of 1400 um x 1440 um was also considered. It has to be mentioned here that the inner two pads of the smaller footprint design and the middle four pads for the larger footprint design are not used and hence removed since they may interfere with the LNA inductors.

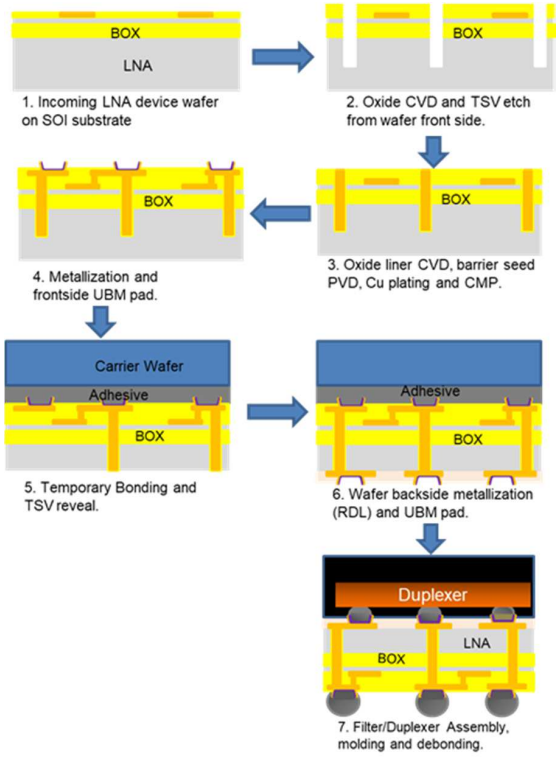


Fig. 4. Sketch of the process flow developed to achieve the 3D integration. The TSV are high aspect ratio (10:1) via-last fabrication from the front side of the SOI substrate. The TSV reveal and backside RDL are made before assembly and debonding [6].

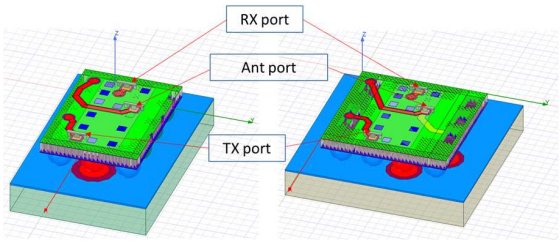


Fig. 5. Tilted view of the 3D models of the stack. On the left 1mm x 1.4mm footprint, on the right 1.4mm x 1.4mm footprint. The RDL consisting of CPW lines (red – signal, green - ground) is visible on the top. The position of the Rx, Tx and Ant port is shown for the two designs.

To summarize, the proposed 3D structure is using the LNA SOI as a base while the duplexer is connected on top of the LNA. On the back of the LNA, RDL is used to redistribute the three ports of the duplexer – Ant, Rx and Tx ports. The redistributed IOs are then routed on the other side of the LNA SOI die through TSVs. On the front side of the LNA, the back end of line (BEOL) process is used to connect the receiver duplexer port into the RF-in LNA port, while the rest of the RF paths (antenna, transmitter and RF-out) are redistributed and connected to pads on which solder balls can be attached. The 3D stack-up can be then mounted on a PCB or substrate as schematically shown in Fig.3. The top RDL is a single metal layer structure with a thickness of 5 um, while the bottom metallization is only 1 um as it uses BEOL technology. The TSVs are high aspect ratio 10:1, with 10 um diameter. To achieve this 3D integration, the process flow schematically shown in Fig. 4 has been developed during this project. A detailed discussion of process integration of high aspect ratio via-last TSV in SOI wafer is given in [6].

III. Models and Simulation of the 3D Stack

In order to understand the RF performance of the 3D stack and to optimize the layout of the RDL as well as the placement of the TSV transitions several models of the structure have been built and solved. First 3D full wave models of the two structures were built and solved in Ansys HFSS. Fig. 5 shows the two 3D models which include the RDL layer on top, the TSV trough the SOI substrate, the BEOL metallization and dielectrics on the bottom of the SOI substrate, the solder pads, solder balls and PCB.

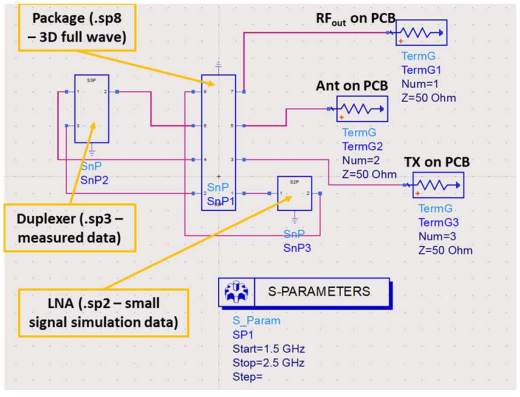
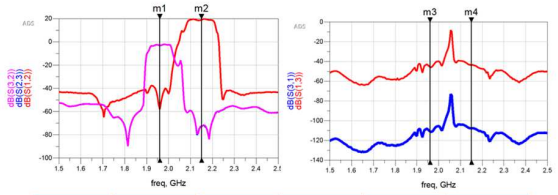


Fig. 6. Hybrid model of the 3D integrated module.

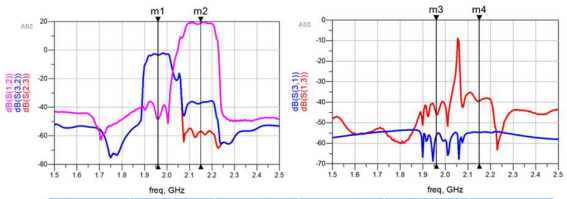


Freq (GHz)	|S12| dB	|S23| dB	|S32| dB	|S13| dB	|S31| dB
1.96	-58.08	-3.049	-3.046	-45.48	-110.9
2.15	18.95	-72.46	-72.85	-43.82	-107.77

Fig. 7. Frequency response of the LNA and duplexer without the package interconnecting structures (base line).

Another hybrid model of the duplexer, LNA and the interconnecting RDL layer, TSV and BEOL was built in ADS (Fig. 6). In the hybrid model S-parameter (Touchstone) data from measurements, circuit and full wave simulation was used to represent the duplexer, LNA and the package. Here the package refers to the whole interconnecting structure as described earlier. The model developed and solved for the package has eight ports. The ports on the top layer are shown graphically in Fig. 5. However, there are five more ports, two are located at the RF_{in} and RF_{out} ports of the LNA and three more are located on the PCB, one to allow access to the antenna port of the duplexer, another one to access the Tx port of the duplexer and the last to connect to the RF_{out} of the LNA. The duplexer has a three port S-parameter file containing measured data, while the LNA has a two port Touchstone file obtained from small signal simulation of the LNA circuit model. The hybrid model was used to analyze the effect of the package on the LNA and duplexer frequency response. Another use of the hybrid model was to develop an ideal baseline case where the effects of the interconnects are removed. The baseline was used in our analysis to identify the issues introduced by the interconnect structures. Once the issues were identified, further simulation of the 3D model of the package was carried out to find solutions and optimize the package.

The base line case frequency response is presented in Fig. 7. The duplexers uplink band (1920-1980 MHz) and down link band (2110-2170 MHz) are clearly visible. The down link is being amplified by the LNA as expected. The gain at 2.15 GHz is 18.95 dB while the insertion loss at 1.96 GHz is -3.04 dB. As the two models are not coupled, the isolation between different ports is ideal.



Freq (GHz)	|S12| dB	|S23| dB	|S32| dB	|S13| dB	|S31| dB
1.96	-48.57	-3.377	-3.374	-45.63	-56.11
2.15	18.826	-56.85	-37.13	-39.62	-54.73

Fig. 8. Frequency response of the 3D integrated module (small footprint case – 1.4mm x 1mm).

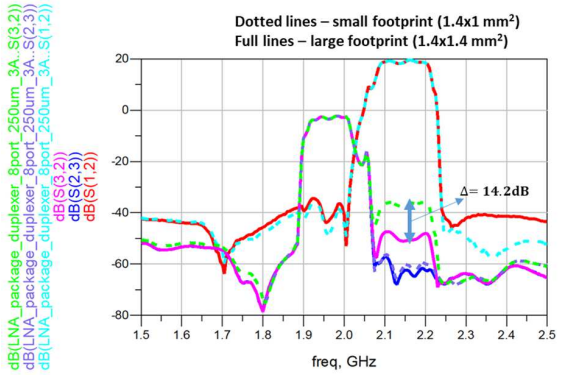


Fig. 9. Comparison of insertion loss and gain for the small footprint module (dotted lines) and large footprint module (full lines).

The frequency response of the small footprint (1.4x1 mm^2) 3D integrated module is shown in Fig. 8. It can be noted that the gain at 2.15 GHz has slightly dropped by 0.12 dB while the insertion loss at 1.96 GHz has also dropped by 0.33 dB. These changes are due to the loss introduced by the RDL, TSV transition and BEOL. The larger loss in the uplink channel is due to the longer CPW line that has to be routed on the RDL to link the duplexer TX pad to the TSV transition pad. The length of this CPW line is about 400um. The down link loss is only affected by the TSV loss as the RX pad of the duplexer is sitting on top of a TSV transition. Much larger changes can be observed in the isolation figures for the model that include the package.

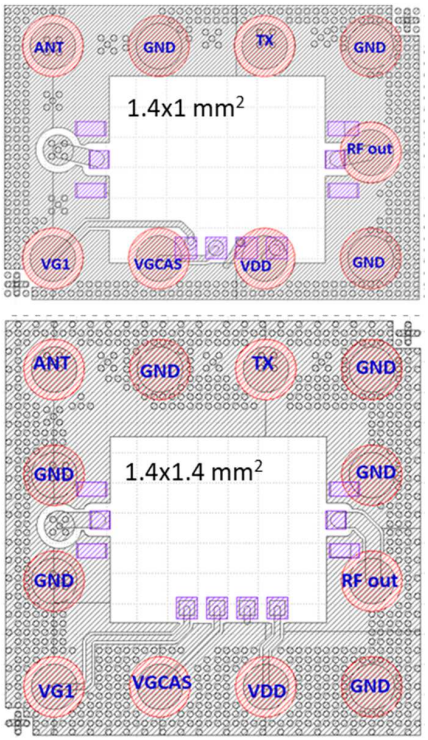


Fig. 10. The layout of the bottom layer and solder ball assignment of the RF 3D module.

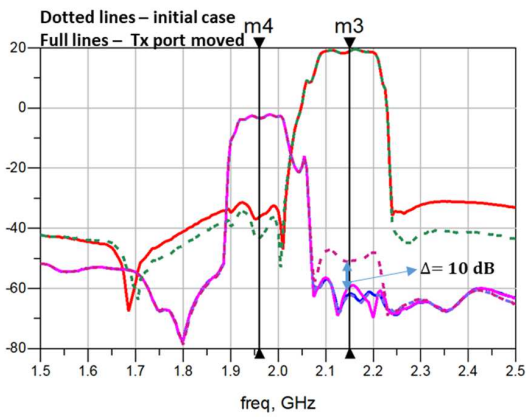


Fig. 11. Improvement in isolation when Tx port is moved away from the RF_{out} port.

At 1.96 GHz the isolation between the two bands has dropped by 10 dB while at 2.15 GHz the reduction is 15.8 dB. These figures clearly show the effect of the package. The largest change observed is in the coupling between the Rx and Tx ports (port 1 and port 3 respectively, as shown in Fig. 6). In the baseline structure the S31 shows values below -100 dB in both bands. However, when the package is included, the values increase with more than 50 dB. Similar results were obtained for the large package footprint (1.4x14 mm^2), as shown in Fig. 9. The larger footprint package shows an improvement of 14.2 dB in isolation between the two channels at 2.15 GHz. To

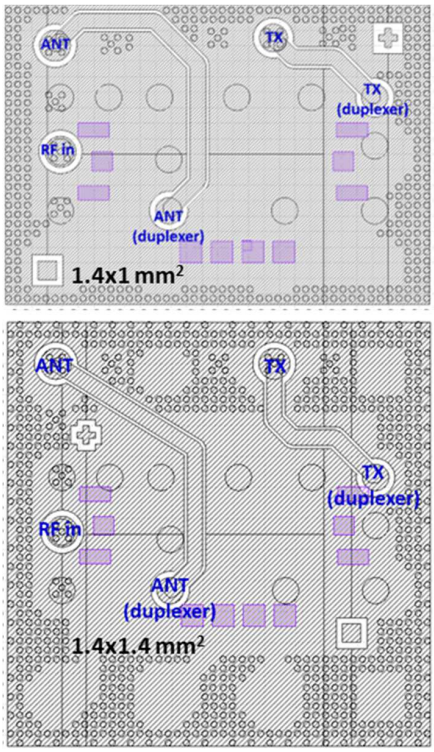


Fig. 12. Layout view of the top layer RDL of the 3D integrated module.

understand this improvement, one has to look at the bump assignment of the two packages. The 1.4x1 mm^2 package has enough space to have 12 solder balls. However due to the design constraints, three of the balls and corresponding pads need to be removed. The middle balls and pads are removed because of their negative effect on the LNA inductors. The left edge ball is removed as it interferes with the RF_{in} path of the LNA. The final design of the bottom layer is shown in top view of Fig. 10. Because of these limitations only three balls can be effectively used for the return path (GND). On the other hand, the 1.4x1.4 mm^2 package allows 16 balls to be fitted in the available area. After removing the middle four balls that will otherwise interfere with the LNA inductors, 12 more balls are still available (Fig. 10 bottom). This arrangement allows for six solder balls to be used as ground, hence improving the return path and isolation.

The isolation can be improved further if the position of the duplexer Tx port can be moved further away from the position of the RF_{out} port of the LNA. In the current design, the Tx duplexer port is located above the RF_{out} port of the LNA and although the signal is routed away to the side of the package to a TSV transition, the energy couples through the silicon substrate. To verify if the coupling from the Tx duplexer port can be reduced, a modified 3D model of the large foot print package (1.4 x 1.4 mm^2) was developed. In the modified 3D model the Tx port was moved from its initial position to the pad of the TSV transition that brings the Tx port to the bottom of the stack. In the new position the distance between the Tx port and the RF_{out} port is more than 4 times larger than in the current design. This situation was simulated, and the data was used to re-calculate the insertion loss and the gain of the 3D module. As shown in Fig. 11 the isolation is further improved by about 10 dB, proving that the position of the ports relative to each other is important in the 3D module integration. However, in the current project the position of the ports is fixed and cannot be modify. This points to the fact that co-design is a very important aspect when 3D system integration is required. The dies that are necessary for the 3D system must be architecturally and physically designed and planed with the 3D module specifications and limitations in mind. In our experience using dies developed for 2D integration in a 3D manner will result in suboptimum module designs.

IV. Measurements of RF Test Structures

In order to quantify the loss introduced by the RDL layer and the TSV transitions used in this 3D integration a test structures that includes CPW lines built on top, and bottom of an SOI wafer connected through TSV transitions was designed, fabricated and measured.

As shown in Fig. 10 and 12, the RF interconnect consists of CPW lines routed on the top layer RDL which are connected through TSV transitions to the bottom BEOL layer. CPW lines are used to route the signals to the associated pads or inputs on the BEOL. The lengths of the CPW lines on the top RDL are much longer than the CPW lines routed on the bottom BEOL layer. The longest CPW line is the one connecting the duplexer antenna port to the pad connected to the TSV transition, which has a length of about 1 mm in both designs. The other transmission line connecting the duplexer Tx port to its

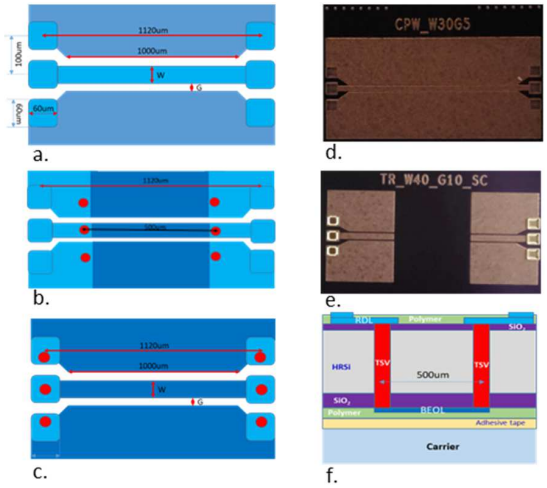


Fig. 13. CPW test structures.

a. CPW line on top RDL; b. CPW on the RDL-TSV transition-CPW on BEOL TSV transition-CPW on the RDL; c. TSV transition-CPW on BEOL-TSV transition; d. Fabricated CPW line on top RDL; e. Fabricated CPW on the RDL-TSV transition-CPW on BEOL TSV transition-CPW on the RDL; f. Cross section the test vehicle.

associated TSV transition is 0.5 mm long for both designs. On the other hand, on the bottom layer the longest CPW line is about 240 um connecting the LNA RF_{out} port to its associated package pad. This CPW line is specific to the 1.4x1.4 mm^2 package, the corresponding line in the small footprint design is less than 100 um length.

With this information in mind, a series of test structures were designed and fabricated [6] on an SOI wafer. The top view drawings and pictures of the test structures as well the drawing of the test structure cross section are given in figure 13. Three types of test structures having the same length were included in the test vehicle: CPW lines on the top RDL only (Fig. 13a. & 13d.), CPW lines on the top RDL connected through a TSV transition to CPW lines on the BEOL which are then connected back to the top RDL through another TSV transition (Fig 13b. & 13e.), and finally TSV transition to CPW lines on BEOL and then TSV transition back to top RDL layer (Fig. 13c.). The probing pads for the test structures are accessible on the top RDL layer, and the SOI test wafer is supported by a carrier wafer as shown in Fig. 13f.

The test structures were measured in frequency domain from 100MHz to 15GHz. The insertion loss for the three types of test structures is presented in figure 14. It can be observed that the 1000 um CPW line routed on the RDL layer only, has the smallest insertion loss, while the 1000 um CPW routed on BEOL and connected to the top RDL layer through the TSV transition has the largest insertion loss. The hybrid test structure that has a component of CPW routed on the RDL layer and a part of 500 um CPW routed on the BEOL layers connected by the TSV transitions has an insertion loss that is larger than the 1000 um CPW line on the RDL layer only but smaller than the

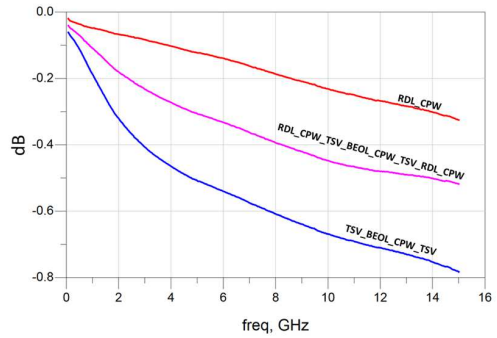


Fig. 14. Insertion loss measured for the three types of test structures.

1000 um CPW line route one the BEOL. The insertion loss in the middle of the two UMTS bands is given in Table I. Based on this data it can be noted that the BEOL CPW lines will introduce a large insertion loss. Therefore, in the functional module the length of the BEOL CPW is minimized.

TABLE I. MEASURED INSERTION LOSS

Freq (GHz)	Insertion Loss of the Test Structures (dB)		
	RDL_CPW	*RDL_CPW_TSV_BEOL_CPW_TSV_RDL_CPW*	*TSV_BEOL_CPW_TSV*
1.96	-0.067	-0.179	-0.317
2.15	-0.069	-0.188	-0.335

To understand how much loss the TSV transition introduces, an equivalent circuit model for the TSV transition was extracted from the measured data. Two types of TSV test structures are designed and included in the test wafer: an open circuit TSV transition and a short circuit TSV transition. The TSV test structures are measured in the frequency domain up to 15 GHz. The open circuit data was used to extract the equivalent capacitance (C) and conductance (G) of the ground-signal-ground (GSG) TSV transition, while short circuit data was used to extract the equivalent resistance (R) and inductance (L). The values of the parasitic are frequency dependent and the models used in this work have included this frequency dependency. The conductance and capacitance have a strong frequency dependance especially at the lower frequencies due to the non-ideal HRSi substrate properties. The extracted RLCG values at 1.96 GHz and 2.15 GHz are given in Table II. Fig. 15 presents that calculated insertion loss of the GSG TSV transition. The faster increase in insertion loss at lower frequencies, due to the finite resistivity of the SOI (HRSi) substrate and parasitic surface conductance (PSC) is clearly visible in Fig. 15. Similar trends of the insertion loss curves have been noted in all the tests structures that have TSV transitions (Fig. 14). The insertion loss introduced by a single TSV transition is -0.04 dB at 1.96 GHz and -0.042 dB at 2.15 GHz.

Fig. 15. Calculated insertion loss for a single GSG TSV transition.

TABLE II. GSG TSV TRANSITION RLCG

Freq (GHz)	RLCG values for GSG TSV transition			
	R(ohms)	*L(H)*	*C(F)*	*G(S)*
1.96	0.092	8.45e-11	3.92e-14	1.48e-4
2.15	0.092	8.44e-11	3.83e-14	1.55e-4

The equivalent circuit of the TSV transition was used to de-embed the TSV effects from the measured data of TSV_BEOL_CPW_TSV test structure. Once the de-embedding operation is done the return loss of the 1 mm long BEOL CPW line can be obtained. The insertion loss per unit length of the BEOL CPW and RDL CPW can now be compared. For example, at 1.96 GHz, BEOL CPW has a -0.236 dB/mm loss while the RDL CPW has -0.067 dB/mm insertion loss, while at 2.15 GHz the BEOL CPW has -0.251 dB/mm and the RDL CPW has -0.069 dB/mm. This data can be used in conjunction with the design details given in the previous section and calculate the maximum insertion loss that the RF interconnects will be contributing at the frequency of interest. The interconnect loss expected in the antenna path introduce by the package will be less than -0.15 dB (this includes the RDL CPW and the TSV transition) for both the uplink and downlink bands. At the transmitting frequency band (1.92-1.98 GHz) the insertion loss from the package is expected to be less than -0.075 dB. At the receiving band the total loss expected to be introduced by the interconnecting structures should be around -0.1 dB for the large footprint package while for the smaller footprint the loss should less than -0.07 dB. This low level of losses from the 3D module interconnect structure gives confidence for the future functional test of the 3D integrated module.

V. CONCLUSIONS

The design, simulation and analysis of a 3D integrated heterogenous module comprising of an SOI LNA and BAW duplexer was discussed. The 3D integration is achieved through a TSV first process designed and fabricated through the SOI LNA wafer. Following the TSV, an RDL layer is fabricated on the back of the SOI wafer, to create the interconnects required to access a duplexer die. The duplexer die is then attached to the LNA wafer forming the 3D RF module. The simulation and design constraints for two different footprint module sizes were discussed here. The data generated from the 3D EM and hybrid simulation models developed for this project, showed that coupling between the transmitter duplexer port and LNA RF_{out} port may be of concern, however to solve this issue a re-codesign of LNA, duplexer and the 3D integration approach may be necessary. Further we have demonstrated through simulation

and measurements that the insertion loss introduced by the TSV transitions and the RDL CPW lines introduce minimal insertion loss at the frequency bands of interests. The measured insertion losses of less than 0.15 dB in the worst-case scenario give us confidence in the anticipation the full function 3D module testing.

ACKNOWLEDGMENT

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