Identify critical packaging parameters impacting wafer warpage using FEA and statistical analysis techniques

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Abstract

Wafer warpage behaviors that result from thermal expansion coefficient (CTE) mismatch during packaging processes are usually complicated due to the interactive influences from materials, package designs and heating histories etc. Poorly controlled wafer warpage would affect the process precision adversely and even interrupt the process when exceeding the equipment's wafer handling limit. The optimization on the material selections, design parameters, and process conditions hence becomes critical to the wafer warpage control. Parametric studies using Finite Element Analysis (FEA) simulations are often performed prior to the actual wafer processes to examine the critical factors so that the warpage could be controlled accordingly. However, such conventional parametric study approach may oversimplify the complex system as it relies on predefined parameters.

Therefore, this paper describes a hybrid approach combining FEA simulations with statistical analysis for a more efficient way to quantify the influence of each parameter on wafer warpage during complex heterogeneous integration processes. This approach allows all the relevant parameters (material, design and process variables, and their interactions) of the wafer processes to be evaluated simultaneously and systematically. By performing the regression analysis, the wafer warpage prediction formula is derived. Hence the potential high wafer warpage could be mitigated as early as in the design stage by screening the variables of interest and performing associated optimizations via such warpage prediction equations.

Introduction

Identifying critical packaging parameters impacting warpage during wafer process for heterogeneous integration can indeed be a challenging task. The factors contributing to wafer warpage involving complex package design are often interconnected and can have complex interactions. For example, the combination of die size, package material properties, bonding method, and process conditions can all influence warpage. It can be difficult to isolate the individual impact of each parameter when they are interdependent. Furthermore, packaging materials, such as the wafer, package substrate, underfill, and bonding materials, can exhibit inherent variability in their properties. Packaging processes can involve various steps, each with its own set of process parameters and potential sources of variation. These variabilities can further complicate the identification of critical parameters, as their impact on warpage may vary from case to case. Understanding the influence of these variations on wafer warpage requires careful analysis and control. On the other hand, gathering experimental data on wafer warpage and the associated packaging parameters can be time-consuming and expensive. Limited experimental data availability may hinder the statistical analysis required to identify critical parameters accurately.

Previously, FEA simulations and the parametric studies have been widely used in the design process. However, such numerical parametric studies treat all the parameters equally and examine the parameters one at a time [1]. It works well for simple problem, but it may oversimplify complex system. Furthermore, it relies on predefined parameters which limits the exploration of unforeseen factors and the interaction between the variables.

To overcome these difficulties and limitations, this paper presents a systematic approach combining experimental validations, FEA simulations, and statistical analysis techniques [2]. Design of experiments (DOE) method is adopted to determine the most influential parameters by strategically selecting a representative set of experiments. Validated by the experimental data, the FEA models are adopted to run the DOE cases virtually without the need of conducting expensive experimental runs. Sensitivity analysis techniques can then be applied for quantifying the relative importance of different parameters based on the FEA results for the DOE cases. Regression analyses are performed to derive the relationship of the wafer warpage regarding the critical packaging parameters, material properties and process conditions.

The proposed approach combining FEA simulations with statistical analysis demonstrated in this paper could efficiently quantify the influence of each parameter on wafer warpage. Subsequently the identified critical packaging and process parameters could be carefully controlled or optimized to minimize warpage. The material properties are also assessed so that suitable materials from the candidates are selected.

Test Vehicle and Process Flow

The wafer test vehicle consists of one through-silicon-via (TSV) interposer, 3 metal layers at the front-side, one re-distribution layer (RDL) at the back-side. The passivation material at the front-side is SiO_2, and back-side passivation uses polyimide. The test vehicle stack-up schematic is shown in Fig.1.

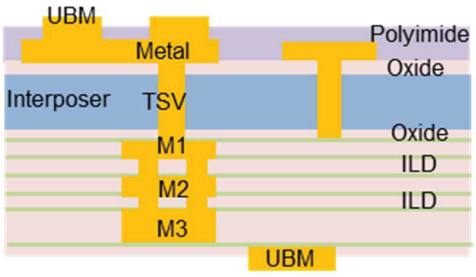


Fig. 1. Schematic of wafer stack-up for test vehicle

With different passivation materials at two sides of the interposer, the wafer structure is unbalanced in terms of thermal expansion. Polyimide usually has much higher CTE (~100 ppm/K) than SiO_2 (~0.5 ppm/K). Under the processes involving high temperatures, polyimide will expand much more than SiO_2 and hence may lead to high wafer warpage. Therefore, proper material candidate screening, design and process optimization are necessary to mitigate the foreseen large wafer warpage issue.

The wafer process flow considered in this study is shown in Fig.2. After oxide deposition on the interposer, TSV is fabricated. Front-side metal layers are subsequently formed using back-end-of-line (BEOL) processing technologies. In-between the metal layers, inter-layer-dielectric (ILD) layers are deposited. After plating the under-bump-metallization (UBM) on the front-side, interposer is then attached to the carrier wafer and is thinned down to reveal the TSVs for back-side processing. Oxide is first deposited on the wafer back-side, followed by the RDL fabrication. Polyimide is then coated on top of RDL and cured. After the backside UBM plating, the wafer is ready for debonding for subsequent assembly processes.

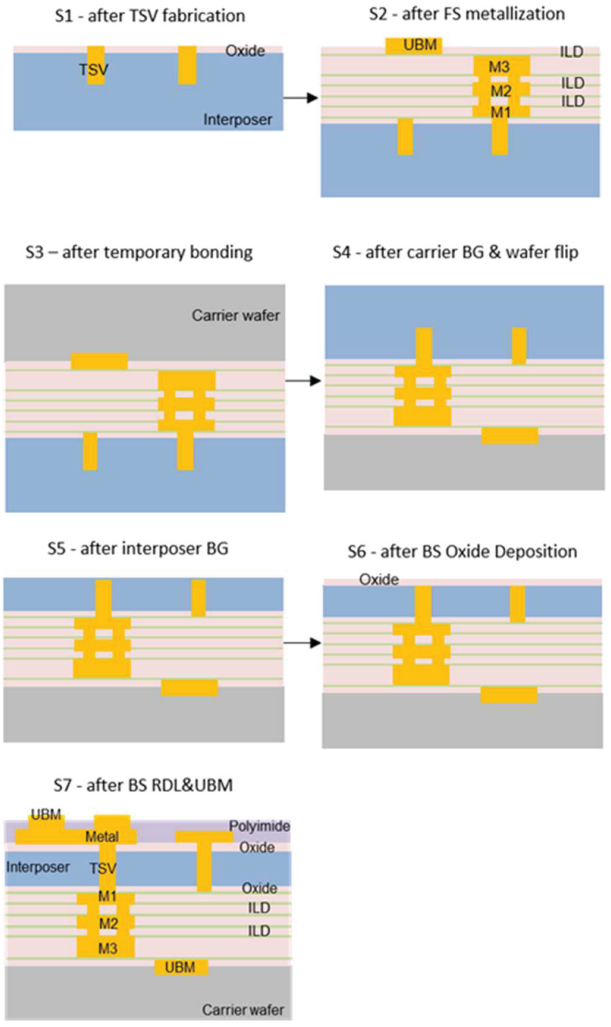


Fig. 2. Process flow of the wafer fabrication

FEA Model and Material Properties

Given the wafer stack-up structure, a quarterly symmetric FEA model shown in Fig.3 is built to reduce the computational effort. Two side-faces cross the wafer center are set as symmetric conditions. Each process step illustrated in Fig.2 is simulated using FEA simulator Ansys Mechanical.

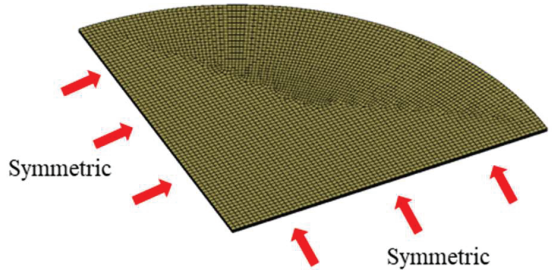


Fig. 3. Quarterly symmetric FEA model for the wafer stack-up

The dimension and design parameter details of the wafer model for the base case are listed in Table.1. The stress-free temperatures for individual materials are assumed to be the same as their respective process temperatures, e.g., annealing temperature for Cu, deposition temperature for SiO_2 and curing temperature for polyimide etc.

Table 1. Dimension and design parameters of the wafer model considered in the base case.

Wafer stack-up	Material	Thickness (μm)	Cu density	Process temperature (°C)
TSV Interposer	Si/Cu	100	1%	25/25
FS Oxide	SiO_2/Cu	0.5	1%	400
FS Metal-1/2/3	SiO_2/Cu	1/1/2	30%/30%/40%	400/250
FS ILD	SiO_2/Cu	1/1	30%/40%	400/250
FS Passivation	SiO_2/Cu	0.3	17%	400/250
BS Oxide	SiO_2/Cu	3	1%	180/25
BS RDL	Polyimide /Cu	3	95%	200/25
BS Passivation	Polyimide /Cu	2	11%	200/25

The thermo-mechanical properties for all the materials involved are listed in Table 2. The fine features such as Cu pads, RDL traces and UBMs have the scale of microns, while the wafer size is 300mm in diameter. This imposes great difficulty in explicitly simulating these fine features. Therefore, effective material approach is applied to simplify the FEA model. The effective material properties of the layer with Cu fine features are calculated based on respective Cu densities in Table 1 using simple area fractions rule.

Table 2. Material thermo-mechanical properties.

Materials	Young's modulus (GPa)	Poisson's ratio	CTE (ppm/°C)	Tg (°C)
Copper	117	0.34	17	-
SiO_2	73	0.17	0.5	-
Polyimide	3.5/0.1	0.3	65/500	215
Si	131	0.28	2.6	-
SiC	410	0.14	4	-
Si carrier	131	0.28	2.6	-

Numerical DOE and Statistical Analysis

Six variables are of interest in this study, which are the interposer material and thickness, respective Cu densities in front-side metal layers (M1, M2 and M3), and Cu density in back-side RDL. Si and SiC are the two interposer material candidates. The minimum and maximum interposer thicknesses are 50µm and 100µm, respectively. The range of all the Cu densities are set from 1% to 95%. In the traditional parametric study, each variable will be investigated one at a time while fixing the rest of variables. Such approach is usually suitable for the simple system and lacks the capability to capture the interactive effects between the variables. For the complex multi-variable problems as the present study, a more systematic data analysis approach should be applied.

In this paper, a hybrid numerical analysis approach combining the FEA simulations and data analysis is developed. After FEA model is set up, the FEA simulations are performed according to the design-of-experiment (DOE) generated using the statistical tools such as Minitab in this study. The simulated wafer warpage results of the DOE are subsequently analyzed in Minitab to quantify and assess the significance of each variables considered. The relationship of the wafer warpage about the critical variables are thus derived by performing regression analysis. For the present wafer warpage study involving six variables, a DOE as listed in Table 3 is generated using Minitab. Half factorial DoE design is used and total 32 FEA design cases are to be performed to carry out the statistical analysis on the FEA results.

Table 3. DoE for FEA simulations.

Interposer		Cu density			
Material	Thickness [µm]	FS M1	FS M2	FS M3	BS RDL
Si/SiC	50	1%	1%	1%	95%
Si/SiC	100	1%	1%	1%	1%
Si/SiC	50	95%	1%	1%	1%
Si/SiC	100	95%	1%	1%	95%
Si/SiC	50	1%	95%	1%	1%
Si/SiC	100	1%	95%	1%	95%
Si/SiC	50	95%	95%	1%	95%
Si/SiC	100	95%	95%	1%	1%
Si/SiC	50	1%	1%	95%	1%
Si/SiC	100	1%	1%	95%	95%
Si/SiC	50	95%	1%	95%	95%
Si/SiC	100	95%	1%	95%	1%
Si/SiC	50	1%	95%	95%	95%
Si/SiC	100	1%	95%	95%	1%
Si/SiC	50	95%	95%	95%	1%
Si/SiC	100	95%	95%	95%	95%

Experimental Validation of FEA Model

Prior to the FEA analysis on the DoE cases listed in Table 3, a validation case study was performed using FEA. The predicted wafer warpage is compared with the actual wafer warpage measurement. The process step selected in this validation case study is after backside RDL and UBM (S7 in Fig.2). The wafer stack-up structure is shown in Fig.4. The interposer material, thickness, and metal densities in each layer for the validation case study are listed in Table 4.

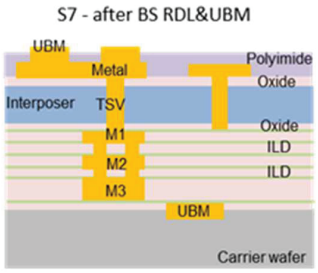


Fig. 4. Wafer stack-up after backside RDL and UBM fabrication (S7)

Table 4. Parameters considered in validation case.

Interposer		Cu density			
Material	Thickness [µm]	FS M1	FS M2	FS M3	BS RDL
Si	100	30%	30%	40%	95%

Fig.5 shows the wafer warpage contour after backside RDL and UBM fabrication predicted by FEA analysis for the validation case. The wafer warpage exhibits a smile face from side view, namely wafer edge higher than wafer center. Fig.6 compares the wafer warpage between the simulation result (607 µm) and actual measurement (599 µm). The difference is 8 µm. The comparison indicates that the simulation result matches the actual measurement well.

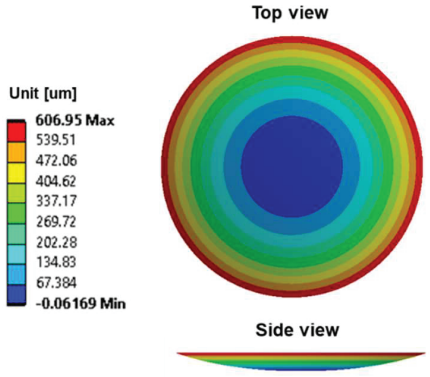


Fig. 5. FEA predicted wafer warpage after backside RDL and UBM fabrication (S7)

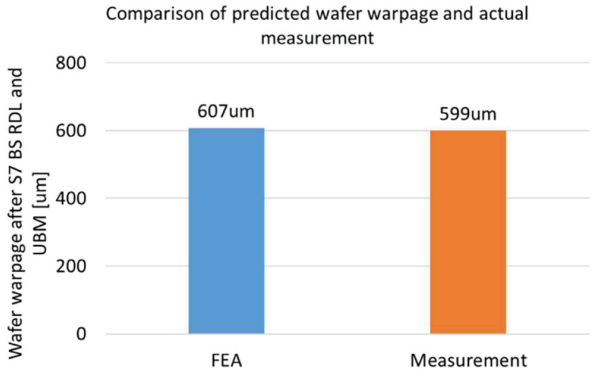


Fig. 6. Comparison of FEA predicted wafer warpage and actual measurement of the validation case

Results and Discussion

The validated FEA model is thus applied to simulate the base case (Table 1) and 32 DoE cases (Table 3). FEA results for each case contain the respective wafer warpages for the 7 process steps as illustrated in Fig.2.

Base Case: Process Dependent Wafer Warpage

The FEA results of the wafer warpage during the process flow for the base case is shown in Fig.7. It is observed that wafer warpage is built up to 480µm after the front-side processes (S2). After attaching the interposer to carrier wafer (S4), wafer warpage is reduced significantly. However, after back grinding the interposer (S5) to its designed thickness of 100µm for the base case, wafer warpage increases to 380µm again. After the backside processes (S6&S7), wafer warpage reaches 610µm.

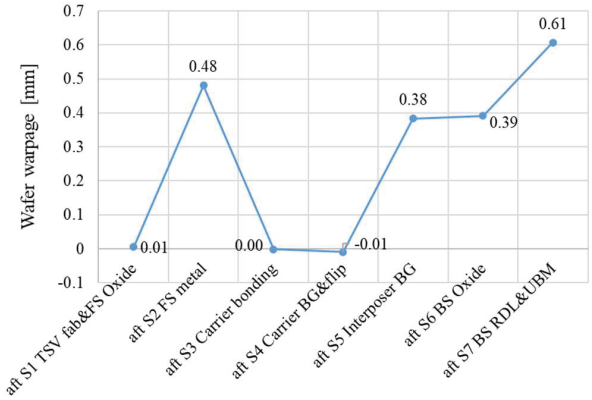


Fig. 7. Wafer warpage during process flow for the base case

It is understood that wafer warpage is highly dependent of Cu densities in both front-side and back-side of the wafer, as well as the interposer material and thickness. Therefore, in the following sections, results of the FEA DoE studies on these mentioned variables are discussed. For the sake of brevity, only the wafer warpage results after interposer back grinding (S5) and after backside RDL and UBM fabrication (S7) are discussed. The wafer warpage after these two steps is critical to the subsequent processes.

Process Step 5: after Interposer Back Grinding

Wafer stack-up after interposer back grinding is shown in Fig.8. At this stage, backside process has not started. Therefore, the DoE studies are limited to the interposer and front-side variables. FEA results for all 32 DoE cases are listed in Table 5. In general, wafer warpage varies from 0.14mm to 1.03mm. Different Cu density combinations in 3 front-side metal layers result in different wafer warpage.

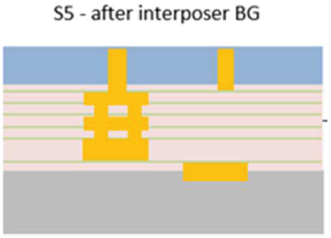


Fig. 8. Wafer stack-up after interposer back grinding (S5)

Table 5. FEA predicted wafer warpage after interposer back grinding (S5) for DoE cases

Interpose thickness [µm]	Cu density			FEA wafer warpage [mm]	
	FS M1	FS M2	FS M3	Si interposer	SiC interposer
50	1%	1%	1%	0.140	0.172
100	1%	1%	1%	0.140	0.181
50	95%	1%	1%	0.458	0.402
100	95%	1%	1%	0.390	0.326
50	1%	95%	1%	0.456	0.401
100	1%	95%	1%	0.388	0.325
50	95%	95%	1%	0.697	0.592
100	95%	95%	1%	0.595	0.457
50	1%	1%	95%	0.692	0.588
100	1%	1%	95%	0.591	0.453
50	95%	1%	95%	0.879	0.747
100	95%	1%	95%	0.760	0.571
50	1%	95%	95%	0.877	0.746
100	1%	95%	95%	0.759	0.570
50	95%	95%	95%	1.029	0.880
100	95%	95%	95%	0.901	0.677

To find out the effects of all the variables on the wafer warpage, FEA results shown in Table 5 are analyzed using Minitab. Main effect plots are presented in Fig. 9 for all the 5 variables. The statistical analysis results indicate that wafer warpage after interposer back grinding is inversely proportional to the interposer thickness, and proportional to the Cu densities in all three front-side metal layers. In spite of its higher CTE, SiC interposer has lower wafer warpage compared to Si interposer. This is due to the higher modulus of SiC which makes the wafer structure stiffer. Among all 5 variables considered, Cu density in M3 layer has most significant effect on the wafer warpage. The higher the Cu density, the more thermal mismatch as well as the warpage due to the high CTE of Cu.

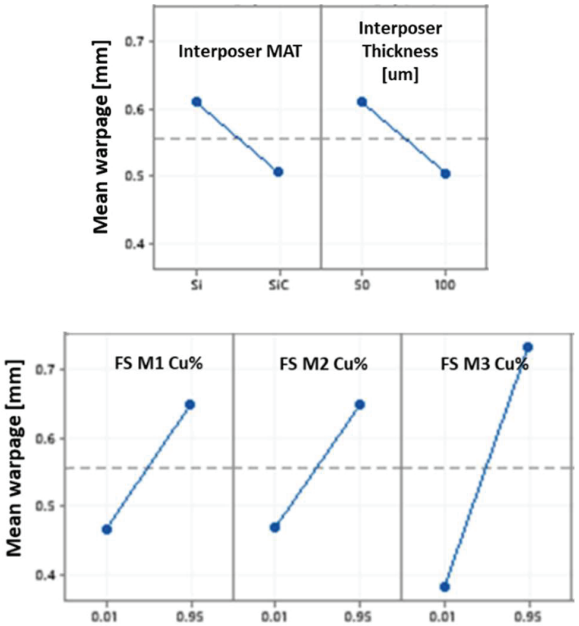


Fig. 9. Main effects plots for S5 after interposer back grinding

To further assess the significance of the variables on wafer warpage after interposer back grinding step, pareto chart is generated from the statistical analysis and is shown in Fig.10. It clearly shows that Cu density in M3 layer is the most significant factor for wafer warpage at this step, followed by Cu densities in M1 layer and M2 layer, interposer thickness and material. The interactions of the variables are generally trivial except for those involving Cu density in M3 layer. This is because among all 3 metal layers at the front-side, M3 layer has the largest thickness.

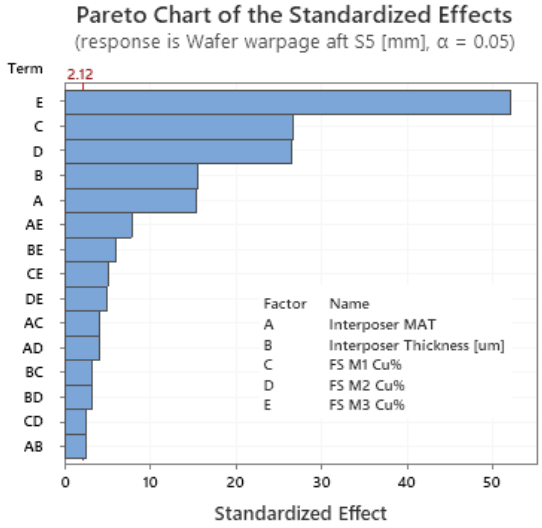


Fig. 10. Pareto chart of the effects on wafer warpage after interposer back grinding (S5)

The relationship of the wafer warpage at this step regarding the significant variables and associated interactions can also be derived by performing regression analysis. The wafer warpage after interposer back grinding could be predicted based on the following regression equations:

For Si interposer:

$$\begin{aligned}\text{Wafer warpage aft S5 [mm]} = {} & 0.1716 - 0.000522\ \text{Interposer Thickness [um]} + 0.3471\ \text{FS M1 Cu\%} \\ & + 0.3452\ \text{FS M2 Cu\%} + 0.6187\ \text{FS M3 Cu\%} \\ & - 0.000682\ \text{Interposer Thickness [um]*FS M1 Cu\%} \\ & - 0.000680\ \text{Interposer Thickness [um]*FS M2 Cu\%} \\ & - 0.001215\ \text{Interposer Thickness [um]*FS M3 Cu\%} \\ & - 0.0521\ \text{FS M1 Cu\%*FS M2 Cu\%} - 0.1033\ \text{FS M1 Cu\%*FS M3 Cu\%} \\ & - 0.1026\ \text{FS M2 Cu\%*FS M3 Cu\%}\end{aligned} \quad (1)$$

For SiC interposer:

$$\begin{aligned}\text{Wafer warpage aft S5 [mm]} = {} & 0.1916 - 0.000289\ \text{Interposer Thickness [um]} + 0.2834\ \text{FS M1 Cu\%} \\ & + 0.2817\ \text{FS M2 Cu\%} + 0.5284\ \text{FS M3 Cu\%} \\ & - 0.001134\ \text{Interposer Thickness [um]*FS M1 Cu\%} \\ & - 0.001131\ \text{Interposer Thickness [um]*FS M2 Cu\%} \\ & - 0.002183\ \text{Interposer Thickness [um]*FS M3 Cu\%} \\ & - 0.0252\ \text{FS M1 Cu\%*FS M2 Cu\%} - 0.0509\ \text{FS M1 Cu\%*FS M3 Cu\%} \\ & - 0.0505\ \text{FS M2 Cu\%*FS M3 Cu\%}\end{aligned} \quad (2)$$

Process Step 7: after Backside RDL and UBM Fabrication

Similarly, wafer warpage results after backside RDL and UBM fabrication is discussed in this section. This is the last step of the lithograph processes. Wafer warpage after this step would affect the subsequent assembly process, e.g., debonding, wafer dicing etc. The schematic of wafer stack-up after this step is illustrated in Fig.11. FEA results of the DoE cases are listed in Table 6. For all the DoE cases considered, wafer warpage varies from 0.4mm to 1.2mm. This is the step with the largest wafer warpage.

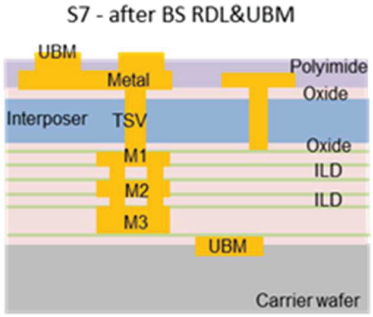
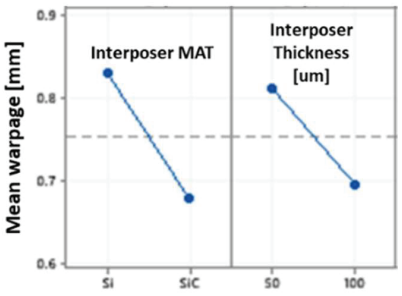


Fig. 11. Wafer stack-up after backside RDL and UBM fabrication (S7)

Table 6. FEA predicted wafer warpage after backside RDL and UBM fabrication (S7) for DoE cases

Interpose thickness [μm]	Cu density				FEA wafer warpage [mm]	
	FS M1	FS M2	FS M3	BS RDL	Si interposer	SiC interposer
50	1%	1%	1%	95%	0.455	0.405
100	1%	1%	1%	1%	0.491	0.402
50	95%	1%	1%	1%	0.750	0.641
100	95%	1%	1%	95%	0.619	0.484
50	1%	95%	1%	1%	0.748	0.640
100	1%	95%	1%	95%	0.618	0.483
50	95%	95%	1%	95%	0.874	0.749
100	95%	95%	1%	1%	0.830	0.635
50	1%	1%	95%	1%	0.919	0.786
100	1%	1%	95%	95%	0.777	0.594
50	95%	1%	95%	95%	1.021	0.877
100	95%	1%	95%	1%	0.958	0.731
50	1%	95%	95%	95%	1.020	0.876
100	1%	95%	95%	1%	0.958	0.731
50	95%	95%	95%	1%	1.191	1.026
100	95%	95%	95%	95%	1.031	0.788

By checking the main effects plot in Fig.12, it is observed that after S7 back-side RDL and UBM fabrication, the trend on the wafer warpage for interposer material and thickness, and Cu densities in the front-side three metal layers remain similar to the respective effects after S5 interposer back grinding as shown in Fig.9. For step S7, back-side RDL Cu density is an additional variable and wafer warpage is inversely proportional to it.



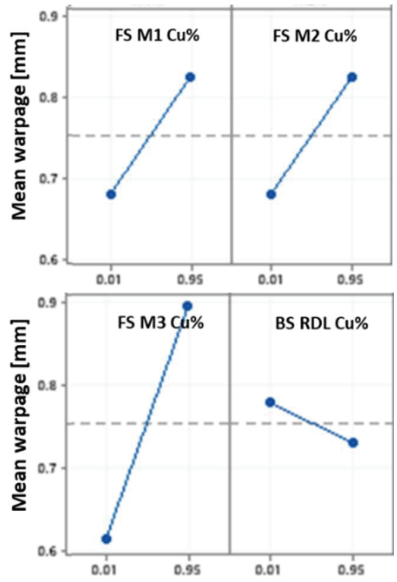


Fig. 12. Main effects plots for S7 backside RDL and UBM fabrication

It is noticed that the back-side passivation material is polyimide, which has much larger CTE compared to front-side passivation material SiO_2. However, due to the lower process temperature (200°C) for the back-side processes than that for front-side processes (400°C), backside RDL Cu density effect is therefore less significant. This observation could be found in the Pareto chart of the effects in Fig.13. After backside RDL and UBM fabrication, the most significant effect is still the Cu density in the front-side M3 layer. However, interposer material shows more influence on the wafer warpage at this step and becomes the 2nd most significant effect.

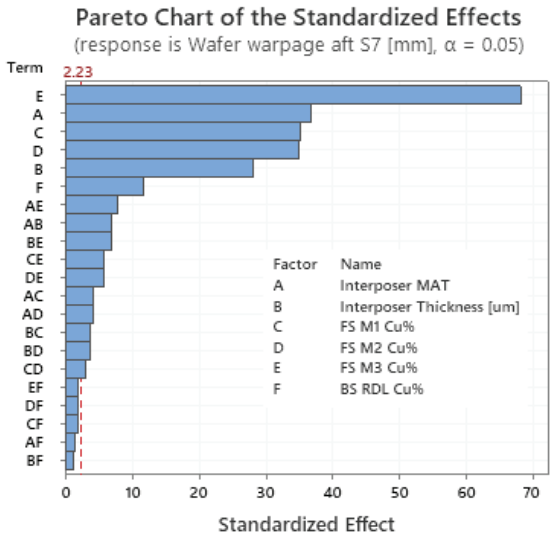


Fig. 13. Pareto chart of the effects on wafer warpage after backside RDL and UBM fabrication (S7)

Similar formula showing the wafer warpage as a function of all six variables considered is given by the regression analysis. The regression equations to predict the wafer warpage after back-side RDL and UBM fabrication are shown as follows for Si and SiC interposer, respectively.

For Si interposer:

$$\begin{aligned}\text{Wafer warpage aft S7 [mm]} = {} & 0.5799 - 0.000957\ \text{Interposer Thickness [um]} + 0.2500\ \text{FS M1 Cu\%} \\ & + 0.2487\ \text{FS M2 Cu\%} + 0.4474\ \text{FS M3 Cu\%} - 0.1030\ \text{BS RDL Cu\%} \\ & - 0.000515\ \text{Interposer Thickness [um]*FS M1 Cu\%} \\ & - 0.000514\ \text{Interposer Thickness [um]*FS M2 Cu\%} \\ & - 0.000848\ \text{Interposer Thickness [um]*FS M3 Cu\%} \\ & + 0.000247\ \text{Interposer Thickness [um]*BS RDL Cu\%} \\ & - 0.03505\ \text{FS M1 Cu\%*FS M2 Cu\%} - 0.06594\ \text{FS M1 Cu\%*FS M3 Cu\%} \\ & + 0.01767\ \text{FS M1 Cu\%*BS RDL Cu\%} - 0.06552\ \text{FS M2 Cu\%*FS M3 Cu\%} \\ & + 0.01765\ \text{FS M2 Cu\%*BS RDL Cu\%} + 0.02137\ \text{FS M3 Cu\%*BS RDL Cu\%} \end{aligned} \quad (3)$$

For SiC interposer:

$$\begin{aligned}\text{Wafer warpage aft S7 [mm]} = {} & 0.5405 - 0.001429\ \text{Interposer Thickness [um]} + 0.2185\ \text{FS M1 Cu\%} \\ & + 0.2171\ \text{FS M2 Cu\%} + 0.4095\ \text{FS M3 Cu\%} - 0.08533\ \text{BS RDL Cu\%} \\ & - 0.000831\ \text{Interposer Thickness [um]*FS M1 Cu\%} \\ & - 0.000829\ \text{Interposer Thickness [um]*FS M2 Cu\%} \\ & - 0.001553\ \text{Interposer Thickness [um]*FS M3 Cu\%} \\ & + 0.000195\ \text{Interposer Thickness [um]*BS RDL Cu\%} \\ & - 0.02247\ \text{FS M1 Cu\%*FS M2 Cu\%} - 0.04065\ \text{FS M1 Cu\%*FS M3 Cu\%} \\ & + 0.01875\ \text{FS M1 Cu\%*BS RDL Cu\%} - 0.04037\ \text{FS M2 Cu\%*FS M3 Cu\%} \\ & + 0.01878\ \text{FS M2 Cu\%*BS RDL Cu\%} + 0.01654\ \text{FS M3 Cu\%*BS RDL Cu\%} \end{aligned} \quad (4)$$

Conclusions

A hybrid FEA numerical study and statistical analysis is presented for predicting the wafer warpage during the heterogeneous integration process. The validated FEA model is applied to generate the numerical results of the factorial DoE cases given by the statistical analysis. The FEA wafer warpage results are then analyzed in a statistical tool to identify the significance of the individual variables considered in the study.

The main findings are summarized as follows:

- Among all six variables considered, namely interposer material and thickness, Cu densities in the front-side three metal layers, and Cu density in the back-side RDL layer, Cu density in the front-side M3 layer has the most significance. This is because the front-side M3 layer has the largest thickness among all 3 metal layers. The high process temperature of 400°C for the front-side process also contributes to the significance in its effect on the wafer warpage.
- Although the back-side RDL layer uses polyimide as passivation material, which has much higher CTE compared to SiO_2, the Cu density in this layer is not as critical as the front-side Cu density due to the lower process temperature of 200°C for the back-side processes.
- Wafer warpage is found lower for SiC interposer than that for Si interposer as SiC is much stiffer than Si.
- Wafer warpage increases proportionally to Cu density in the front-side three metal layers, while it decreases proportionally to the Cu density in the back-side RDL layer and the interposer thickness.

By carrying out the statistical analysis, the regression equation for the wafer warpage as a function of all six variables is developed. If the variables are within the ranges shown in DoE Table 3, wafer warpage can be estimated using the derived regression equations. This numerical tool can facilitate wafer warpage optimization during the design stage without the need for prototypes.

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