Two-phase Liquid Cooling of Vertically Stacked High-Power Chips with Backside-Embedded Micro-Pin Fins

Huicheng Feng, Gongyue Tang, Xiaowu Zhang, *Fellow, IEEE*, Boon Long Lau, and Ming Chinq Jong

***Abstract*—Three-dimensional integrated circuits (3D ICs) enable a higher level of device integration for high-performance computing but also introduce significant thermal challenges due to increased power density. This letter demonstrates a two-phase liquid cooling approach for stacked high-power chips featuring backside-embedded micro-pin fins. Deionized water is circulated directly through the chips, providing internal cooling. The results show effective thermal management, with maximum power levels of 126 W and 140 W achieved for Chip 1 and Chip 2, respectively. Temperature fluctuations in the two-phase regime remain minimal, confirming the approach's practicality. Chip 2 benefits from lower temperatures and higher heat transfer coefficients due to double-side cooling by water flowing through both itself and Chip 1. Increasing the flowrate reduces the chip temperatures and improves heat transfer coefficients but incurs higher pressure drops. The coefficient of performance decreases with flowrate but improves with heat power. These findings validate the feasibility of the proposed cooling method and establish a proof of concept for further integration in 3D IC designs.**

***Index Terms*—3D ICs, micro-pin fins, two-phase cooling**

I. Introduction

The relentless demand for higher performance in electronics has driven the adoption of three-dimensional integrated circuits (3D ICs), which overcome the limitations of traditional planar designs through the vertical stacking of active layers. This architecture enables greater integration density, shorter interconnects, and enhanced functionality [1]–[4]. However, the compact nature of 3D ICs exacerbates thermal challenges, as concentrated power dissipation within a small volume leads to high power densities and restricted heat dissipation pathways. Without effective cooling, thermal hotspots degrade performance, reliability, and device lifetime.

Conventional air-cooling methods are insufficient for managing the thermal demands of high-performance 3D ICs. Consequently, liquid cooling has emerged as a superior alternative [5]–[8]. Among liquid cooling strategies, two-phase cooling with micro-pin fins is particularly effective, combining low thermal resistance with high heat transfer coefficient from phase change [9]–[11]. Micro-pin fins enhance thermal performance by increasing surface area, promoting nucleate boiling, and improving liquid replenishment to prevent dryout [12]–[15].

Despite these advantages, most prior studies have examined only single-layer cooling, such as bottom interposers with embedded microstructures or top-side cooling [16]–[18]. These approaches are inadequate for vertically stacked high-power chips, where distant layers are particularly challenging to cool. To address this limitation, we developed thermal test vehicles with through-silicon vias (TSVs) that enable embedded liquid cooling of two vertically stacked chips [19], along with preliminary feasibility demonstrations [20], [21]. In this work, we significantly expand upon those initial results with a detailed experimental investigation of two-phase liquid cooling in stacked chips, each featuring backside-embedded micro-pin fins. Deionized water is supplied to both chips in parallel, providing direct internal cooling. In contrast to our earlier studies, we now provide comprehensive two-phase characterization, including stable thermal regulation with maximum temperature fluctuations within $\pm 3.2^\circ$C. These results validate the feasibility of this approach for 3D IC integration and highlight its advantages over single-layer cooling techniques.

II. Methodology

A thermal test vehicle (TTV) was designed and fabricated (Fig. 1). The assembly consists of a silicon cap, two silicon chips, and a printed circuit board (PCB), vertically stacked as shown in Fig. 1(a). Each silicon die is 300 μm thick with a 10 mm $\times$ 10 mm footprint. Both chips feature backside-embedded micro-pin fins for cooling, and frontside-deposited heaters and resistance temperature detectors (RTDs) for heat load application and temperature monitoring. The staggered micro-pin fins are 100 μm in diameter, 150 μm in pitch, and 200 μm in height (Fig. 1(b)). The heaters and RTDs are designed as meandering structures with widths of 200 μm and 20 μm, respectively (Fig. 1(c)). Through-silicon vias (TSVs) with a diameter of 30 μm are fabricated in Chip 1 for Chip 2's electrical connections (Fig. 1(d)).

The TTV was fabricated using a via-first TSV process. A 2 μm oxide hardmask defined the via pattern, followed by deep reactive ion etching. A chemical vapor deposition (CVD) oxide liner and physical vapor deposition (PVD) tantalum/copper

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(Ta/Cu) seed were deposited, then copper was electroplated bottom-up to fill the vias. Post-plating annealing and chemical mechanical polishing (CMP) removed excessive copper and planarized the surface. Subsequent frontside processing included dielectric vias for heater/RTD contacts, PVD titanium (Ti) metallization (3.6 μm), polyimide dielectric isolation, and copper/nickel/gold (Cu/Ni/Au) under-bump metallization (UBM) for solder bonding [19].

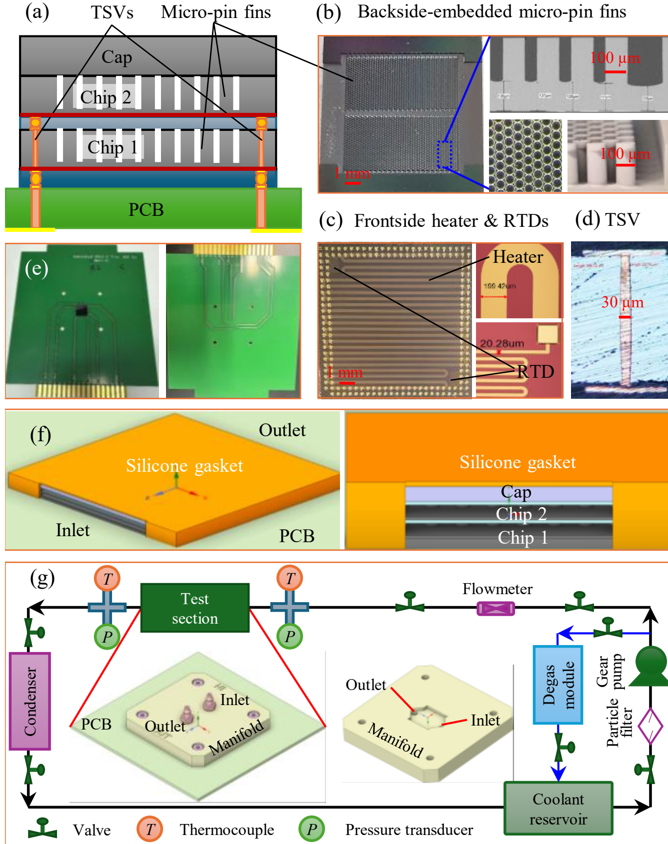

Fig. 1. (a) Cross-sectional schematic of the TTV; (b) backside-embedded micro-pin fins (diameter: 100 μm, pitch: 150 μm, height: 200 μm); (c) frontside-deposited meandering heater and RTDs (widths: 200 μm and 20 μm, respectively); (d) TSV cross-section (diameter: 30 μm); (e) photographs of the assembled TTV; (f) silicone gasket sealing between TTV and manifold; and (g) schematic of the cooling loop and manifold. The chips and cap have a footprint of 10 mm × 10 mm and a height of 300 μm.

Backside processing involved wafer thinning to 300 μm to expose TSVs, deposition of a 2 μm oxide passivation layer, and fabrication of micro-pin fins by deep reactive ion etching. Cu/Ni/Au UBMs were also patterned for stacking. The carrier wafer was then removed, and the dies were diced and assembled. Chip 1 and Chip 2 were stacked by flip-chip bonding, while the Cap and Chip 2 were bonded with sidewall epoxy (Figs. 1(a, e)).

The TTV was integrated with a manifold featuring a bottom cavity and sealed using an elastic, self-adhesive silicone gasket (Fig. 1(f)). The manifold cavity was CNC-machined with precise dimensional control, and the gasket thickness was slightly larger than the gap between the TTV and manifold to ensure effective compression and prevent bypass flow. The manifold was connected to a closed-loop cooling system (Fig. 1(g)), with deionized water as coolant.

A gear pump (Fluid-o-tech FG204) drove the flow, monitored by a McMillan 105 flowmeter (accuracy ±0.1%). Inlet/outlet temperatures were measured with type-T thermocouples (accuracy ±0.4%), and pressures with Omega PX409-015-G10V transducers (accuracy ±0.08%). The RTDs were calibrated in a hot oven for the coefficient $\alpha = \frac{R-R_0}{R_0(T-T_0)}$. The measurement accuracies for the resistance and the oven reference thermometer are ±0.008% and ±0.2%, respectively, resulting in an overall RTD accuracy of ±0.2%. Additional details of the uncertainty analysis are provided in [8].

During testing, the flowrate was maintained constant while chip power was incrementally increased. Temperatures and pressures were continuously monitored until the onset of two-phase cooling was observed.

III. Results and Discussion

Fig. 2 presents the cooling performance at a flowrate of 685.3±1.6 mL/min. Chip power was adjusted by increasing the supply voltage, with maximum powers of 126 W and 136 W achieved for Chip 1 and Chip 2, respectively. As expected, chip temperatures rose with power, and RTD 2 (near the outlet) consistently measured higher temperatures than RTD 1. Chip 1 exhibited higher temperatures than Chip 2, as it receives only single-side cooling, whereas Chip 2 benefits from double-side cooling by coolant passing through both chips. This configuration significantly enhances Chip 2's thermal performance, yielding a higher heat transfer coefficient h ($h = Q/A\Delta T$, where Q is the heat power, A is the chip bottom surface area, and ΔT is the logarithmic mean temperature difference). The coefficient of performance (COP), defined as the ratio of total heat power to the product of pressure drop and flowrate, also increases with heat power.

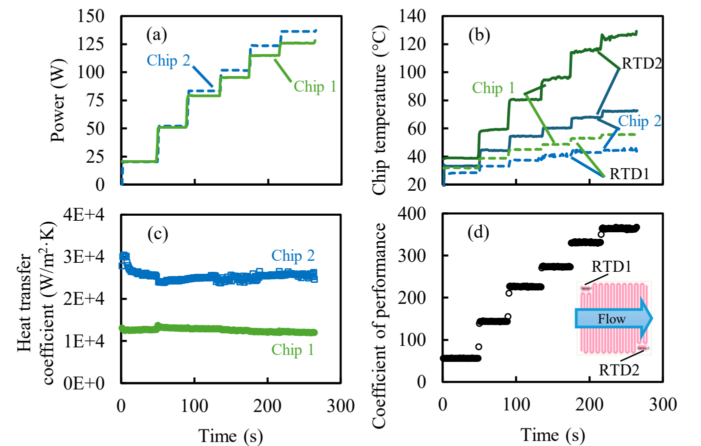

Fig. 2. Cooling performance over time at a coolant flowrate of 685.3±1.6 mL/min: (a) Power, (b) chip temperature, (c) heat transfer coefficient, and (d) coefficient of performance. The first and second terms of the flowrate represent the average and standard deviation of the measured flowrate during the test, respectively. This definition applies throughout this letter.

Fig. 3 shows the relationship between chip temperature and heat power at various flowrates. Chip 2 consistently

maintains lower temperatures than Chip 1. Its RTD readings scale linearly with heat power, indicating single-phase cooling. In contrast, RTD 2 of Chip 1 shows a nonlinear rise beyond 100°C, signaling the onset of two-phase cooling. This is further supported by the temperature fluctuations observed in RTD 2 (Fig. 4), while RTD 2 of Chip 2 remains stable.

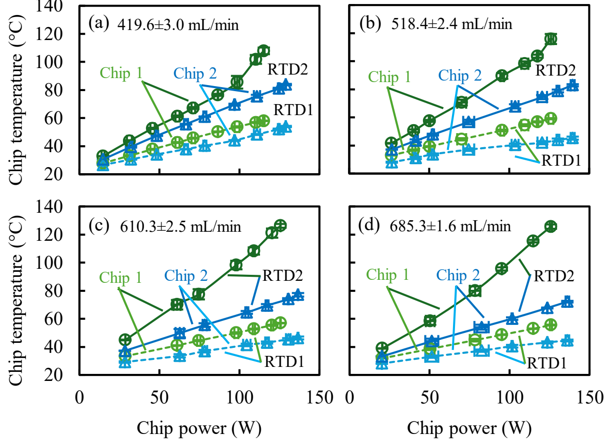

Fig. 3. Maximum chip temperature versus chip power at coolant flowrates of (a) 204.9±0.6 mL/min, (b) 304.4±1.6 mL/min, (c) 518.4±2.4 mL/min, and (d) 685.3±1.6 mL/min.

Temperature fluctuations in RTD 2 during two-phase cooling are undesirable as they may induce local overheating. To mitigate this, a degas module was employed prior to the experiment to remove dissolved air, thereby minimizing bubble size and stabilizing the boiling process. As shown in Fig. 4, Chip 2 maintains steady temperatures under single-phase conditions, while Chip 1 exhibits only ±3.2°C fluctuations in the two-phase regime, substantially reduced compared to non-degassed cases [22], [23].

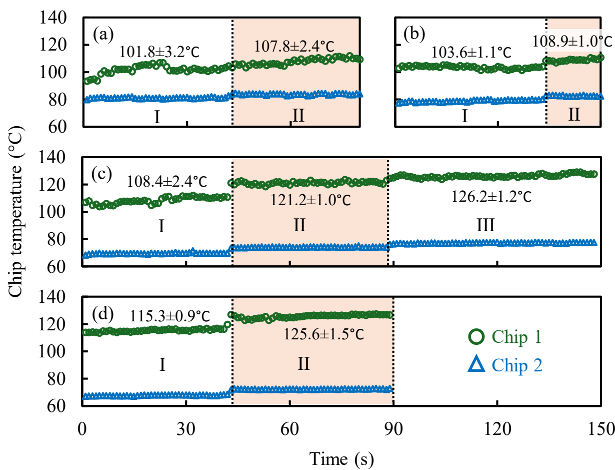

Fig. 4. Temperature fluctuations (RTD2) in the two-phase regime at different flowrates: (a) 419.6 mL/min (I: 110.3/124.6 W, II: 115.2/128.9 W), (b) 518.4 mL/min (I: 117.2/130.4 W, II: 126.0/139.7 W), (c) 610.3 mL/min (I: 109.0/117.3 W, II: 120.4/130.5 W, III: 125.7/136.6 W), and (d) 685.3 mL/min (I: 114.8/123.6 W, II: 125.9/136.2 W). Power values shown as Chip 1/Chip 2; all measurements: flowrate ±3 mL/min, power ±1.5 W max.

The heat transfer coefficient (h) further highlights performance differences (Fig. 5(a)). Chip 2 achieves 1.2-2.0 times greater h values than Chip 1 due to double-side cooling. Flowrate optimization involves a key trade-off: increasing flowrate from 127.9 mL/min to 685.3 mL/min improves h by 2.9-5.0 times (from 4,400-5,100 W/m^2·K to 12,600-25,500 W/m^2·K) but also increases pressure drop by 18.2 times (from 3.4 kPa to 62.7 kPa) (Fig. 5(b)). As shown in Fig. 5(c), COP decreases with flowrate but increases with heat power, underscoring the need for system-level optimization to balance cooling performance against pumping efficiency.

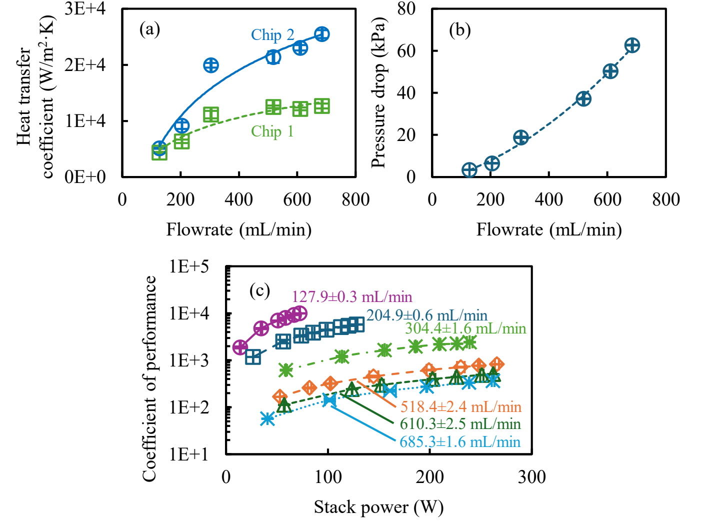

Fig. 5. (a) Heat transfer coefficient and (b) pressure drop versus flowrate. (c) Coefficient of performance versus stack heat power at different flowrates.

IV. Conclusion

This study demonstrates that a two-phase liquid cooling approach with backside-embedded micro-pin fins can effectively address thermal challenges of stacked high-power 3D ICs. Experiments show stable operation with minimal temperature fluctuations (±3.2°C) in the two-phase regime, validating the method's practicality. Chip 2's superior performance, enabled by double-side cooling, highlights the importance of cooling strategy in multi-chip stacks. Although higher flowrates improve thermal performance, they concurrently increase pressure drops, necessitating system-level optimization based on the coefficient of performance. Future work will focus on adapting this approach for integration into functional chip architectures and advanced packaging schemes.

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