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Reconfigurable High-Performance Memristors Based on Few-layer High-κ Dielectric Bi_2SeO_5 for Neuromorphic Computing

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Abstract

Memristors are pivotal for energy-efficient artificial intelligence (AI) hardware, potentially eliminating the von Neumann bottleneck by in-memory realizations of synaptic operations. However, the dynamic requirements of neuromorphic computing on specific electronic devices poses reliability and universality challenges, limiting progress toward more widely applicable computing platforms. Here, we successfully demonstrate a two-dimensional (2D) high-κ dielectric-based memristor with the desired reconfigurable resistive switching behavior. Utilizing a few layered Bi_2SeO_5 possessing excellent electrical insulation properties as the switching medium, the device features a low operating voltage (~ 0.5 V), low operation current (10 pA), long memory retention (>10^3 s), large switching window (~ 10^8), steep slope (<1 mV/dec), fast switching speed (40 ns), and low energy dissipation (~ 1 pJ). The switching characteristics between volatile and non-volatile memory can be achieved on demand by

regulating compliance currents, offering the possibility of implementing multiple neural computational primitives. A simulated convolutional neural network (CNN) based on long-term potentiation/depression (LTP/D) achieves 85% accuracy in complex image recognition. Furthermore, MNIST and fashion-MNIST recognition with built reservoir computing (RC) utilizing volatile behaviors reach 97% and 85% accuracy, respectively. This work opens new opportunities for 2D high-κ dielectrics in next-generation AI hardware with enhanced energy efficiency and computational versatility.

1. Introduction

To propel the ongoing advancement of machine learning and artificial intelligence (AI) technologies, there is an urgent need for efficient data storage and computing paradigms to address the fundamental limitations of von Neumann computing, such as memory bottlenecks, high energy consumption, and latency due to frequent data shuttling between storage and processing units.[1] Neuromorphic compute-in-memory (CIM) approaches have emerged as a promising alternative, with a wide range of memory devices being extensively explored for the physical implementation of neuromorphic CIM platforms.[2, 3] Among them, resistive random-access memories (RRAMs) are noted due to their superior scalability, high integration density, low fabrication cost, and seamless compatibility with existing complementary metal-oxide-semiconductor (CMOS) back-end-of-line (BEOL) process.[4] RRAM has been strategically earmarked by the International Technology Roadmap for Semiconductors (ITRS) as a key candidate for the next generation of memory technologies.[5]

However, as the device scales down, cell capacitance decreases rapidly, which in turn results in a significant increase in the forming voltage, adversely affecting the reliability and performance of the memory device.[6] Therefore, dielectric materials with higher dielectric constants are needed to store sufficient charge for reliable bit operation and to increase integration density while reducing power consumption. Conventional amorphous dielectrics, including materials such as AlO_x and HfO_x, are hindered by high interface trap states and surface dangling bonds.[7] In addition, the dielectric parameters of these materials become unstable when their thickness is reduced to a critical value or subjected to increased stress, which is not conducive to stacked, high-density three-dimensional (3D) integration.[8] The development of novel 2D materials with high dielectric constants, atomically flat and dangling-bond-free surfaces undoubtedly provides the high-quality interfaces in the devices and brings advantages of suppressing leakage currents,[9] further contributing to low energy consumption memristors and efficient neuromorphic computing. Recently, as a novel van der Waals (vdW)

layered dielectric material with excellent insulating properties like high dielectric constant (ε_r > 20), low leakage current density (~0.015 A·cm^{-2}), ultralow equivalent oxide thickness (EOT) of 0.3 nm, and good environmental stability, 2D Bi_2SeO_5 has attracted great research attention,[10-12] opening up new possibilities for fast ion migration and steep, energy-efficient resistive switching. Unlike h-BN or other 2D vdW insulators, the ε_r of Bi_2SeO_5 is predominantly governed by its ionic composition. As a result, the high ε_r remains nearly constant even with the reduction in thickness up to the monolayer and/or variations in stress within 6%,[10] making it highly favorable for integrated circuits with high density. Peng et al. recently demonstrated wafer-scale Bi_2O_2Se/Bi_2SeO_5 heterostructure arrays,[12] marking a significant advancement toward practical deployment of this high-performance material system. Furthermore, despite CIM promises significant advancements in general-purpose AI due to its superior energy efficiency, existing devices are often tailored for specific, stationary applications and lack the versatility to adapt to dynamic computational demands.[13-14] This limitation diminishes the flexibility of bionic hardware in ever-changing scenarios, highlighting the need for reconfigurable neuromorphic capable of performing diverse brain-inspired functions.[15-17]

In this study, we demonstrate a reconfigurable memristor based on few-layer high-κ dielectric Bi_2SeO_5. Taking advantage of the superior electrical insulation properties and high-quality interface of the Bi_2SeO_5, the sandwich $Ag/Bi_2SeO_5/Au$ device exhibits outstanding forming-free resistive switching behaviors, characterized by a low operating voltage (~ 0.5 V), low operation current (10 pA), long memory retention time (>10^3 s), a large switching window (~ 10^8), a steep slope (<1 mV/dec), fast switching speed (40 ns) and low energy dissipation (~ 1 pJ). By modulating current compliance (I_{cc}) during the SET process, switching characteristics between volatile and non-volatile memory can be selectively achieved on demand. The coexistence of volatile and nonvolatile functionalities allows for the mimicry of short- and long-term synaptic plasticity, underscoring its potential for applications in RC and CNN. This capability facilitates the integration of multiple computational primitives onto a single chip within the same hardware substrate. Simulations of the constructed CNN and physical reservoir system evaluate the device's good performance in recognizing complex images, providing an innovative platform for simple, versatile neuromorphic applications in the field of electronics.

2. Results and discussion

Bi_2SeO_5 crystallizes in an orthorhombic lattice with a space group of *Abm*2 (a = 11.42 Å, b = 16.24 Å, c = 5.49 Å, Z = 8).[11] It is characterized by a vdW layered structure with a covalently saturated surface along the [100] direction. Each unit cell contains eight formula

units, assembled through vdW layered stacking along the c-axis.[11] **Figure** 1a illustrates the front, side, and top views of the Bi_2SeO_5 structure. The thickness of a monolayer Bi_2SeO_5 is about 11.47 Å.[10] As shown in **Figure** 1b, the indirect bandgap of layered Bi_2SeO_5 is approximately 2.82 eV, indicated by density functional theory (DFT) calculations. In addition, the bandgap of Bi_2SeO_5 was also experimentally determined by ultraviolet-visible (UV-vis) absorption spectroscopy in a single crystal, as depicted in **Figure** S1, where the absorption sharply drops after 330 nm. High-quality Bi_2SeO_5 crystals with typical dimensions in the centimeter scale were synthesized using the Chemical Vapor Transport (CVT) method (inset in **Figure** 1c). X-ray diffraction (XRD) analysis substantiates the high quality and single crystallinity of the Bi_2SeO_5 crystals (**Figure** 1c). The XRD pattern exhibits strong and sharp (h00) signals without other diffraction peaks, confirming the crystallinity and the preferential orientation of the sample, and the results are in good agreement with the standard diffractogram of Bi_2SeO_5 without the impurity phases. Clear signals for the elements Bi, Se, and O were detected by energy-dispersive X-ray spectroscopy (EDX) in a scanning electron microscope (SEM) (**Figure** 1d). Quantitative analysis revealed that the atomic ratios of Bi, Se, and O were 2:1:5. EDS element mappings confirmed the homogeneous distribution of these three elements. The characteristic peaks of Bi, Se, and O in the X-ray photoelectron spectroscopy (XPS) are displayed in **Figure** 1e and **Figure** S2 respectively. The peaks for Bi at 159.0 eV (4f7/2) and 164.3 eV (4f5/2) are consistent with previous reports,[18] suggesting that the bismuth valence state is maintained at +3 in the natural oxide. The peaks for Se 3d located at approximately 59.5 eV and 58.7 eV respectively, are indicative of Se^{4+} within the sample. The O 1s peak appears at 530.9 eV, corresponding to lattice oxygen species. Quantitative XPS analysis reaffirms the stoichiometric ratio of Bi, Se, and O to be 2:1:5. These results demonstrate the acquisition of high-quality Bi_2SeO_5 crystals. The low cleavage energy (~ 26 meV· $Å^{-2}$) facilitates the easy mechanical exfoliation of large-area flat nanosheets from bulk Bi_2SeO_5 onto the target substrate.[11] **Figure** 1f displays the optical image of a mechanically exfoliated Bi_2SeO_5 nanosheet embedded in Polydimethylsiloxane (PMDS) and transferred onto a SiO_2/Si substrate, with the sample exhibiting a typical lateral dimension exceeding 100 μm. **Figure** 1g shows that the thickness of the Bi_2SeO_5 nanosheet is approximately 7.1 nm (~ 6 layers), with a clean and smooth interface. The close-up high-resolution TEM (HRTEM) image and the corresponding selected area electron diffraction (SAED) pattern reveal a d-spacing of 0.273 nm for the (002) plane in few-layer Bi_2SeO_5. The sample is well crystallized into a tetragonal crystal lattice.

Figure 2a and **Figure** S3 depict a schematic illustration and an optical image of the fabricated vertical memristor cross-point array based on a few-layer Bi_2SeO_5. A 30 nm thick

inert Ni/Au layer was deposited as the bottom electrode, and a 60 nm thick electrochemically active Ag layer was deposited as the top electrode. The systematic electrical measurements for Ag/Bi_2SeO_5/Au device are present in **Figure** 2. **Figure** 2b illustrates the typical direct current (DC) dual sweep characteristics of the device across a voltage range from 0 to 1.5 V, with a compliance current (I_{cc}) limit set to 1 μA. An abrupt switching was observed in devices to occur at voltages as low as 0.2 V, which stands well below the targeted sub-1 V switching threshold for random access memory (RAM) devices specified in the International Roadmap for Devices and Systems (IRDS).[19] Extracting and fitting the Gaussian equation from **Figure** 2b yields a smaller average V_{set} of 0.3 V (coefficient of variation C_V = 13 %) (as shown in **Figure** S4), leading to potentially low energy consumption in the application. The observed abrupt switching behavior suggests the presence of an electrochemical metallization filament-type switching phenomenon. To evaluate the robustness and reproducibility of our devices, the resistive switching behavior and cycle-to-cycle (C2C) and device-to-device (D2D) variability of 30 fabricated Ag/Bi_2SeO_5/Au devices were shown in **Figure** S5. These devices exhibit cycling stability and consistency. Under an I_{cc} of 1 μA, the switching characteristic exhibits volatility; specifically, once the applied bias is removed, the low-resistance state (LRS) rapidly transitions back to the high-resistance state (HRS), further proving the volatile nature, which is due to the spontaneous dissolution of weak Ag-conducting filaments. The HRS maintains a high value of ~ 10^{13} ohms, which significantly contributes to an on/off ratio of up to 10^7 (**Figure** S4). The substantial resistance in the HRS offers several benefits, such as reduced power consumption, elimination of parasitic sneak currents, lower operating current, and the ability to achieve high on/off ratio across multiple conductance levels. A very steep switching slope of 1 mV per decade was observed, providing the advantage of an immediate response to the applied voltage (**Figure** S4). This results in a distinct variance in electron flux based on the threshold value. The device exhibits small resistance fluctuations and excellent cyclic stability in DC stress cycling performance over 50 cycles. This highlights the robustness of the device in maintaining consistent electrical characteristics throughout the testing process (**Figure** 2b). **Figure** 2c presents a series of multi-level *I-V* characteristics, illustrating the device's versatility in response to varying I_{cc}. Notably, a total of 11 distinct multi-level states are realized, each corresponding to unique operating conditions at different I_{cc}. The operating current of the memristor can each achieve an ultralow level of 10 pA. This value significantly undercuts the typical operating currents reported for traditional chalcogenide-based memristors, transition metal oxide memristors, and most 2D material-based memristors. Such a remarkably low current highlights potential for low-power consumption applications. A switching time of 40

ns, measured through subjecting to a voltage pulse with an amplitude of +1 V and a width of 700 ns, indicates the fast-switching speed (**Figure** 2d).

When the set I_{cc} is elevated to 1 mA, the device transitions to a non-volatile switching state. As indicated in **Figure** 2e, a positive bias applied to the top Ag electrode sets the device to LRS, whereas applying a negative bias resets our memory cell to HRS. Specifically, the application of applying a positive SET bias of +1 V transitions the device from HRS to LRS and retains this state after the voltage is removed. Conversely, a RESET bias of −1 V converts the device from LRS back to HRS and maintains its state thereafter. Switching between volatile and non-volatile modes in these Ag/Bi_2SeO_5/Au devices can be controlled by adjusting the I_{cc}. The I_{cc} value is critical in determining the lifetime of the Ag conductive filaments; higher I_{cc} levels lead to stronger and thicker filaments, thereby extending the retention time of LRS and vice versa. The underlying physical mechanism responsible for this nonvolatile switching in the Bi_2SeO_5 memory cell is explored in depth subsequently. A very large memory window approaching 10^8 was observed, with some devices even showcasing memory windows exceeding 10^{10}, demonstrating exceptional performance. **Figure** 2f displays representative testing results over 50 cycles. During the cyclic resistive switching process, a median SET voltage of 0.5 V and a RESET voltage of −0.6 V were recorded. **Figure** 2g presents the cumulative probability distribution of the SET and RESET voltages, which span between +0.3 and +0.7 V and −1.0 V to −0.5 V, respectively. These findings demonstrate reliable resistance switching with consistent performance across the tested voltage ranges. To further evaluate the uniformity and thickness dependence of device performance, we systematically characterized multiple Bi_2SeO_5 devices with varying thicknesses. Atomic force microscopy (AFM) measurements were carried out on Bi_2SeO_5 films with four distinct thicknesses (8.3 nm, 10.1 nm, 12.5 nm, and 20.2 nm), labeled as devices 1 to 4, as shown in **Figure** S6. Devices with different thicknesses demonstrate comparable volatile and nonvolatile switching characteristics. The switching ratios and set/reset voltages are close across four groups (see **Figure** S7). **Figure** 2h illustrates that the Bi_2SeO_5 memristor maintains highly stable resistance states for both the LRS and HRS over 1000 s with a 0.1 V reading voltage and ±2 V pulsed voltages. The power consumption of the device was calculated to be 1.16 pJ per switching, which is comparable or lower than that of most 2D materials, including MoS_2/MoO_x, $CuInP_2S_6$, $MoTe_2$, Bi_2O_2Se, and WSe_2/WO_x, as well as bulk materials like Ta_2O_5, SiO_2, and $Zr_{0.5}Hf_{0.5}O_2$.[20-27] **Figure** 2i provides a comprehensive comparison of the switching speed and energy performance of several previously reported memristors.[7, 20-31] Evidently, our device demonstrates good performance, characterized by a fast switching speed of 40 ns, a minimal energy dissipation of about 1.16 pJ, a high on/off ratio

close to 10^8, a steep switching slope of less than 1 mV/dec, and a low set/reset voltages of less than ±1 V. Although mechanical exfoliation−enabled by the low cleavage energy of Bi_2SeO_5 (~26 meV· $Å^{-2}$) is well suited for rapid device prototyping, it inevitably yields flake-to-flake thickness variations and lateral dimension constraints that limit uniformity. To address these scalability challenges and facilitate wafer-scale device integration, a viable route is the chemical vapor deposition (CVD) of Bi_2O_2Se nanoflakes from Bi_2Se_3 and Bi_2O_3 precursors, followed by a controlled, room-temperature O_2 plasma treatment that converts the as-grown Bi_2O_2Se into continuous Bi_2SeO_5 films. Drawing on recent demonstrations of wafer-scale Bi_2O_2Se/Bi_2SeO_5 heterostructures,[12] to achieve large-area uniformity and reproducible device performance for accelerating practical toward hardware-array integration.

Since the top electrode is electrochemically active Ag, the resistance switching mechanism in Bi_2SeO_5 memristor may be the formation of Ag conductive filaments. The volatile or nonvolatile behavior is dependent on the capability in sustaining conducting filaments (CFs) in the LRS (**Figure** 3a-c).[14] The thickness and lifetime of CFs can be effectively controlled by adjusting the value of I_{cc} in Bi_2SeO_5. The relationship between I and V is plotted by linear curve fitting, revealing that the conduction mechanism adheres to the space charge limited conduction (SCLC) theory (**Figure** S8).[32] The slopes of the LRS during the SET and RESET processes are nearly equal to 1, suggesting that the conduction mechanism aligns with ohmic conduction (**Figure** S8). For the HRS, in the low voltage region, where the impact of the electric field is minimal, and the quantity of injected charge carriers is significantly less than the number of thermally generated free charge carriers. This results in Ohmic conduction in the device, which is reflected in the nearly identical slope of 0.989 for the SET process and 0.93 for the RESET process.[32] As the applied voltage increases, the density of injected charge carriers gradually increases until it surpasses the number of thermally generated carriers.[28] At this point, the injected charge carriers gradually transition into free carriers, allowing them to move within the resistive layer. From the analysis of the conduction mechanism of the device, the resistive switching behavior indeed depends on the conductive filament mechanism. To confirm the Ag permeation, cross-sectional (CS)-TEM images of the memristors were collected. **Figures** 3d and 3e display the CS-TEM images of a pristine $Au/Bi_2SeO_5/Ag$ memristor. Bi_2SeO_5 exhibits a distinct vdW gap and a layered structure with a interlayer spacing of ~1.17 nm. Upon the memristor is SET to LRS after multiple memristive switching cycles, distinct Ag filaments become clearly visible. The conductive filaments outlined by dotted white lines were observed in the CS-TEM image (**Figure** 3f-h). The Ag conductive filament model is schematically illustrated in **Figure** 3a-c. The Ag (111) plane and Ag (200) was observed near the interface

between Ag TE and Bi_2SeO_5 layer (**Figure** 3i). These results further prove that the resistance switching mechanism in Bi_2SeO_5 memristor is attributed to the formation and dissolution of Ag conductive filaments, induced by the electrochemically active Ag top electrode.

To facilitate the implementation of synaptic functions for neuromorphic computing, the presence of multilevel conductance states is highly desirable. We further explored the feasibility of synaptic emulation in Bi_2SeO_5-based memristor. The electrical impulses used here as biological spikes conveyed between different neurons, and the changes in device conductance effectively simulates the synaptic weight update occurring between two neurons (**Figure** 4a).[3] **Figure** S9 shows the excitatory postsynaptic current (EPSC) or inhibitory postsynaptic current (IPSC) stimulation under positive and negative voltage pulses in this device. **Figures** 4b and 4c depict the synaptic weight update, highlighting the processes of potentiation and depression, as a function of the continuous application of pulses. The LTP and LTD process is composed of 100 identical positive pulses and 100 identical negative pulses. Under positive-pulse excitation increases, the conductance steadily increased, thereby mimicking the synaptic potentiation process. Conversely, under negative-pulse stimulation, the conductivity gradually decreases, thus replicating the synaptic inhibition process, demonstrating the effective modulation of the device conductance through electrical pulses. Subsequently, the reproducibility of the training effect was assessed. As illustrated in **Figure** 4d, the normalized LTP/D conductance exhibits small fluctuations across 40 consecutive cycles (each cycle consisting of 100 positive and negative pulses), substantiating the high C2C stability of the Bi_2SeO_5 memristor. The LTP/D curves were fitted as follows:[33]

$$G_{LTP} = B(1-e^{-P/A}) + G_{\min}$$

$$G_{LTD} = B(1-e^{(P-P_{\max})/A}) + G_{\max}$$

$$B = (G_{\max} - G_{\min}) / (1-e^{-P_{\max}/A})$$

where G_{LTP} and G_{LTD} represent the conductance values associated with LTP and LTD processes, respectively. G_{min}, G_{max}, and P_{max} are the minimal conductance, maximal conductance, and maximal level of conductance, respectively. A is a parameter that regulates the nonlinear behavior of the weight update process. And A is 0.1088 for LTP and −0.5395 for LTD. The calculated nonlinearity for LTP and LTD are 5.57 and -3.98, closely approximating the ideal symmetric case. [33] These results highlight the outstanding LTP and LTD characteristics of our device. Taking advantage of the exceptional long-term plasticity, an image recognition task was performed using a CNN for evaluation.[34] **Figure** 4e and **Figure** S10 schematically illustrate a neural network hardware system consisting of a Bi_2SeO_5 memristors crossbar array. This 2×9

array can be utilized to construct a 3×3 convolutional kernel for feature extraction in image processing. In this configuration, pairs of memristors function as a differential unit, representing positive and negative conductance values to encode synaptic weights. The multiplication and summation of V_i and G_i involved in the convolution operation, that is $I^{+(-)} = \sum_{i=1}^{n} V_i \times G_i^{+(-)}$ and $I_{out} = I^+ - I^-$, can be efficiently implemented using the crossbar array.[33] **Figure** 4f illustrates the architecture of a VGG-8 CNN designed for image recognition using the (Canadian Institute for Advanced Research) CIFAR-10 dataset.[35] Our memristive devices were simulated on the NeuroSim platform to assess their performance in CNN hardware implementations (see **Supplementary Note 1** for details). **Figure** 4g displays the simulation outcomes, where the Bi_2SeO_5 memristor achieves a complex image recognition accuracy of 84.5% after 20 training epochs. These experimental findings emphasize the learning capability of 2D high-κ memristors and their potential for high-performance neuromorphic computing applications. Furthermore, to ensure the practical scalability of the crossbar array, it is essential to address sneak-path currents that arise when unselected cells form unintended low-resistance pathways. In the most adverse case—one HRS cell surrounded by LRS cells—there can be $(N-1)^2$ parallel leakage paths, degrading read fidelity and energy efficiency. A proven strategy to suppress such parasitic currents is the integration of a one-transistor–one-resistor (1T1R) or one-selector–one-resistor (1S1R) architecture.[36-40] Specifically, by pairing each Bi_2SeO_5 memristor with a complementary Bi_2O_2Se field-effect selector, one can leverage the high carrier mobility and excellent subthreshold characteristics of Bi_2O_2Se to mitigate sneak currents until the desired read or write voltage is applied. Implementing such 1T1R/1S1R configurations will be favorable for realizing large-scale, high-density neuromorphic arrays with both low leakage and high operational reliability.

Finally, we demonstrated RC based on the short-term plasticity behavior (i.e., volatility) of the Bi_2SeO_5 memristor. The RC system is a powerful paradigm for efficiently processing time-related and sequence inputs.[41,42] As shown in **Figure** 5a, the architecture of RC system contains an input layer, a physical reservoir layer, and an output layer. In RC, temporal inputs are transmitted through a network of neurons with random and nonlinear connections, which can subsequently be decoded using a simple readout algorithm.[43] **Figure** S11 shows the short-term plasticity after applying a pulse train of 0.4 V, 40 μs. **Figure** 5b presents the 3-bit dynamic responses of the memristor, where each input voltage pulse represents one bit, with "1" and "0" indicated by the presence and absence of a pulse, respectively. The 3-bit patterns were converted into a pulse stream featuring 8 unique

combinations ranging from "000" to "111," and all 8 states are clearly distinguishable. **Figures** 5c and 5d demonstrate the use of the MNIST dataset and the fashion-MNIST (f-MNIST) dataset for handwritten digit recognition and image recognition. The MNIST dataset comprises 60,000 training images and 10,000 test images, each with a resolution of 28×28 pixels. To integrate the MNIST images into the 3-bit RC system, the images from the MNIST dataset were further cropped and binarized. The simulated outputs of a typical digit “0” and “Sneaker” image were present in **Figures** 5c and 5d, respectively. **Figure** 5e shows an accuracy of 97.03% was achieved after 50 training epochs, and the confusion matrix indicates an overall accuracy of 96.9% across all 10 classes in the MNIST dataset. In addition, the training accuracy for image pattern recognition reaches 86.6% across all 10 categories of the f-MNIST dataset (as shown in **Figure** 5f). Furthermore, we modeled possible realistic D2D and C2C variations by superimposing Gaussian-distributed noise with a pre-specified standard deviation (σ) onto each reservoir’s output current. Owing to the stochastic nature of this noise, there is a small probability that the current may momentarily drop to extremely low values. **Figure** S12 and **Figure** S13 depict the overall accuracy as a function of σ. Even at a relatively high σ of 0.2, the accuracy declines only marginally, underscoring the system’s robust resilience to device noise and variability. The error bars further highlight minimal variation between cycles of different simulation runs (10 trials) (see **Supplementary Note 2**).

3. Conclusion

In summary, few-layer Bi_2SeO_5 based 2D high-κ memristors are fabricated, demonstrating good performance resistance switching behavior. Benefiting from the excellent electrical insulation properties of Bi_2SeO_5, the device exhibits a low operating voltage (~ 0.5 V), ultra-low operation current (~10 pA), long memory retention time (>10^3 s), a large switching window (~ 10^8), steep slope (<1 mV/dec), fast switching speed (40 ns), and minimal energy dissipation (~ 1 pJ). By modulating the compliance current to control Ag filament variation, the device enables on-demand switching between volatile and non-volatile memory characteristics, offering the possibility of implementing multiple computational primitives in neural networks. Key synaptic features, such as LTP/D and short-term plasticity, are successfully emulated, further confirming the great potency of 2D Bi_2SeO_5 for deployment in complex computing of hardware neural networks.

Although 2D high-κ memristor synaptic devices hold a bright future in neuromorphic computing, they are still in their infancy, with several challenges that need to be overcome to fully unlock their advantages. Concerns remain about device reliability and integration, with a

lack of integration may limit the accuracy of complex information recognition. Future efforts may prioritize the incorporation of 1T1R and 1S1R configurations to suppress sneak-path currents in densely packed arrays, thereby enhancing scalability and operational robustness. Additionally, achieving generalizability and developing scalable, cost-effective, and reproducible technologies with universally applicable protocols for practical applications. Looking ahead, this exciting topic requires further research to bridge the gap between AI technology and the potential-filled 2D material.

5. Experimental Section

Materials characteristics: Bi_2SeO_5 bulk crystals were synthesized by the CVT method. 2D Bi_2SeO_5 nanoflakes were mechanically exfoliated from the Bi_2SeO_5 bulk crystals. The electronic properties of Bi_2SeO_5 were calculated by first-principles calculations within the framework of DFT employing the Vienna Ab initio Simulation Package (VASP). The DFT calculations were performed using the projector-augmented wave (PAW) pseudopotentials under the generalized gradient approximation (GGA). XRD (SmartLab SE) was utilized to reveal the crystal structure. The elemental composition and proportions were characterized using EDX in a SEM (FEI Inspect F50). XPS (Thermo Kalpha) was employed to determine the chemical composition and valence states. Surface morphology and thickness were investigated using an optical microscope (BX41M-LED) and an atomic force microscope (Dimension ICON). HRTEM (Talos F200X) and SAED were used to further elucidate the crystal structure.

Device Fabrication: The bottom electrode (Ni/Au, 5/30 nm) was fabricated using standard electron beam lithography (EBL) followed by thermal evaporation and lift-off in acetone. Few-layer Bi_2SeO_5 flakes, obtained via mechanical exfoliation from bulk crystals, were precisely aligned onto the pre-patterned electrodes using a polydimethylsiloxane (PDMS)-mediated dry transfer technique. Subsequently, the top electrode (Ag, 60 nm) was patterned via EBL and the Ag layer was deposited by thermal evaporation, thus completing the formation of the Au/Bi_2SeO_5/Ag device. The device was annealing in glove box for 2 hours. For electrical characterization, DC and pulsed voltage-sweep testing were carried out at room temperature utilizing a Keithley SCS4200/Agilent B1500A parameter analyzer, equipped with two remote pulse units connected via preamplifiers. The semiconductor parameter analyzer was connected to the bottom electrode (Au) and top electrode (Ag) through Au-coated tungsten probes.

Simulation: A customized physical reservoir computing simulation platform was built. The pulse train pattern of 0.4 V amplitude and 40 us duration was used to stimulate the reservoir node (Ag/Bi_2SeO_5/Au memristors), with current read at 0.1 V. A fully connected readout layer

was used for classifying the simulated memristors reservoir output, which was offline supervised trained with logistic regression (maximum-entropy classification) by stochastic average gradient (SAG) solver with L1 regularization. Fashion-MNIST dataset containing 70,000 images of fashion styles categorized into 10 classes was used for benchmarking the simulated PR system, where 60,000 was used for training and the rest 10,000 separated images were saved for validation. The static image was input into the dynamic PR row by row, with a simulated reset every 3 pixels. Each run in the simulation was independent. All simulation programs were exploited in Python 3.9 environment.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

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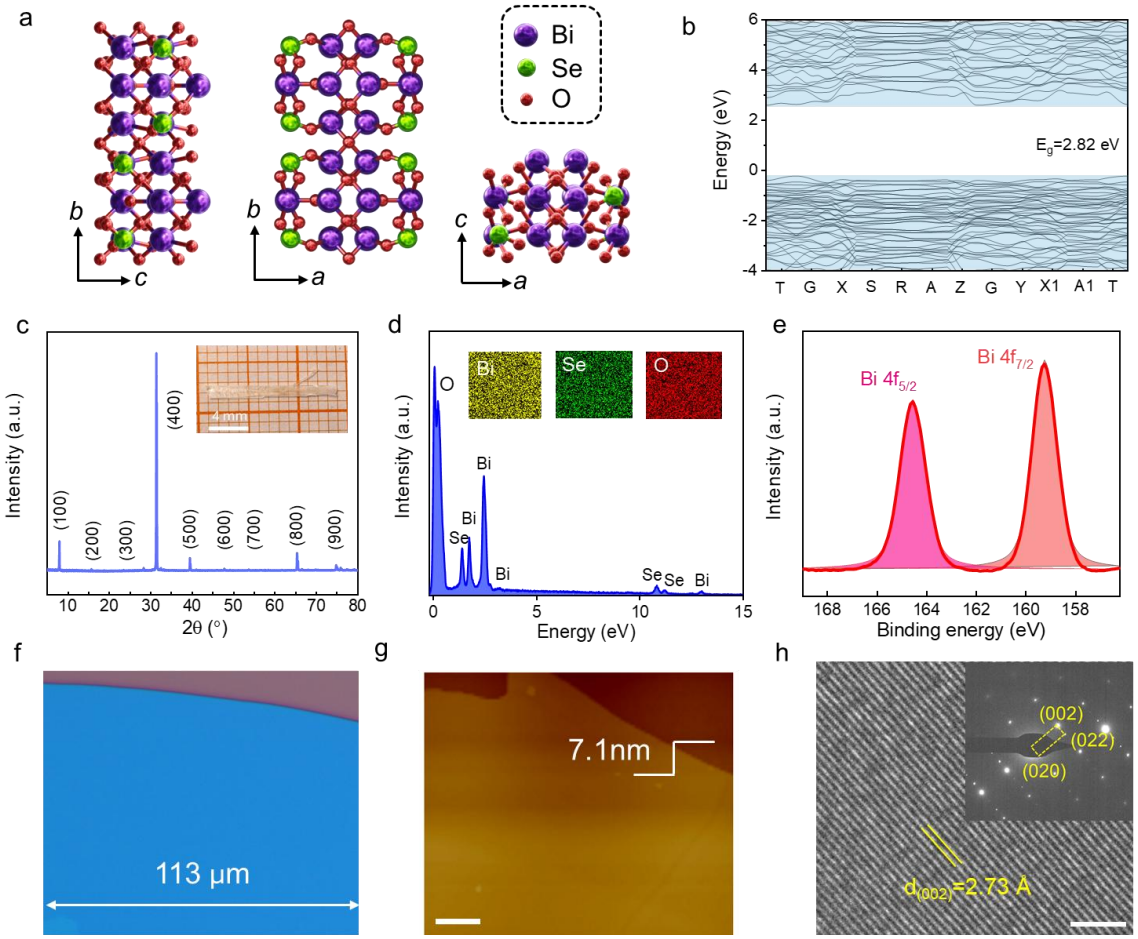

Figure 1. Characterization of Bi_2SeO_5. (a) The front, side, and top views of the Bi_2SeO_5 structure. (b) Calculated band structure of Bi_2SeO_5. (c) XRD patterns of a Bi_2SeO_5 single crystal flake. Insert: photograph of as-grown crystals. (d) EDS spectrum of Bi_2SeO_5 nanoflake. Inserts: EDS maps of Bi_2SeO_5 nanoflake. (e) XPS scans of representative fitted Bi $4f_{5/2}$ and Bi $4f_{7/2}$ spectra of the sample. (f) Optical image of mechanical exfoliated few-layer Bi_2SeO_5 in SiO_2/Si substrate. (g) AFM image of exfoliated few-layer Bi_2SeO_5 (Scale bar: 2 um). (h) HRTEM image and SAED pattern of the few-layer Bi_2SeO_5 (Scale bar: 1 nm).

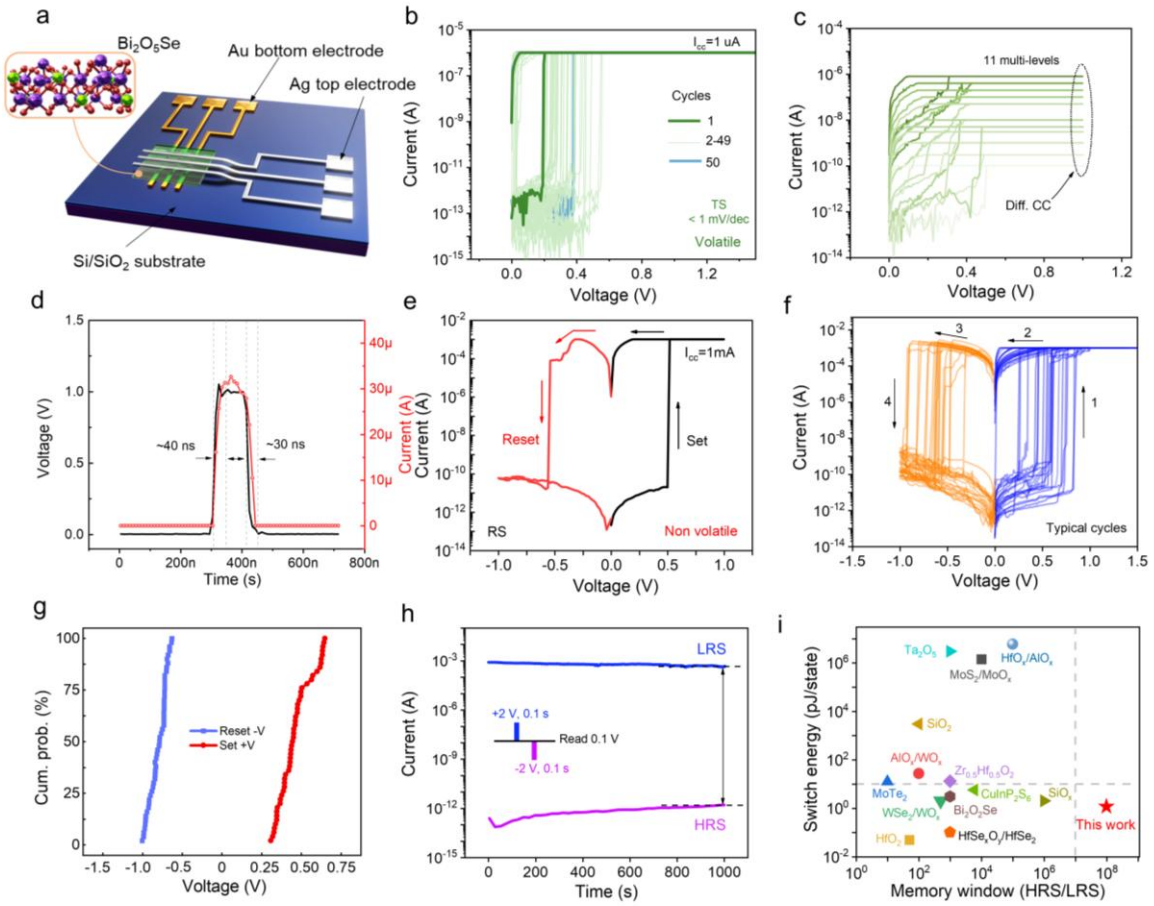

Figure 2. Coexistence of volatile and nonvolatile behavior in 2D Bi_2SeO_5. (a) The schematic diagram of the vertical memristor cross-point array based on a few-layer Bi_2SeO_5. (b) Typical volatile *I-V* dual-sweep characteristics of the device, exhibiting a threshold swing (TS) <1 mV/dec. (c) Multi-level *I-V* characteristics showing 11 distinct states modulated by I_{cc}. (d) Temporal response measured by applied of a voltage pulse with an amplitude of 1 V and a width of 150 ns. (e) Typical nonvolatile *I-V* dual sweep characteristics of the device. (f) Cyclic resistive switching process. (g) The cumulative probability distribution of the SET and RESET voltages for the Ag/Bi_2SeO_5/Au memristor. (h) Retention test with a 0.1 V reading voltage and $\pm$2 V pulsed voltages. (i) Benchmarks of switching energy and memory window in different memristors.

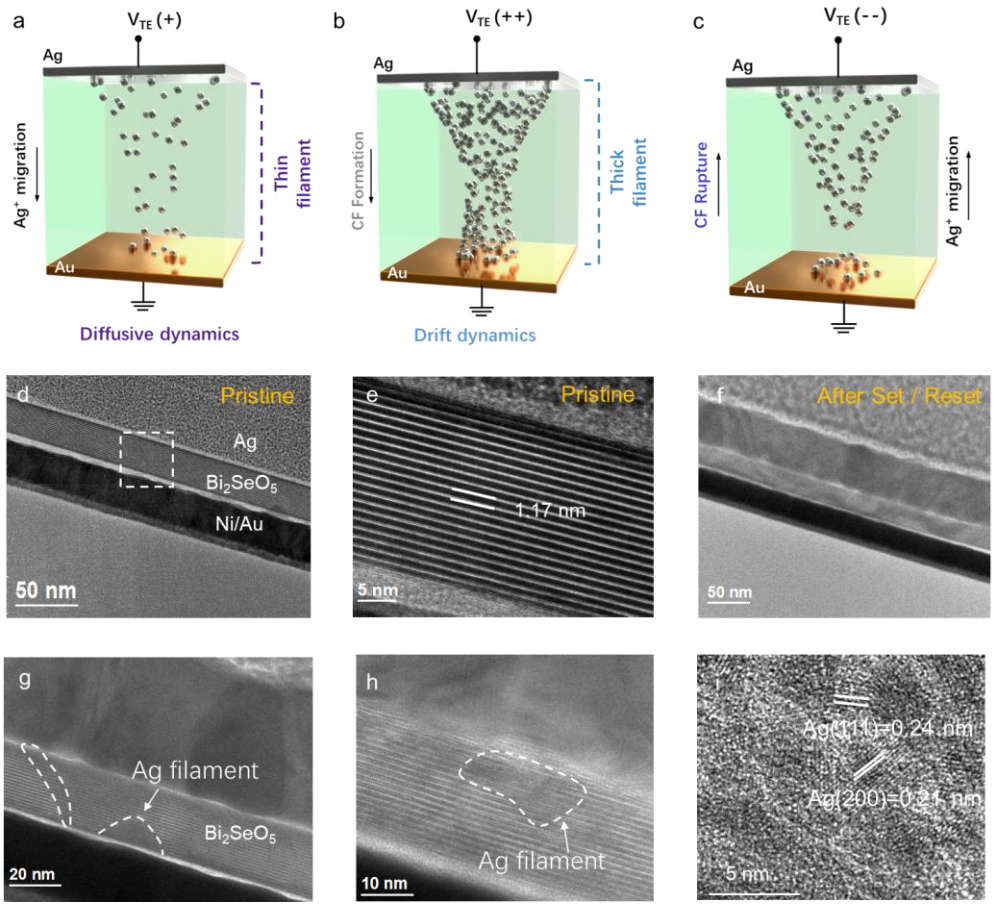

Figure 3. The resistance switching mechanism of the reconfigurable Bi_2SeO_5 memristor. (a) Schematic illustration of the volatile diffusive switching mechanism. (b, c) Schematic illustration of the non-volatile drift switching mechanism. (d, e) Cross-section TEM images of a pristine Au/Bi_2SeO_5/Ag memristor. (f-h) Cross-section TEM images of the Au/Bi_2SeO_5/Ag memristor after multiple memristive switching cycles and Ag conductive filaments outlined by dotted white lines. (i) The observed Ag(111) and Ag(200) in the memristor.

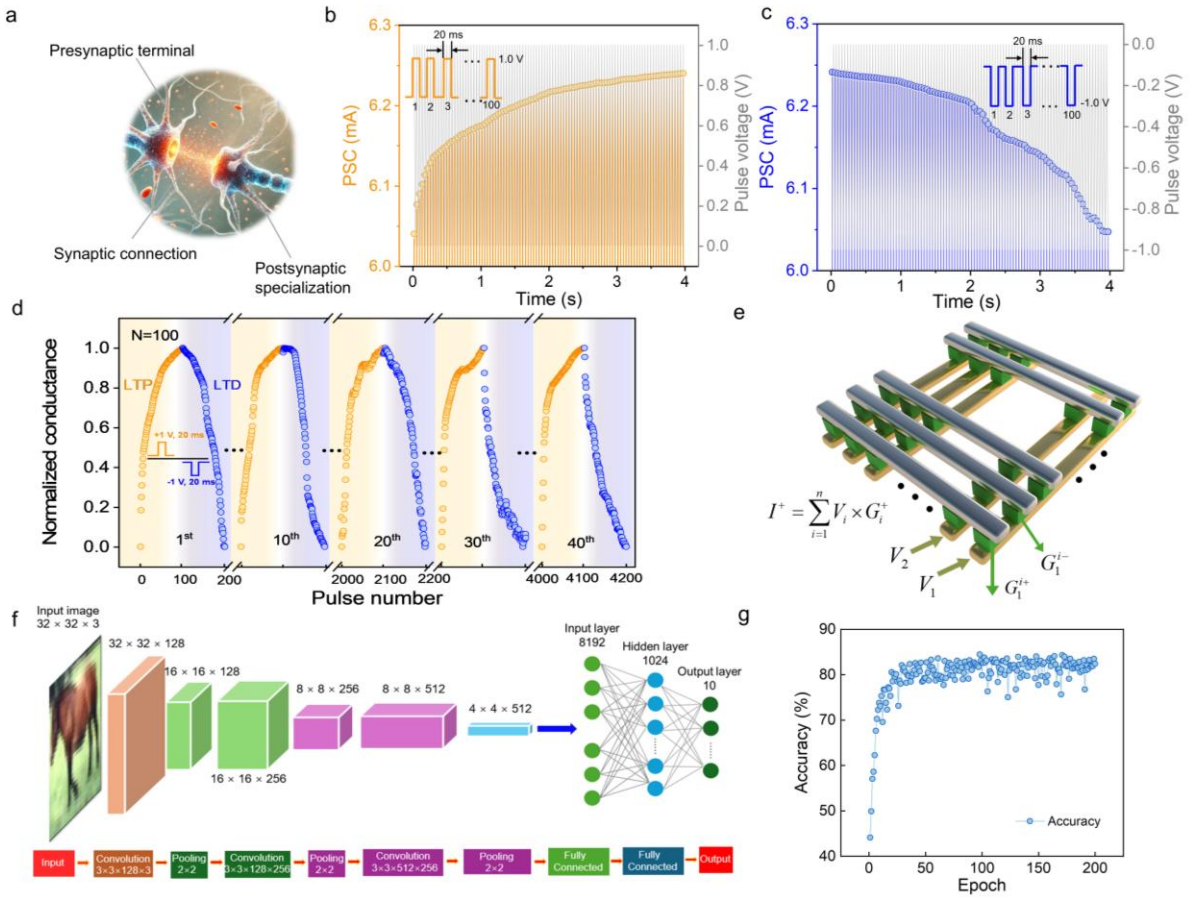

Figure 4. Emulation of synaptic characteristics and CNN simulation based on 2D Bi_2SeO_5 memristor. (a) Schematic diagram of information transmission and the synaptic weight updating via biological spikes conveyed between different neurons. (b) The synaptic weight update (i.e., a gradual increase in conductance) under 100 positive-pulse excitations. Reversible synaptic weight modulation via LTP (+1 V, 20 ms) pulses. (c) The synaptic weight update (i.e., a gradual decrease in conductance) under 100 negative-pulse excitations. Reversible synaptic weight modulation via LTD (−1 V, 20 ms) pulses. (d) Cycling test for the progressive potentiation/depression behaviors, showing small C2C variations over 40 cycles. (e) Schematic diagram of the hardware implementation for the VGG-8 neural network. (f) Schematic architecture of the VGG-8 CNN built for image recognition using the CIFAR-10 dataset. (g) The accuracy of image recognition with the training epochs.

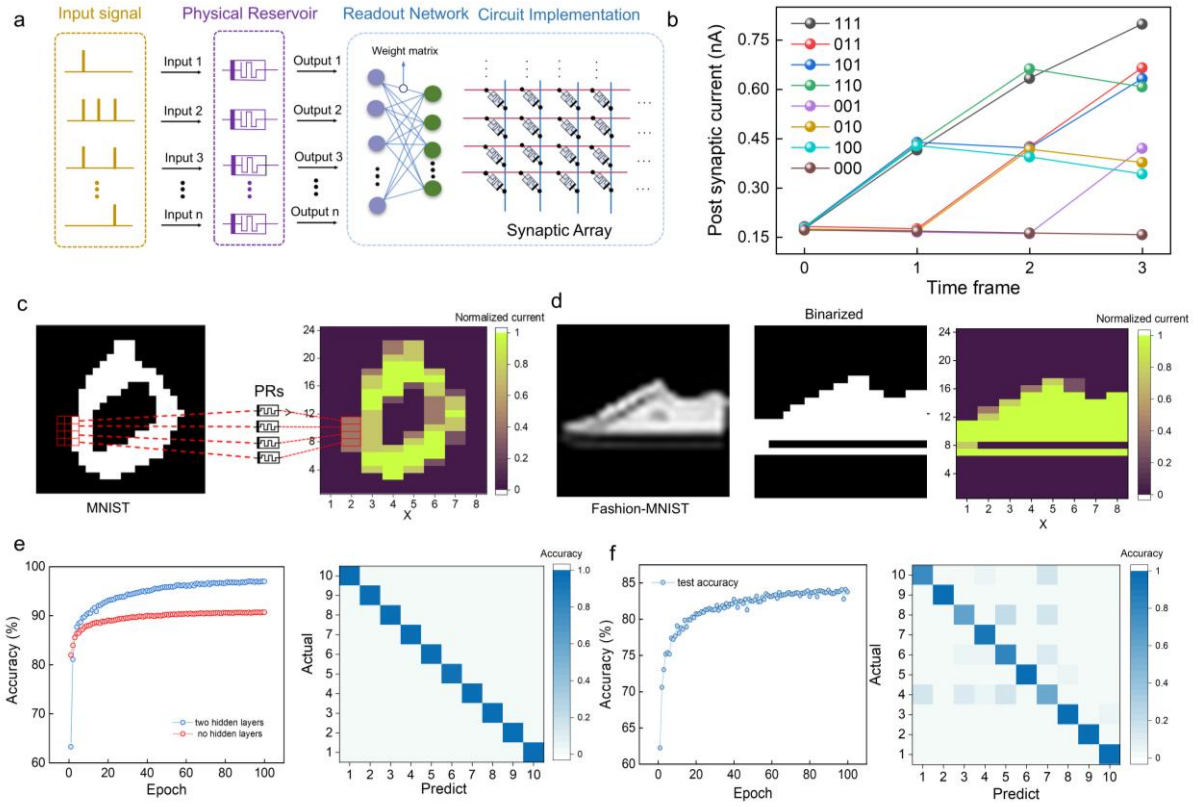

Figure 5. RC system for image classification. (a) The schematic working principle of the Bi_2SeO_5 based RC system for image classification tasks containing an input layer, a physical reservoir layer, and a readout layer. (b) The output current response of reserve to 8 different input voltage pulse streams. The distinguishable output of 3-bit reservoir states. (c) The recognition of handwritten digits "0" from the MNIST dataset. Reservoir output of digits "0". (d) The recognition image "sneaker" from the f-MNIST dataset. Reservoir output of image "sneaker" (e) Training accuracy after 100 epochs of digit pattern recognition and confusion matrix for all 10 classes in the MNIST dataset, showing the classification results. (e) Training accuracy after 100 epochs of image "sneaker" from the f-MNIST dataset and confusion matrix for all 10 classes in the MNIST dataset, showing the classification results.