A Novel Packaging Solution for Photonic Engine Application

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Abstract

Silicon photonic is a very promising solution to meet the dramatical increase of bandwidth and the ultra-low power consumption demands for data centers and high-performance computing. One of the challenges on realization of final product is the packaging which integrate both electronics integrated circuits (EICs) and the photonics integrated circuits (PICs). A careful packaging solution should be developed to handle higher bandwidth at a cost of lower power consumption, or improper solution can negate all the possible benefit of silicon photonic. In this paper, we suggest a novel packaging solution by the combined method of flip-chip and wire-bonding to realize 400G data rate photonic engine.

I. Introduction

The demand for data center interconnect bandwidth is growing exponentially, driven by the surge in global internet traffic, which is projected to reach 400 exabytes per month by 2022 [1]. Meeting this escalating data bandwidth requirement can be achieved through two primary approaches. The first involves expanding the number of I/O pins, which roughly doubles every six years. The second approach is to enhance the bandwidth per I/O. Industry trends typically follow a "tick-tock" pattern to achieve a doubling of total I/O bandwidth every 3 to 4 years [2].

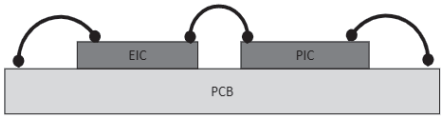
Increasing data rates per I/O might seem straightforward by raising electrical speeds. However, limitations arise due to copper connection performance issues, including insertion loss and inter-symbol interference at high frequencies. High symbol rates and high-order modulation exacerbate these signal integrity (SI) problems. While adding equalization circuitry can address these issues, it results in higher power consumption, which is undesirable since data centers strive to reduce power consumption to the range of tens of pico-joules per bit to sub-picojoules per bit.

To address these challenges, data centers integrated with silicon photonics emerge as a highly promising solution. Silicon photonics offers superior signal quality and lower power consumption at high speeds compared to conventional technologies. Commercially available key components such as modulator drivers, traveling-wave Mach-Zehnder modulators (TW-MZMs) [3], and photodiodes have demonstrated capabilities above 50GHz. When combined with high-order modulation schemes like PAM4 instead of NRZ, data rates of 100Gbps per channel can be achieved.

However, to fully harness the benefits of silicon photonics, careful consideration of interconnects between Electro-Optical Integrated Circuits (EICs) and Photonic Integrated Circuits (PICs), as well as EICs and switch ICs, is essential. Neglecting these aspects could negate the advantages of silicon photonics. Therefore, the choice of packaging solutions becomes crucial, as it ultimately determines the overall system performance. In the context of photonic engines, a well-designed packaging solution is critical, with an emphasis on minimizing interconnect parasitic, which can adversely affect signal integrity (SI) and power consumption.

In Section II, we provide an overview of popular packaging architectures commonly adopted in photonic engines. Section III introduces a novel packaging solution. In Section IV, we show the simulation result. Finally, in Section V, we draw our conclusions based on the discussed packaging solutions and their implications for system performance.

II. Integration Architectures



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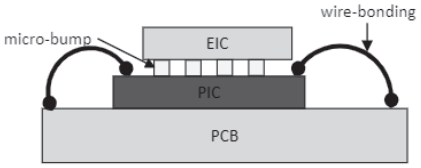

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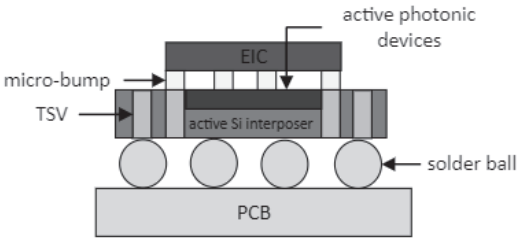

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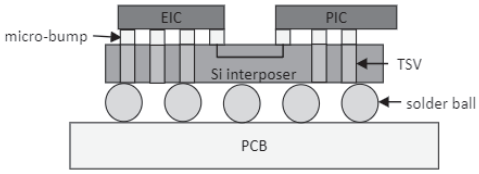

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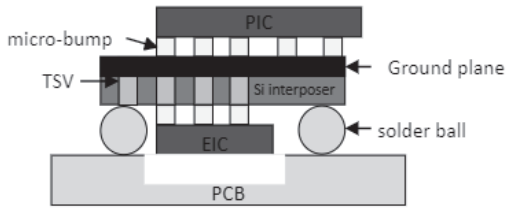

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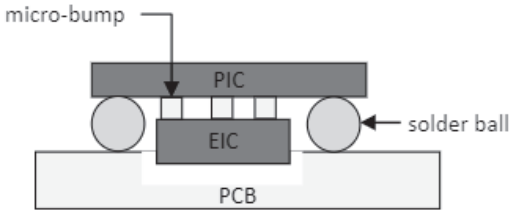

(f)

Fig. 1. Various integration architectures for EIC and PIC packaging. (a) 2D integration. (b) 3D integration with active silicon interposer. (c) 3D integration with active silicon interposer. (d) 2.5D integration with passive silicon interposer. (e) A sandwich-like 3D packaging solution with passive silicon interposer. (f) A low-cost 3D integration solution without silicon interposer.

Fig. 1(a) illustrates the prevalent 2D integration approach employed in earlier generations of photonic engines. In this setup, the Photonic Integrated Circuit (PIC) and Electro-Optical Integrated Circuit (EIC) are placed side by side on a Printed Circuit Board (PCB), communicating with each other and with Application-Specific Integrated Circuits (ASICs) through wirebonds. While 2D integration offers the advantage of being a cost-effective and straightforward packaging method, it has its drawbacks. The fixed diameter and pitch of wirebonds result in a characteristic impedance significantly higher than the standard 50 ohms, acting as a parasitic inductor. As frequencies increase to meet high bandwidth demands, this parasitic effect worsens, leading to issues like bad return loss, bad insertion loss, and degraded signal integrity. Ultimately, this limits the data rate per I/O. Another limitation of 2D integration is that all interconnects, including high-speed signals, grounds, power supplies, and bias lines, are constrained to the edges of the ICs. Attempting to increase the number of I/O lanes for higher data rates through 2D integration poses a significant routing challenge, as the perimeter does not scale proportionally with the number of I/O lanes. These drawbacks of the 2D integration method constrain its ability to scale up to higher data rates.

To address these limitations, a 3D EIC-on-PIC packaging solution [4] is proposed, as depicted in Fig. 1(b). EICs are stacked on top of PICs to save space, and micro-bumps replace the interconnects between them, with typical dimensions of 60um diameter, 60um height, and 90um minimum pitch. This advanced packaging approach substantially mitigates parasitic effects between EICs and PICs, enabling support for higher frequencies while maintaining acceptable signal integrity. However, the interconnects between EICs and ASICs remain wirebonds, like the 2D solution. This approach still faces the challenge of increasing the number of I/Os and the efficient delivery of power to EICs and active photonic devices, known as the power integrity issue.

To tackle these challenges, Through-Silicon Vias (TSVs) are introduced, as illustrated in Fig. 1(c). TSVs, with typical dimensions of 10um diameter, 100um height, and 40um minimum pitch, offer direct access from EICs and PICs to ASICs. Due to their shorter length, TSVs exhibit lower parasitic inductance and IR drop, enabling signal and power integrity at higher frequencies of interest. Furthermore, this solution can be readily scaled up to high data rates by increasing the number of I/Os, as the population of micro-bumps and TSVs grows proportionally with the area. This high-density, low-parasitic 3D integration method is considered a promising solution for the next generation of silicon photonics. However, careful co-design between electrical and photonic components is crucial, given the strong electrical and thermal coupling between EICs and PICs due to their proximity.

The combination of PICs and TSVs can create an active photonic interposer, a key component of this 3D packaging solution. Nevertheless, this technology is relatively expensive, immature, and has a long lead time. As a compromise, a 2.5D solution [10] has been developed, as shown in Fig. 1(d). In this configuration, EICs and PICs are mounted side by side on a passive silicon interposer, connected to ASICs using TSVs and Ball Grid Array (BGA) connections. The interconnect between EIC and PIC comprises two micro-bumps and one transmission line on Redistribution Layer (RDL). While this setup occupies more space compared to the 3D solution, it reduces thermal coupling between EIC and PIC due to the absence of stacking.

In Fig. 1(e), a pioneering 3D EIC-on-PIC packaging solution [11] is introduced, characterized by a novel "sandwich-like" approach. This method involves employing a passive silicon interposer with double-sided Integrated Circuits (ICs), a process successfully demonstrated in previous works [5-7]. Specifically, the Photonic Integrated Circuit (PIC) is flip-chipped onto the top side of the interposer, while the Electro-Optical Integrated Circuits (EIC) are attached to the back side. The integration utilizes Through-Silicon Vias (TSVs), micro-bumps, and Ball Grid Array (BGA) connections to establish communications between the EICs, PIC, and the Printed Circuit Board (PCB). This packaging solution offers several notable advantages:

1. Scalability: The aggregate number of interconnects across the interposer area can scale proportionally with the number of channels, facilitating the accommodation of higher data rates.
2. High Data Rate Handling: Due to the low parasitic effects and short interconnect lengths, this solution is well-suited to handle higher data rates effectively.
3. Electrical and Thermal Isolation: The interposer situated between the PIC and EIC plays a crucial role in mitigating electrical and thermal crosstalk between these components. Additionally, it allows for the effective removal of thermal concerns from the PCB side.

This packaging approach is designed to easily scale up to 800G data rates and beyond, making it a promising solution for advanced photonic applications.

In Fig. 1(f), an alternative, cost-effective variation is proposed, based on a chip-to-chip integration process demonstrated in previous works [8-9]. In this variation, an interposer is not utilized. The EIC is directly attached to the PIC through micro-bumps. The entire packaging assembly is reversed and connected to the PCB using BGA connections. This approach offers a simplified design but comes with specific challenges, primarily associated with the proximity of the EIC to the PIC. Careful co-design is essential to minimize both electrical and thermal coupling between these closely positioned components.

III. Suggested Packaging Solution

The suggested packaging solution is shown in Fig. 2. A driver is mounted on an IC carrier board by flip-chip method, it is connected to PCB through RF traces, vias and solder balls. Compared to wire-bonding method with high parasitic inductance, the impedance of differential RF trace on carrier board can be easily controlled as 100Ohm and can handle higher bandwidth. And usually, wire-bonding also require cutting a cavity on PCB to offset the height gap between EIC and PCB, for suggested method this cavity is not necessary. Wire-bonding is used to connect PIC and the driver, although wire-bonding introduce parasitic inductance, in our solution the height gap between driver pad on carrier board and PIC pad is less than 50um, and the gap between them is 100um, so the length of it is short enough to handle 100G data rate. Flip-chip and FOWLP are also possible packaging solutions for PIC, but fiber array needs to be attached to the front side of PIC, a special process of face-down packaging needs to be developed and the fiber array assembly becomes more difficult.

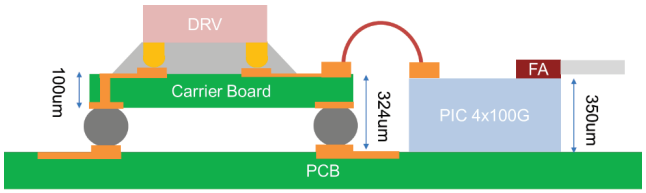

Fig. 2. Diagram of suggested packaging solution.

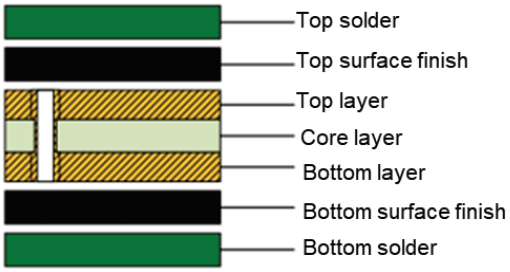

Fig. 3. Stack-up.

IV. Results and Analysis

Fig. 3 shows the stack-up used in simulation, a symmetrical structure is applied to avoid PCB warpage. Table 1. Shows the thickness and electrical parameters used in simulation. The calculated differential GSGSG type RF transmission line of 100Ohm and 60Ohm are presented in Table 2.

Table 1. material used in simulation.

Layer	Thickness (um)	material	Dk/Df
Top solder	20	Taiyo Ink	4.3/0.029
Top surface finish	4	Nickel, Gold	-
Top layer	12	Copper	-
Core layer	100	GX Laminate R-1515E	4.7/0.011
Bottom layer	12	Copper	-
Bottom surface finish	4	Nickel, Gold	-
Bottom solder	20	Taiyo Ink	4.3/0.029

Table 2. calculated transmission line dimension.

Transmission line	Impedance (Ohm)	Width/ Gap (um)
Diff. CPWG	100	30/ 38.6
Diff. CPWG	60	105/ 30

Fig. 3 shows the full-wave simulation 3D model of RF path between driver and PCB, the total length of is about 1.5mm. Fig. 4 shows the model of RF path between driver and PIC, the total length is about 1.3mm. As shown in Fig. 5, the S11 of RF path between driver and PCB is better than -10dB at 28GHz and the S21 is better than -0.5dB at 28GHz. As shown in Fig. 6, the S11 of RF path between driver and PIC is also better than -10dB at 28GHz and the S21 is better than -0.3dB. So, these simulation results validate that suggested packaging method can handle 100G data rate, if PAM4 modulation scheme is used.

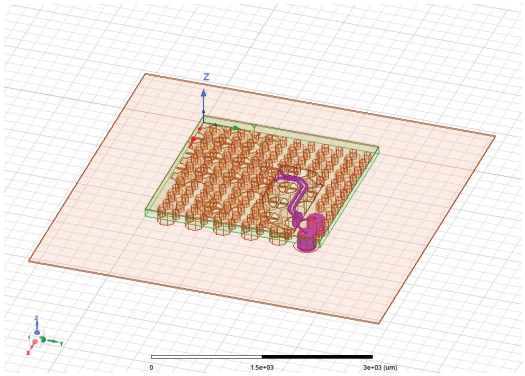

Fig. 3. the full wave model of RF path from PCB to modulator driver input.

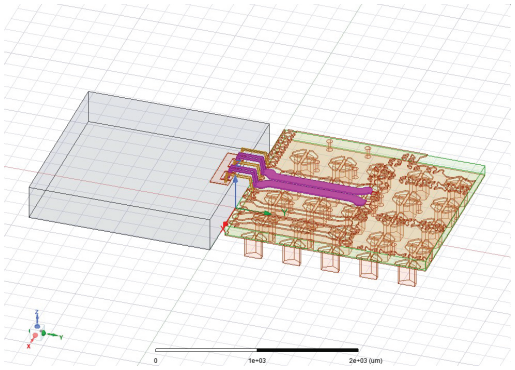

Fig. 4. the full wave model of RF path from modulator driver output to PIC.

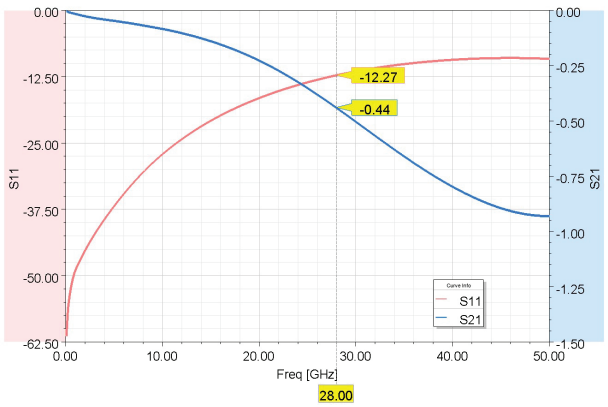

Fig. 5. S-parameter of RF path from PCB to modulator driver input, normalized to 100Ohm

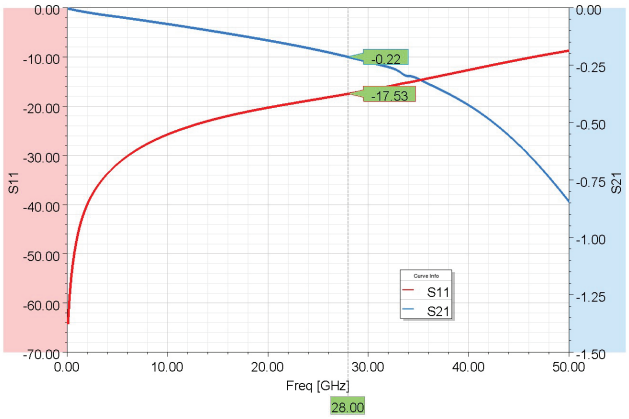

Fig. 6. S-parameter of RF path from modulator driver output to PIC, normalized to 60Ohm.

V. Conclusions

In this paper, a novel packaging solution for 400G photonic engine is suggested. It fully exploits the benefit of flip-chip and wire-bonding method and avoids their drawback, such as cavity on PCB to offset height gap for wire-bonding and fiber array assembly difficulty of flip-chip and FOWLP.

Acknowledgments

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