

Development of Large RDL Interposer Package using RDL-first FOWLP Process

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Abstract

In this work, an organic RDL interposer with large package size of 52 x 44 mm consisting of 12 embedded chiplets on a 60 x 60 mm organic substrate has been demonstrated using RDL-first FOWLP process. 2 field masks stitching was used to create the large interposer package size. 6 layers of high-density Cu RDL have been processed to meet the 12 chiplets interconnectivity and bandwidth performance requirements. Chiplets with micro-bumps were assembled on the RDL with a mass reflow process and encapsulated with mold compound thus forming the RDL interposer package. Electrical testing was conducted on the RDL test structures and the chiplets and results show good electrical continuity across the stitched Cu RDL traces and assembled chiplets. Shadow Moiré warpage measurement was performed on the RDL interposer package to characterize the warpage behavior during board assembly. The Shadow Moiré results show a large warpage change associated with the large RDL interposer during reflow process. A TCB technique was used to assemble the RDL interposer to the organic build-up substrate, to reduce the package warpage and enable the assembly of the RDL interposer to the organic substrate.

1. Introduction

In recent years, the chiplets packaging approach has attracted great interest among major semiconductor companies as an alternative to system on chip (SoC). SoC technology has traditionally been used to construct high-performance application systems by integrating many technologies and functional blocks onto a monolithic chip. However, as SoC design complexity increases, it takes longer development time and higher cost to manufacture. Chiplets are a low-cost, faster-to-market alternative to SoC. Companies can build systems using the chiplets technique, which involves combining chips from diverse technologies into a system using an advanced packaging platform.

There are several platforms for chiplets packaging, such as embedding chiplets in a fan-out wafer level package based RDL interposer [1,2], assembling chiplets on silicon interposer [3,4] or high-density build-up organic substrate [5]. The substrate materials are what differentiate various platforms, with the redistribution layer (RDL) serving as the technology that enables all chiplets systems. Chiplets platforms frequently demand a large package area and large number of layers of high-density fine pitch RDL to facilitate routing between multiple chiplet I/Os. If the package area exceeds the photolithography tool's maximum photomask field size, several mask fields must be stitched together to reach the required package size, and mask stitching misalignment need to be

corrected so that RDL traces continuity is maintained across the stitched area.

In this work, a RDL-first or chip-last FOWLP process was developed to fabricate a large organic RDL interposer for chiplets packaging. The RDL-first procedure [6] is chosen as the fabrication method because it allows for the processing of large number of RDL layers on a temporary carrier substrate with very low wafer warpage. Furthermore, chiplets with micro-bumps can be solder assembled onto the RDL stack and then encapsulated with mold compound with a wafer level molding process to create a reconstructed wafer. Once the temporary carrier is de-bonded, the reconstructed wafer is diced up forming the RDL interposer package. Since, all the fabrication processes are performed on the carrier substrate, there is less warpage related issues, as compared to mold-first FOWLP process.

Experimental Procedure

2.1 Test Vehicle Design

Figure 1 shows the illustration of FOWLP based RDL interposer assembled on organic build-up substrate. The RDL interposer consist of 6 layers of high-density fine pitch RDL with minimum Cu trace of 2 μm L/S. Chiplets with micro-bumps are assembled onto the RDL stack. The chiplets are then underfilled and encapsulated with an epoxy mold compound forming the RDL interposer package. The RDL interposer package is then assembled on a larger organic substrate. Figure 2 shows the top view schematic of chiplets size and position. A total of 12 chiplets are integrated in the RDL interposer. The RDL interposer package size is 52 x 44 mm, while the organic substrate is 60 x 60 mm. Table 1 shows the specification of the chiplets and RDL interposer.

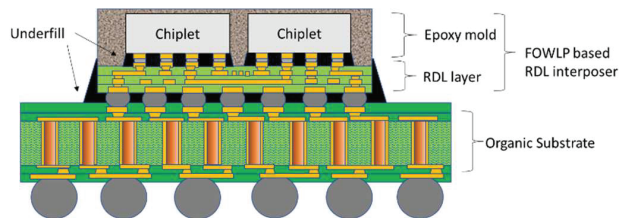


Figure 1. Illustration of RDL interposer on organic build-up substrate based on RDL-first FOWLP

Table 1. Specifications of the Chiplets and RDL interposer

Chiplets	Die Size	Critical dimension
Chiplet A	11.87 x 7.75 mm	25 μm dia. bump / 55 μm pitch

Chiplet B	23 x 9.75 mm	25 μm dia. bump / 55 μm pitch
RDL interposer	52 x 44 mm	Top UBM: - 25 μm dia. UBM / 55 μm pitch Cu RDL (6 -layer): - Min. 2 μm L/S Cu RDL - Min. 3 μm contact via Bottom solder bump: - 100 μm dia. SAC305 bump/200 μm pitch
Organic substrate	60 x 60 mm	Solder mask defined pre-solder pad: - 100 μm dia. pad/ 200 μm pitch

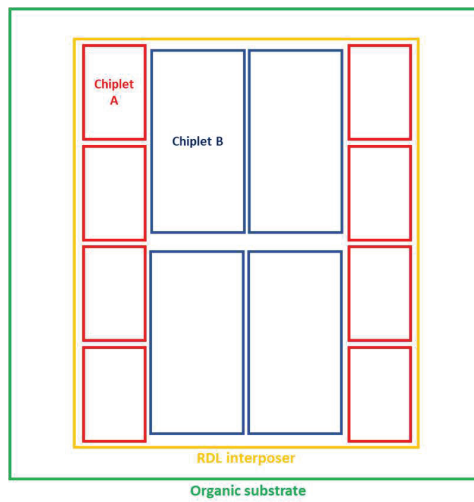


Figure 2. Top view of the RDL interposer showing the position and size of the chiplets, RDL interposer and organic build-up substrate

1.2 Process Flow

The RDL-first FOWLP process flow was used to fabricate the RDL interposer as shown in figure 3. Multi-layer high density Cu redistribution traces were first fabricated on a temporary transparent carrier. For the RDL process, a low temperature cured photo-dielectric was used as the interlayer passivation, and Cu distribution lines are fabricated using a semi-additive process (SAP). The photolithography stepper used in this work has a maximum exposure field size of 44 x 26.7 mm and two field mask stitching was used to form the large package size of 52 x 44 mm. Figure 4 shows the wafer map during photomask exposure. RDL interposer packages can be produced from a 300 mm diameter carrier. Chiplets with micro-bumps interconnects were then assembled to the top UBM pads on the RDL stacks using a mass reflow process. The chiplets and RDL stacks were encapsulated with epoxy mold compound to form a reconstructed wafer. The temporary carrier was de-bonded from the reconstructed wafer. Solder balls were attached to the bottom UBM pads of the reconstructed wafer to

form the solder ball grid array. The reconstructed wafer was diced to individual RDL interposer package. The RDL interposer package was then attached to the organic substrate. Underfill material was dispensed and cured to fill-up the gap between the FOWLP and the organic substrate.

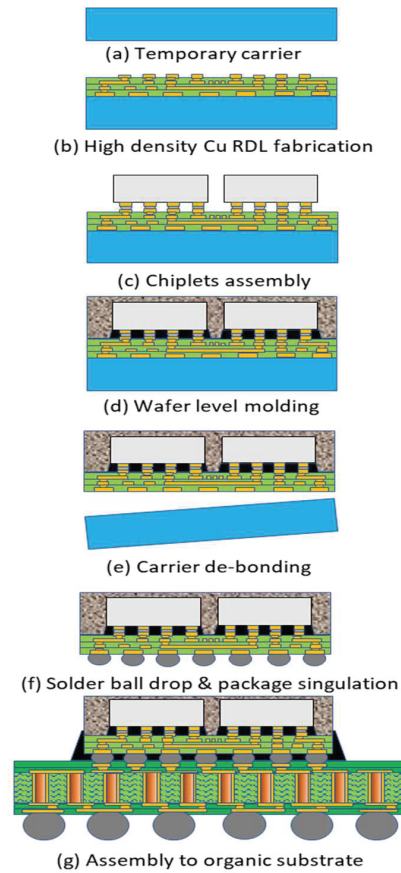


Figure 3. Fabrication process of RDL interposer package using RDL-first FOWLP

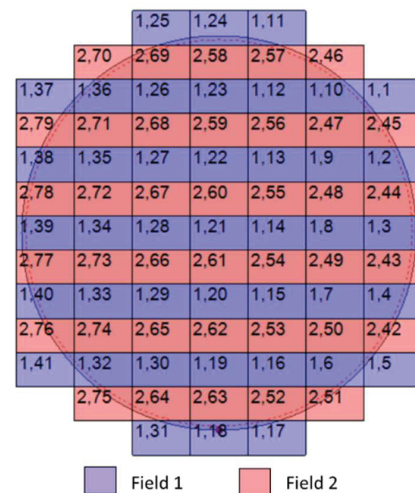


Figure 4. Wafer map during photomask exposure showing mask field and exposure sequence

1.3 Testing

The fabricated RDL interposers were subjected to electrical and warpage measurement as mentioned below.

1.3.1 Electrical measurement of Cu RDL and Chiplets

Electrical measurement was performed on the following e-test structures:

- (a) 2 μm L/S meander combs located at the stitched area between the 2 masks field to check the continuity of the RDL traces.
- (b) Daisy chain connecting the chiplets to the RDL layers to verify the continuity of the solder bumps and RDL interposer.

2.3.2 Warpage measurement

Package warpage is crucial as it can affect the assembly process of the RDL interposer to the organic substrate and results in poor solder joint formation, particularly for an interposer package of such large dimension. Fabricated packages were loaded into Shadow Moiré measurement tool and subjected to heating profile that simulate the reflow condition. Shadow Moiré optical technique was used to measure the warpage of RDL interposer under the reflow condition.

2. Results and Discussions

3.1 RDL Interposer Fabrication Results

3.1.1 Cu RDL Process Results

Figure 5(a) shows the RDL and UBM layers fabricated on temporary transparent carrier, prior to chiplets assembly. Figure 5(b) shows magnified optical images of single interposer package. Figure 6 shows high density 2 μm L/S Cu RDL traces at different magnifications to support the high bandwidth requirement of the chiplets. Figure 7(a) shows the 3 μm diameter contact via openings developed in photo-dielectric film used to connect the different Cu metallization layers and figure 7(b) shows the landing pads and Cu traces processed over the contact vias. Figure 8 shows the fine pitch Cu traces fabricated at the stitching section (blue dash line) between 2 mask fields. No Cu traces discontinuity was observed along the stitching line boundary.

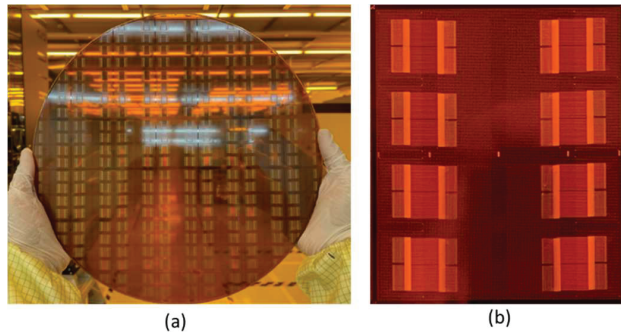


Figure 5. RDL processing on temporary carrier; (a) RDL layer fabricated on transparent carrier, (b) magnified image of single interposer package.

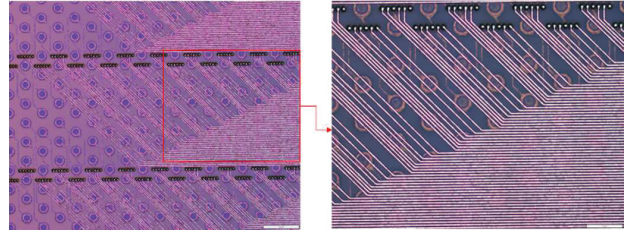


Figure 6. A segment of the high density 2 μm L/S Cu RDL traces at different magnifications.

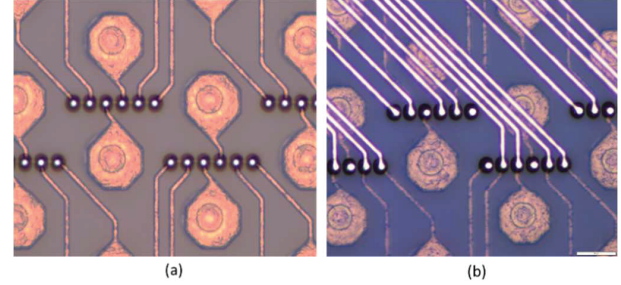


Figure 7. Contact vias for connecting the different Cu RDL; (a) 3 μm diameter contact via openings developed in photo-dielectric film, (b) Cu traces and landing pad processed over the contact vias.

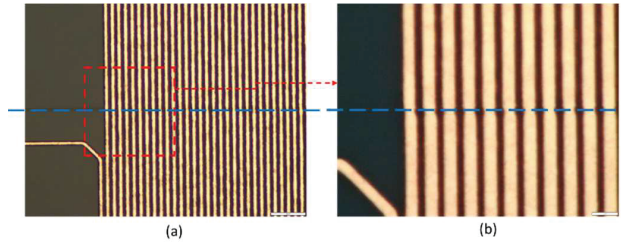


Figure 8. Cu RDL traces located at the stitch line (blue dash line) between the 2 mask fields; (a) 2 μm L/S Cu traces stitched, (b) magnified images showing the section of the stitched traces.

3.1.2 Chiplet Assembly, Wafer Level Molding and RDL interposer Package Assembly

Figure 9(a) and (b) shows the optical images of the chiplets, assembled onto the RDL stack on the carrier wafer and after wafer level molding, respectively. X-ray inspection was performed on the assembled chiplets showing good solder joint alignment and formation with the RDL stack layer (Figure 10). Figure 11(a) and (b) show the fabricated RDL interposer package after singulation and solder bump attachment, respectively. The RDL interposer was finally assembled onto the organic build-up substrate with thermo-compression bonding (TCB) process as shown in Figure 11(c).

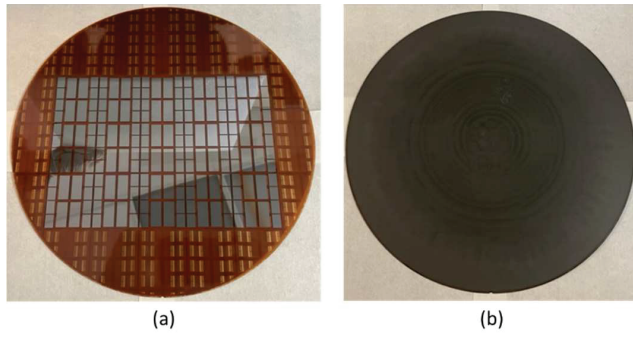


Figure 9. Chiplets assembled on carrier; (a) an array of chiplets assembled on the RDL layers, (b) after wafer level molding to encapsulate the chiplets assembly and RDL layer

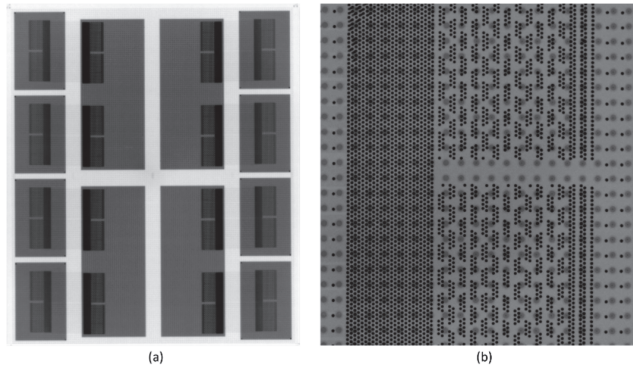


Figure 10. X-ray images of solder interconnects; (a) single RDL interposer with the 12 chiplets, (b) magnified X-ray images of fine pitch solder bumps.

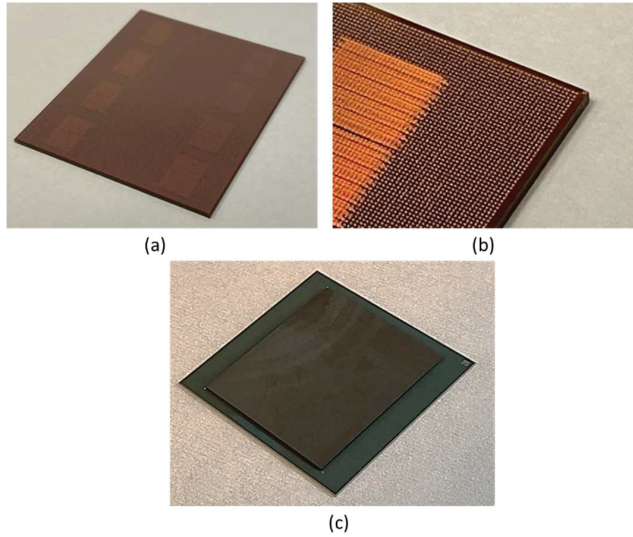


Figure 11. RDL interposer package after solder ball drop and attachment to organic substrate; (a) tilted optical image of the solder bump side of the RDL interposer, (b) magnified image showing the SAC305 solder bumps, and (c) after attachment to organic substrate

2.2 Electrical Measurement

2.2.1 Meander Comb Test Structure at Stitch Line

Figure 13 shows a $2\ \mu\text{m}$ L/S meander comb test structure located at the stitch line between the two masks field. A slight taper can be observed at the point where the two traces meet. Figure 14(a) shows the I-V curve of the meander trace, indicating good connectivity for the stitched Cu traces. The measured intra-layer leakage current is shown in figure 14(b). the measured leakage current is in the range of pico-ampere which is within the target specifications.

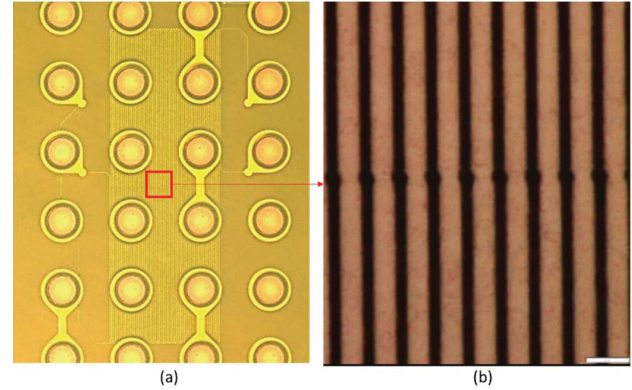
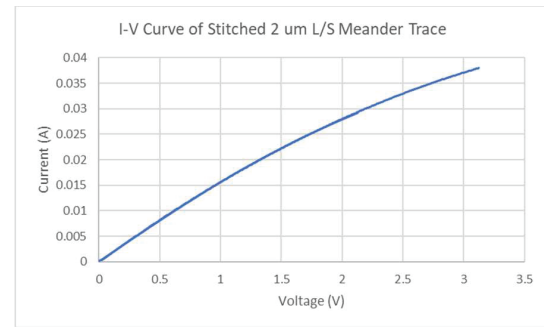
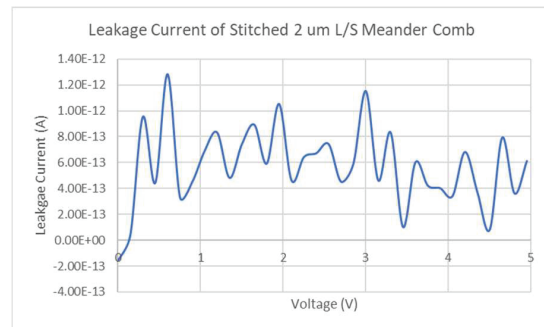


Figure 13. (a) Meander comb test structure at stitch line, (b) magnified image of meander traces at the stitch line



(a)



(b)

Figure 14. Electrical test results of stitched meander comb structure; (a) I-V curve of meander Cu trace, (b) intra-layer leakage current of meander comb.

3.2.2 Chiplets to RDL Daisy Chain

Figure 15 show the daisy chain locations between RDL and chiplets. Electrical testing was performed on the respective UBM pads connected to the RDL and chiplets and all daisy

chains shows good electrical continuity with no open connections, indicating good assembly yield of the chiplets with mass reflow process.

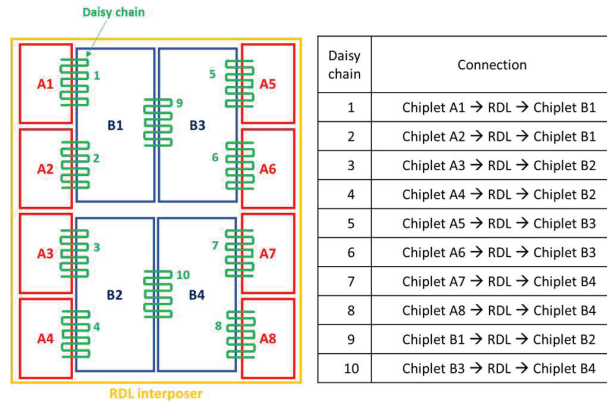


Figure 15. Designation of the chiplets and daisy chain locations.

3.3 Warpage Measurement

Shadow Moiré technique was used to measure the warpage of fabricated RDL interposer packages when subjected to a reflow process. This is to evaluate the warpage of the interposer package when it is being mounted to organic substrate. Figure 16 shows the package warpage during reflow process. The fabricated package was measured with bump side facing down (live-bug). Positive values indicate a convex profile and negative values indicates a concave profile. The RDL interposer has an initial convex warpage of 213 μm , and the package profile transit from convex to concave with profile with increasing temp, eventually reaching a max warpage of -736 μm at peak temperature of 275 degree Celsius, before reducing with reduction in temperature. The final package warpage is 277 μm upon cooling down to room temperature. The large change in warpage is due to the CTE mismatch between the RDL layers and the chiplet and mold compound. This result indicates the large warpage change in RDL interposer package. This represents significant problem when assembling the RDL interposer to the organic substrate using a reflow approach, such as no solder joints formation.

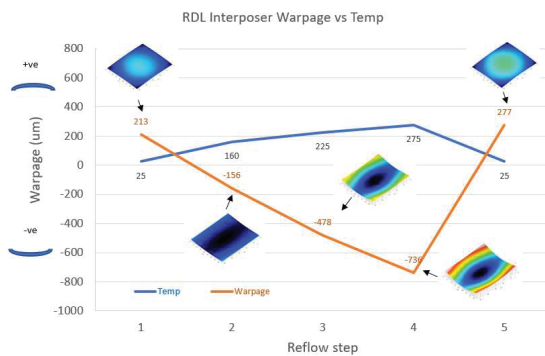


Figure 16. Package profile of RDL interposer measured by Shadow Moiré at key reflow temperature.

A TCB process was implemented for assembling a large RDL interposer package to overcome the large package

warpage. The RDL interposer is first pick-up on the bond tool and pre-heated to 100 degree Celsius to reduce the interposer warpage. The RDL interposer is aligned and pressed onto the organic substrate with a low bond force. The bond tool is then heated up to peak bond temperature of 300 degree Celsius for a short duration and cooled down. The bond force is maintained throughout the cooling step to reduce the warpage of the RDL interposer during the cooling. Figure 11(c) shows the RDL interposer successfully assembled to the organic substrate with the TCB process.

3. Conclusions

A RDL interposer with large package size of 52 x 44 mm with 12 embedded chiplets has been demonstrated using RDL-first FOWLP process. 2 masks stitching was used to produce the large RDL interposer. 6 layers of high density RDL with 2 μm L/S was processed on the temporary carrier. Chiplets with micro-bumps were assembled on the RDL by picking and placing the chiplets on the respective UBM bonding sites and forming the solder joints with a mass reflow process. X-ray inspection show good alignment and solder joints formation of the chiplets to RDL layer using the mass reflow process. The assembled chiplets were encapsulated with epoxy mold compound to form the RDL interposer package. Electrical testing was conducted on the 2 μm L/S meander comb test structure located at the stitching line between the 2 mask fields, and the test results show good electrical continuity for the stitched structure with low leakage current in the intra-layer RDL. Daisy chain connectivity test was also conducted for the 12 chiplets and the chiplets shows good connectivity with the RDL layer. Shadow Moiré warpage measurement was carried out on the fabricated RDL interposer package with bump side down (live-bug) and the package was subjected to reflow process to characterize the warpage behavior of the large package. The fabricated RDL interposer show an initial convex warpage of 213 μm and change to convex warpage of -738 μm at the peak temperature of 275 degree Celsius, before returning to a convex warpage of 277 μm when cooled to room temperature. This large warpage change in the RDL interposer package poses a major risk when assembling the RDL interposer to the organic substrate through reflow. A TCB process was implemented to assemble the RDL interposer to the organic substrate to reduce the package warpage during the assembly process.

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References

- [1] K. Sakuma et al., "Heterogeneous Integration on Organic Interposer Substrate with fine-pitch RDL and 40 micron pitch Micro-bumps," 2023 IEEE 73rd Electronic Components and Technology Conference (ECTC), (2023) pp. 872-877

- [2] Lin, Yihang et al. "Multilayer RDL Interposer for Heterogeneous Device and Module Integration." 2019 IEEE 69th Electronic Components and Technology Conference (ECTC) (2019), pp. 931-936
- [3] I. Lee et al., "Extremely Large 3.5D Heterogeneous Integration for the Next-Generation Packaging Technology," (2023), 2023 IEEE 73rd Electronic Components and Technology Conference (ECTC), (2023), pp. 893-898
- [4] K. Murai et al., "Study of Fabrication and Reliability for the extremely large 2.5D advanced Package," 2023 IEEE 73rd Electronic Components and Technology Conference (ECTC), (2023), pp. 899-906
- [5] S. Miki et al, "Development of 2.3D High Density Organic Package using Low Temperature Bonding Process with Sn-Bi Solder," 2019 IEEE 69th Electronic Components and Technology Conference (ECTC) (2019), pp. 1599-1604
- [6] V. S. Rao et al., "Development of High Density Fan Out Wafer Level Package (HD FOWLP) with Multi-layer Fine Pitch RDL for Mobile Applications," 2016 IEEE 66th Electronic Components and Technology Conference (ECTC), (2016), pp. 1522-1529