The Role of Ti Capping Layer in HfO_x-Based RRAM Devices

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***Abstract*— In this letter, we examine the role of the Ti capping layer in HfO_x-based resistive random access memory (RRAM) devices on the memory performance. It is found that with a thicker Ti capping layer, the fresh device initial leakage current increases and as a result, the forming voltage decreases. In addition, with a thin Ti layer of <3 nm (on top of 8-nm HfO_x), there is no resistive switching, while by inserting a thicker Ti layer of 10 nm, the memory window enlarges to about two orders. Very good uniformity has also been observed in thick Ti capping devices, demonstrating the effectiveness in RRAM device engineering. It is believed that the Ti layer serves as an oxygen reservoir, by extracting oxygen during device formation and electrical forming process and facilitates resistive switching thereafter.**

***Index Terms*— Nonvolatile memory, resistive random access memory (RRAM), resistive switching (RS), Ti capping.**

I. Introduction

WITH continuous shrinking of device dimensions, Flash memory is facing severe challenges mainly due to its charge based storage concept. It is necessary to identify emerging memory technologies that can fulfill the ever increasing demands on high density, high speed and low power consumption. Resistive random access memory or RRAM has been extensively researched as one of the most promising candidates for the next generation nonvolatile memory, due to its high performance and simple structure that can be integrated into CMOS back-end-of-line [1]–[3].

Among many resistive switching materials, binary transition metal oxides have attracted great attention due to their simple composition and excellent device performance [4], [5]. However, many of these devices are working with noble metal electrodes either one side or both [5], which may be difficult to integrate with CMOS circuits. HfO_x has been reported good device performance with TiN electrodes and inserting thin layers, e.g., Ti by Lee *et al.* [6], Zr by Wu *et al.* [7] or Hf by Govoreanu *et al.* [8]. It is believed that the capping layer is essential for the good resistive switching behaviors [9], [10], and Chen et al has compared the Hf/Ti/Ta metal cap on the endurance and retention performance [11]. In this letter, we focused on HfO_x based RRAM cell with Ti capping layer, and studied the role of this metal cap on the memory performance.

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II. Device Fabrication

Fabrications of TiN/HfO_x/Ti/TiN RRAM devices were done on 8″ CMOS platform without high thermal budget process. Both top and bottom electrodes (TE and BE) were 50 nm TiN, deposited by reactive sputtering in high vacuum. HfO_x of 8 nm was deposited using PICOSUN^{TM} P-300C atomic layer deposition (ALD) system from Picosun Oy with tetrakis (ethylmethylamino) hafnium (TEMAH) precursor and water vapor. Thin Ti capping layer in between oxide and top electrode was deposited by sputtering with splits of 1, 3, 5 and 10 nm respectively. After RRAM stack deposition, devices were patterned into square shapes with 248 nm lithography and dry etch. Then post-metal dielectrics of plasma enhanced chemical vapor deposition (PECVD) SiN/SiO_2 and Al metallization were used to complete device fabrications. Electrical characterization was carried out on Agilent B1500A semiconductor device analyzer.

III. Results and Discussion

High resolution transmission electron microscopy (TEM) was used to examine the micro morphology of the device as shown in Fig. 1, taking S4 as an example. It is seen that HfO_x layer is about 8nm as designed and there is 10nm Ti capping on top of it. As seen from TEM images, there are some small crystalline grains inside ALD HfO_x, indicating the film is not purely amorphous. The interface between Ti film and TiN electrode is not very sharp due to poor contrast, so to further confirm the materials stack information, EDX (energy-dispersive X-ray spectroscopy) line scan was performed along the direction as indicated in Fig. 1 (b). It is observed that oxygen profile tends to be attracted towards Ti side [12], by taking the intersection point of oxygen and nitrogen curve,

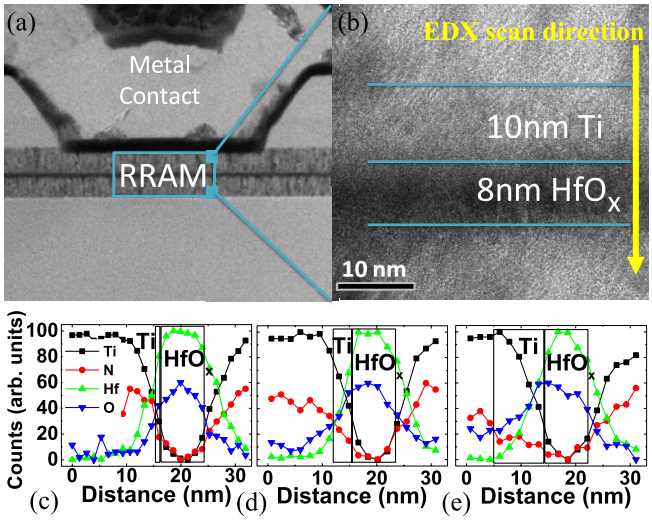

Fig. 1. (a) High resolution TEM image of S4 with 10nm Ti capping layer, confirmed the thickness of ALD HfO_x deposition of 8nm. EDX line scan was performed along the direction indicated by the arrow in (b) and spatial profile was plotted for S1 (c), S3 (d) and S4 (e) with Ti capping layer thickness of 1, 5 and 10 nm, respectively.

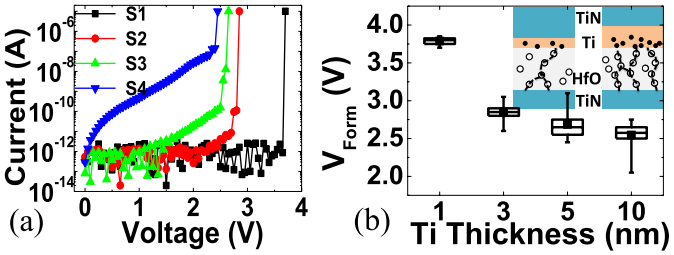

Fig. 2. (a) Initial device forming curve of all 4 samples, with forming voltage in the range of 2-4 V. (b) Forming voltage distribution box plot of 4 samples (collected from 10-20 devices each) versus Ti capping layer thickness. Larger fluctuations are observed in thick Ti capping devices. Inset schematically illustrates the origin of forming voltage fluctuations.

we can roughly identify the capping layer edge and it fits experiment design well, as shown in Fig. 1 (c) to (e).

In most of RRAM devices, a forming process is needed to initialize the resistive switching behavior, and the forming voltage is usually much higher than those of subsequent switching operations. Some literatures have been reported on the reduction of forming voltage amplitude for the ease of circuit design of RRAM chips [13], [14]. As seen from Fig. 2, forming voltages of four samples with Ti capping thickness of 1, 3, 5 and 10 nm, are 3.7, 2.8, 2.6 and 2.4 V, respectively. It demonstrates the effectiveness of Ti inserting layer in the reduction of initial forming voltage of oxide based RRAM device, making it an easy method to achieve low forming voltage or even forming free devices [15]. This can be attributed to the attraction of oxygen inside HfO_x towards Ti layer, as suggested from the EDX results. By inserting thicker Ti on top of oxide, more oxygen ions are removed, leaving more oxygen vacancies related defects. As a result, the fresh device leakage increases with thicker Ti capping layer and then a smaller forming voltage. It is worth noting that larger fluctuation of the forming voltage is observed in

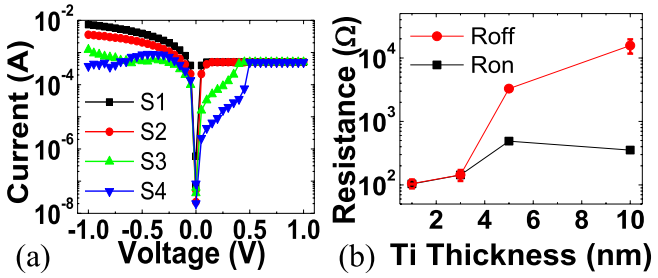

Fig. 3. (a) Typical resistive switching characteristics of all samples, showing no switching phenomena in S1 & S2 and good switching behaviors in S3 & S4. (b) On/off resistance plot of all samples versus Ti capping layer thickness.

thick Ti capping devices, which can be attributed to more possible breakdown paths with high density of oxygen vacancy related defects [16]. With thicker Ti capping, more oxygen vacancy related defects will be induced in the HfO2 layer, this results in more possible breakdown paths as indicated in the inset of Fig. 1(b) with dotted lines. Hence, larger variation in the forming voltage has been observed as compared to thinner or no Ti capping devices. However, once the filament is formed, it will dominate the current conduction and the resistive switching will occur within the major leakage path. Therefore, it doesn't affect the resistive switching uniformity afterwards.

After forming, devices exhibit bipolar resistive switching behaviors as reported in the literatures [6]. Set process from high resistance state (HRS) to low resistance state (LRS) happens in positive direction and vice versa reset process in negative direction with all bias applied to top electrode and bottom electrode grounded. As plotted in Fig. 3, there is hardly any resistive switching in S1 or S2, resistance remains unchanged after negative bias sweep, indicating there is no recovery of switching layer to high resistance with this operation. It is seen from Fig. 2 (a) that the fresh leakage current of S1 and S2 are extremely low, and during forming, there is a few orders current jump. This is probably due to the very thin Ti layer is not enough to induce resistive switching in HfO_x RRAM device, and there is severe current overshoot during forming process [17], which induced permanent breakdown to the switching layer. In comparison, devices with thicker Ti capping of 5 and 10 nm show good resistive switching. For S3 with 5 nm Ti, there is an on/off resistance window of around 10 times; and for S4 with 10 nm Ti, this window enlarges to about 2 orders.

This improvement in resistive switching behavior can be attributed to the oxygen gettering capabilities of Ti. Ti is well-known for its oxygen attracting properties. By adding Ti capping layer in between HfO_2 and TiN electrode, it will attract oxygen ions in the oxide and keep them in the interstitial sites or form Ti-O bonded structure near the oxide interface during fabrication process and device operations [18], [19]. When applying forming/set voltage, driven by the electric field, more oxygen ions are drifted towards Ti/oxide interface and formed oxygen vacancies related conduction filament. For most devices, compliance in current is necessary to limit the amount of oxygen to be removed from oxide to prevent

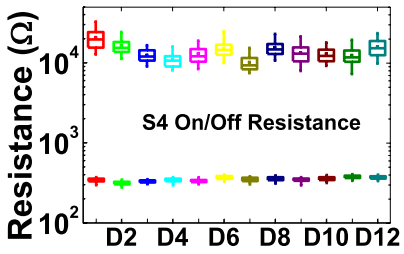

Fig. 4. Device-to-device on/off resistance uniformity plot of S4. Data taken from 100 DC cycles of 12 randomly selected devices across 8 inch wafer.

permanent breakdown. During reset process, by reverse the electric field, the oxygen ions stored near the Ti/oxide interface can be release to recover the vacancy related defect sites to rupture the conduction filament, and switch the device to high resistance state. A proper control of reset voltage in amplitude is also important to prevent oxide breakdown in the reverse direction. For Ti capping to work, it requires certain minimum amount, e.g. in this letter, to induce switching in 8 nm HfO_x, it requires at least of around 5 nm Ti. There is no resistive switching in S1 or S2, in comparison to >90% in S3 and S4. However, it may not be the case that the thicker Ti capping the larger on/off resistance. It will depend on how much the Ti insertion can take effect in HfO_x switching layer. For an optimum switching in thin HfO_x layer, it suggests a Ti capping layer of about 1 to 2 times of the switching oxide thickness.

To confirm the switching performance of Ti capped HfO_x RRAM device, 100 DC switching cycles were tested on 12 randomly selected devices on S4. On/off resistance extracted from measurement is plotted in Fig. 4. Excellent resistance distribution from device to device can be observed with memory window of about 100 times.

IV. Conclusion

The role of Ti capping layer on improving resistive switching performance in HfO_x based RRAM devices with CMOS compatible TiN electrodes was investigated in this work. It's observed the thicker Ti, the higher fresh device leakage and lower forming voltage. Also, by tuning the thickness of Ti capping layer, adjustable memory window and high device yield can be achieved, and showing an optimum thickness of about 1 to 2 times of the underlying HfO_x layer. All these together with EDX results indicate the oxygen reservoir capability of Ti capping layer, which may attract/release oxygen from/to the HfO_x layer during reversible switching.

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