An Integrated 60GHz Low Power Two-Chip Wireless System Based on IEEE802.11ad Standard

Kaixue Ma[1], Shouxian Mou[1], Nagarajan Mahalingam[1], Yisheng Wang[1], Bharatha Kumar Thangarasu[1], Jinna Yan[1], Wanxin Ye[1], Keping Wang[1], Wei Meng Lim[1], Thin Sek Wong[1], Yang Lu[1], Wanlan Yang[1], Kiat Seng Yeo[1], Francois Chin[2], Xiaoming Peng[2], Albert Chai[2], Khiam-Boon Png[2], Wong Sai Ho[2], Raymond Keh[2], Cai Zhaohui[2], Zhang Guoping[2], Chee Piew Yoong[2], Yin Jee Khoi[2], Zhang Weiqiang[2], Qu Xuhong[2], Law Sie Yong[2], Zhao Cheng[2], Chen Jian Simon[2], Cheng Wang Cho[2], Raymond Jayaraj[2] Jin Bo[2], Mei Sun[2], Xianmin Qing[2] and Zhining Chen[2]

[1]VIRTUS IC Design Center of Excellence, EEE School, Nanyang Technological University, Singapore.

[2]Institute for Infocomm Research (I[2]R), Agency for Science, Technology and Research (A*STAR)

Abstract — **This paper presents our developed two-chip wireless communication system adhering to the IEEE 802.11ad standards with a baseband IC (BBIC) integrated with a low power 60 GHz transceiver SOC (RFIC) and antennas. The novel low power 60GHz RFIC using a sub-harmonic sliding-IF scheme is fully integrated based on low cost SiGe 0.18 um BiCMOS process. The BBIC uses an adaptive time domain equalizer rather than the commonly used frequency domain equalizer to lower the requirements on power consumption.**

Index Terms — Millimeter-wave, System-On-Chip (SOC), RFIC, Baseband IC (BBIC), Antenna, IEEE802.11ad, 60GHz

I. INTRODUCTION

The 60 GHz unlicensed band has been identified as a suitable medium for the operation of short-range wireless system with transmission speed of multi-gigabits per second. Implementation of wireless communication system based on IEEE 802.11ad standard using cost-effective CMOS process has been reported in [1]. Although designed for low power consumption and small form factor, these implementations use Fast Fourier Transform (FFT) based frequency domain equalizer (FDE) to counteract the frequency-selective channel [1]-[3]. This paper presents a low power two-chip communication system solution with a baseband integrated circuit (BBIC) using adaptive time domain equalizer (TDE) and a novel low power 60GHz radio frequency integrated circuit (RFIC), both adhering to the IEEE 802.11ad standard, together with directional antennas. The two SOC chipsets are developed for mobile applications operating in line-of-sight (LOS) environment with relatively small multipath delay spread using single-carrier (SC) modulation. The use of adaptive TDE allows for lower power consumption while lowering the requirement on the hardware size for the equalization process compared to the FDE.

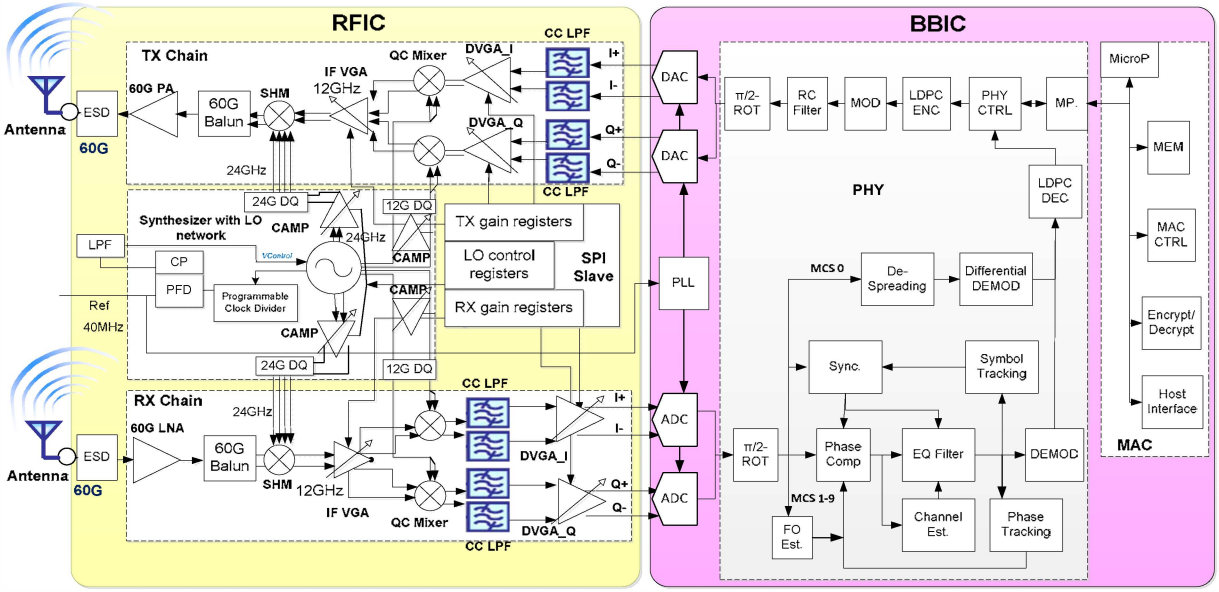

Fig. 1 block diagram of 60GHz RFIC and BBIC

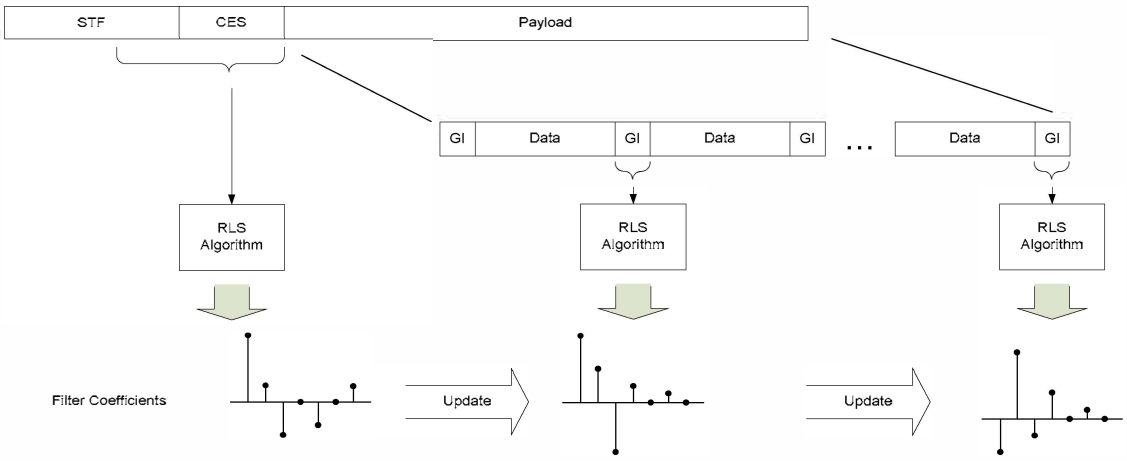

Fig. 2 Adaptive time-domain RLS filter training and tracking

II. TWO-CHIP SYSTEM

Fig.1 shows the system block diagram with the RFIC and the BBIC. The 60GHz RFIC is based on sub-harmonic sliding IF scheme for a low operating frequency requirement of the local oscillator (LO). A K-band synthesizer (22.5~26.23 GHz), which is shared as LO by either TX or RX through LO feed network, is composed of a K-band VCO based on triple-coupled LC tanks, transformer based Injection locked frequency divider (ILFD) and a composite PLL. The LO feed network includes a triple-well single pole double throw (SPDT) switches, a broadband differential quadrature (DQ) converter, which convert differential signals into differential I and Q signals in 11GHz~30GHz, and gain controllable compensation amplifiers (CAMP) i.e. 12GHz CAMP and 24GHz CAMP with gain of about 7~9dB and P1dB of ~7dBm at 12GHz and 24GHz for the optimum drive power level -5~0dBm at LO ports of the mixers. In TX chain, the differential "I" and "Q" signals from baseband are filtered by four sets of cross-coupled (CC) LPFs and then amplified by differential drive DVGAs, with variable gain of -12~8dB. The differential output of 12GHz image rejection up-conversion mixer is amplified by 12GHz differential IF variable gain amplifiers (IF VGA) and then fed into the 60GHz up-conversion sub-harmonic mixer (SHM), connected to 60GHz balun in RF output of the SHM. The 60GHz PA, connected to single-ended port of 60GHz balun, has gain of 20dB, P1dB of 5.6dBm and dedicated ESD protection at the PA output with 60GHz insertion loss of only 0.26dB. In the RX chain, the 60GHz signal is firstly amplified by a LNA with 15dB gain and the output signal is converted to differential by a 60GHz balun, and then the differential signals are converted to 12GHz IF through 60GHz down-conversion SHM pumped by K-band LO. The output IF 12GHz is amplified by 12GHz IF VGA and then fed into the direct conversion mixer with 12GHz LO drive with half frequency of K-band LO. The IF output differential "I" and "Q" signals pass by the proposed passive (CC) LPFs then controlled with gain of 0~30dB by two sets of differentially DC offset cancelling (DCOC) digitally variable gain amplifier (DVGA) operating in the 2MHz~1.9GHz for baseband processing. The PTAT and Bandgap reference are adopted in the DC supply to compensate for temperature changes.

In BBIC, Differential I/Q analogy signals to/from the RFIC are connected to the 6bits DAC/ADC in the BBIC using 3.52 GHz sampling rate in BBIC. The BBIC supports the mandatory data rates, MCS 0 – MCS 4, in IEEE 802.11ad standard as well as the optional data rates, MCS 5 – MCS 9, with the highest data rate at 2.5 Gbps. The BBIC uses a generic 16-bit parallel host interface with a maximum supported throughput of 4.6 Gbps.

Fig. 2 shows the time domain equalization process using an adaptive finite impulse response (FIR) filter. The recursive least square (RLS) algorithm is used to derive the FIR filter coefficients. The RLS adaptive filter coefficients are trained using the preambles, which consist of Golay sequences that have good auto-correlation property. Subsequently, the filter coefficients are updated during the guard interval using the Golay sequence appended to each data block as a form of channel tracking. The equalized Golay sequence is also used to perform symbol and phase tracking to ensure that the symbol and frequency synchronization are maintained throughout the reception of the entire frame and not degraded due to the presence of sampling and carrier frequency offset.

III. PERFORMANCE SUMMARY

The size of the 60GHz RFIC is 3.9 mm x 5 mm and the size of the BBIC is 4 mm x 4mm. The RFIC is mounted on a PCB board with an on-board Antipodal Fermi Antenna (AFA). The IF I/Q ports of RFIC are connected to the BBIC mounted on a separate PCB board. Both PCB boards can be attached to a system debugging platform. The AFA with end-fire radiation

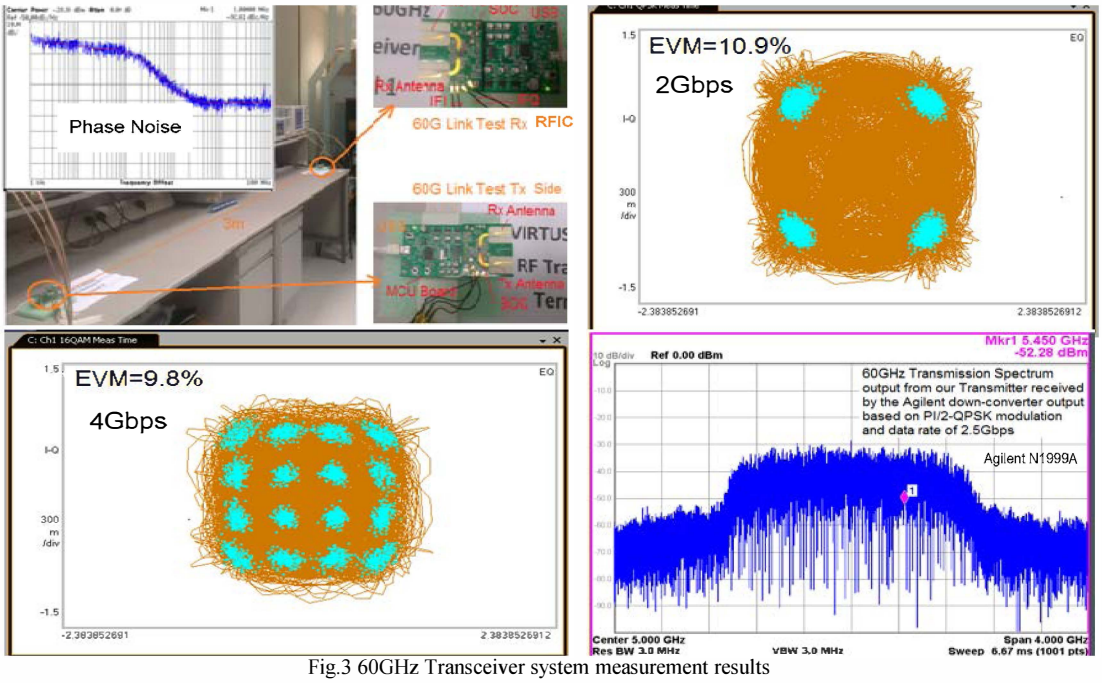

Fig.3 60GHz Transceiver system measurement results

Table I: system specifications

	This Work		[1]	
	RFIC	BBIC	RFIC	BBIC
Technology	180 nm SiGe	65 nm CMOS	90nm CMOS	40 nm CMOS
Supply Voltage	1.8V	1.2 V /1.3 V /2.5 V	1.8 V / 2.5 V	1.1 V / 1.8 V
Chip Size	3.9 mm x 5 mm	4 mm x 4mm	3.6mmx 3.75mm	7.4 mm x 6.3 mm
TX Mode Power	218 mW	500 mW	347 mW	441 mW
RX Mode Power	261 mW	678 mW	274 mW	710 mW
NF	5.5 – 7 dB	N.A.	<7.1dB	N.A.
Maximum Gain	42 dB for RX 34dB for TX	N.A.	N.A.	N.A.
AGC range	36dB for RX 25dB for TX	N.A.	N.A.	N.A.
Phase Noise @1MHz	-98 dBc	N.A.	N.A.	N.A.
Die I/O Pin	64	-	64	-
EI RP	18.7dBm	N.A.	8.5dBm	N.A.

	This Work	[1]	[2]	[3]
Standard	IEEE 802.11ad		N/A	Proprietary
Integration	RF/PHY/MAC	RF/PHY/MAC/USB	RF/PHY	RF/PHY/MAC
Equalization	TDE	FDE		
Channel Tracking	Yes	NA		

is achieved with half-power beamwidths of 18° and 24° in E- and H-planes and a gain of 11~14dBi including the feed line loss. The performance of the measured link phase noise, EVM performance and the transmit spectrum is evaluated based on 60GHz RF transceiver link setup. The transceiver link alone can reach up to 3 meters with TX input of 50mVp-p and Rx output of 100mVp-p. The measured link phase noise as given in the figure is 92dBc at 1MHz offset. The measured EVM for QPSK and 16QAM with a symbol rate of 1GHz are 10.9% and 9.8% respectively as the example case given in Fig.3. The measured transmitter spectrum under modulation is given after down-conversion with Agilent N1999A. The performance of the proposed SiGe based 60GHz RFIC is compared with other published SiGe implementations [4-6], the performance is better and the power consumption is lower than that in [4-6]. To the best of authors' knowledge, it is also the first fully integrated SiGe transceiver SOC.

The BBIC has the size of 4mm by 4mm and uses three supply voltages of 1.2V/1.3V/2.5V and consumes a total measured power of 500 mW and 678 mW in the TX and RX modes respectively. The supply voltage of the RFIC is 1.8V, drawing power approximately 218 mW and 261mW in TX and RX modes respectively.

The comparison of the simulated theoretical BER performance of the system with the measured BER performance for MCS 0 and MCS 5 shows a performance degradation of 3~4 dB as the simulation and measurement results given in Fig.4. Table I lists the characteristics of the developed transceiver chipset with [1] - [4]. The developed integrated two-SOC system use TDE coupled with low power RFIC to lower the requirements on the power consumption and hardware size of the 60 GHz wireless system. The chipset includes antennas, RF, PHY and MAC subsystems based on

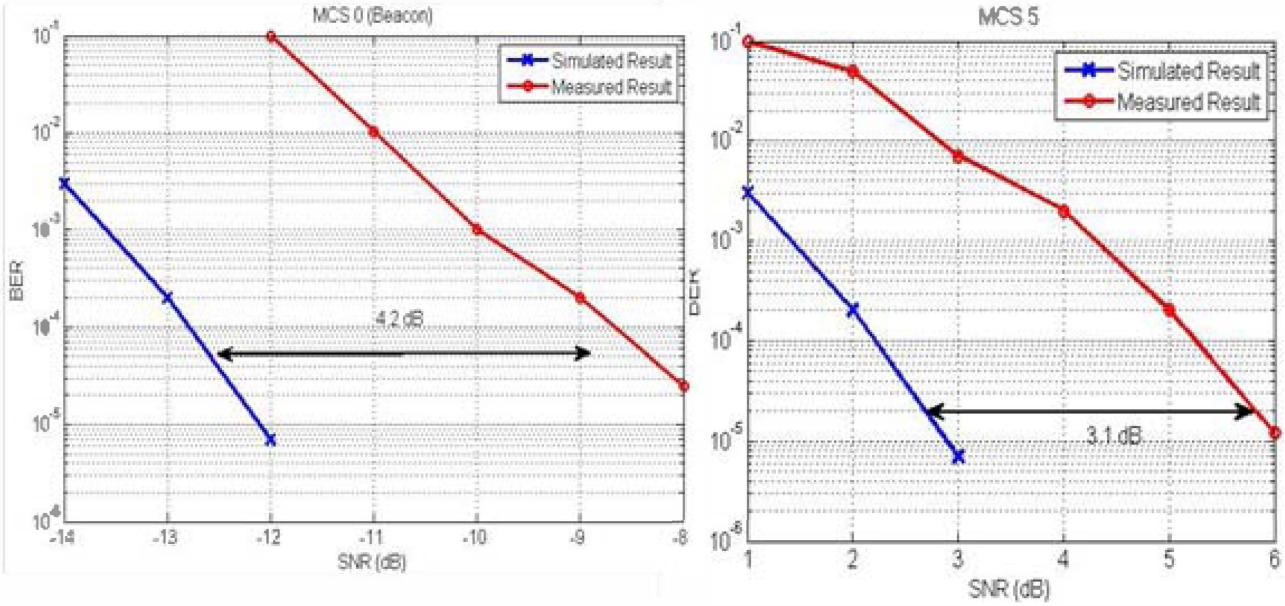

Fig. 4 Simulation and measurement results of the system BER performance

the IEEE 802.11ad standard with a power consumption of only 718 mW in TX mode and 939 mW in RX mode. Based on the setup in Fig.5, the video streaming from DVD to the TV using 60GHz RFIC and BBIC can be done with the communication distances of 10 meters based on MCS0 and 3 meters based on MCS5. The proposed 60GHz solution with RFIC on SiGe and BBIC on CMOS together with the TDE equalization scheme has lower operation power and good communication performance.

ACKNOWLEDGEMENT

This work was financially supported in part by A-STAR, Exploit Technologies Pte. Ltd (ETPL), Singapore and Nanyang Technological University (NTU), Singapore. The authors from NTU are thankful to Tower Jazz Semiconductors for fabrication.

REFERENCES

[1] T. Tsukizawa, et al., "A Fully Integrated 60 GHz CMOS Transceiver Chipset Based on WiGiG/IEEE802.11ad with Built-In Self Calibration for Mobile Applications", ISSCC Dig. Tech. Papers, pp. 230-232, Feb., 2013.

[2] K. Okada et al., "A Full 4-Channel 6.3Gb/s 60GHz Direct-Conversion Transceiver with Low-Power Analog and Digital Baseband Circuitry", ISSCC Dig. Tech. Papers, pp. 218-219, Feb. 2012.

[3] T. Mitomo, et al., "A 2Gb/s-Throughput CMOS Transceiver ChipSet with In-Package Antenna for 60 GHz Short-Range Wireless Communication", ISSCC Dig Tech. Papers, pp. 266-267, Feb. 2012.

[4] S. Reynolds, et al., "60GHz Transceiver Circuits in SiGe Bipolar Technology," ISSCC Dig. Tech. Papers, pp. 442–443, Feb. 2004.

[5] B. Floyd, et al., "A Silicon 60GHz Receiver and Transmitter Chipset for Broadband Communications," ISSCC Dig. Tech. Papers, pp. 218-219, Feb. 2006.

[6] C.-H. Wang, et al. "A 60GHz Transmitter with Integrated Antenna in 0.18μm SiGe BiCMOS Technology", *ISSCC Dig. Tech. Papers*, pp. 659-668, Feb., 2006.

[7] N. Mahalingam, Y. Wang, Kaixue Ma, K. S. Yeo, S. Mou, "A 24 GHz Low Power Low Phase Noise Dual-Mode Phase locked Loop Frequency Synthesizer for 60 GHz Applications," *IEEE Int. Microwave Symposium, 2014(accepted).*

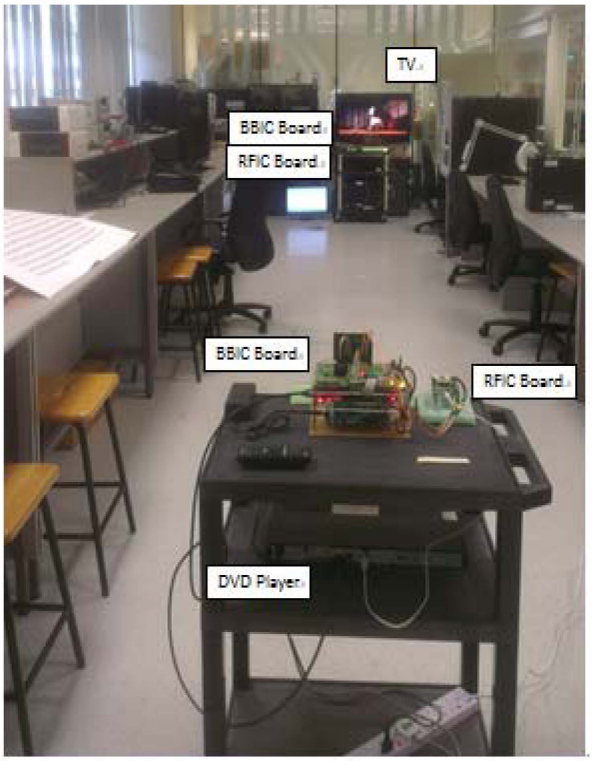

Fig. 5 Video Steaming MCS0 at 60GHz 10 meters between Tx and Rx