Heterogeneously Integrated III-V Laser on Thin SOI with a Compact Optical Vertical Interconnect Access

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Our recent development of the heterogeneous III-V/Si laser from the design, fabrication to experimental demonstration is presented in this letter. The III-V/Si laser design ensures a sufficient light confinement in the bonded active gain medium, effective light coupling been the III-V semiconductor layer and silicon photonic layer, and it can provide a great flexibility in general functional photonic circuits development as the III-V is sitting on silicon without any trenches or predefined silicon waveguide beneath. Fabrication details are given and this heterogeneous III-V/Si Fabry–Pérot (FP) laser with characterized specifications is demonstrated as a proof-of-concept. The fabricated FP laser has a threshold current of 65mA, with the total collected power of 9mW from two facets. Following this proof-of-concept demonstration, more complex laser configuration based on the same platform can be demonstrated.

The heterogeneous III-V/Si platform enables fully-integrated photonic system-on-chip technology, and heterogeneous III-V/Si laser is the key component in this integration technology as it acts as an on-chip light source required for various functional photonic systems [1]. Two fundamental bottlenecks to be solved before on-chip laser source eventually coming into the technology roadmap are: effective light confinement/amplification in the active III-V layer which gives high power efficiency; efficient and compact vertical interconnect structure design to couple the light down to silicon nanowaveguide layer [2].

In the recent reports of hybrid integration platform development, three major integration schemes are provided. The evanescent laser/photodetectors reported in Refs [3, 4] consists of a silicon micro-waveguide under the III-V layer. In fact, the major part of the field is located in the silicon waveguide and only the tail of the optical mode overlaps with the III/V active region. An adiabatic hybrid waveguide mode transformer in Refs [5, 6] has been proposed, which tapers only the III-V waveguide and keep the straight silicon waveguide underneath. It requires the silicon waveguide to have a relatively large cross-section (~ 1 um) to match the effective index of the III-V and silicon layer, Another integration scheme is by exploring BCB interlayer wafer bonding technique [7], of which optical interconnect access through tapering the III-V and SOI waveguide in an opposite direction [8, 9]. A tapering region ~100 um is required for a sufficient light coupling.

A different heterogeneous integration platform is considered in this letter, in which the III-V semiconductor layers are directly bonded on a thin SOI layer and the III-V layers are etched to form a rib waveguide with the underneath SOI layer so that the light can be basically confined in the III-V bonded layer with a proper design of the waveguide width. Light coupling between the Si/III-V waveguide and silicon nanophotonic waveguide is realized through a tapered III-V waveguide and silicon waveguide (i.e., optical vertical interconnect access). Our previous design reports the detailed design of the waveguide and tapering structure for the maximal light confinement and efficient light coupling [10], and experimental result verifies and coupling efficiency could reach ~90% with a tapering length of 50um [11].

In this letter, our recent development of the heterogeneous III-V/Si laser from the design, fabrication to experimental demonstration is presented. Fabrication details are given and this heterogeneous III-V/Si Fabry–Pérot (FP) laser with characterized specification is demonstrated as a proof-of-concept.

Structure Design

Fig. 1 shows the three dimensional and top view schematic drawing of the hybrid III-V/Si laser design. It consists three parts: active III-V gain region, coupling region, and silicon waveguide

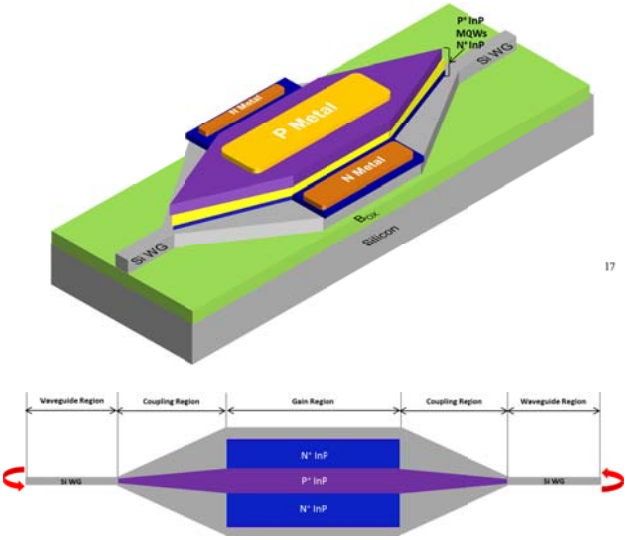

Figure 1: Three dimensional and top view schematic diagram of the laser design. The III-V gain medium is sitting on top of SOI platform with 2 adiabatic tapering to couple the light down to silicon waveguide layer. The laser cavity is formed by the cleaved facet on silicon.

region. The total thickness of the III-V thin film bonded on silicon is 2.2um, and it has a P^+ InP layer, separate confinement heterostructure (SCH) layer, multiple quantum wells (MQWs), and a N^+ InP layer. The detailed layer structure of the III-V wafer can be found in Ref. [12]. The width of the III-V gain region varies from 2 – 3um, and the length varies from 50um to 500um in a step of 50um. The III-V thin film bonded on a 300 nm thick silicon layer is etched until the N^+ InP layer to form a rib III-V waveguide. A short optical vertical interconnect access of 50um long is formed through tapering the III-V and silicon simultaneously in the same direction as shown in the coupling region. In this region, the III-V is completely removed until silicon layer to ensure a good coupling efficiency. In the silicon waveguide region, the silicon waveguide has a width of 600nm and thickness of 300nm, which ensures the structure operating in single-mode regime. It is then tapered from 600nm wide to 4um wide to facilitate the measurement. The FP cavity is defined by the cleaved mirror on silicon waveguide. The total cavity length is about 2mm after cleaving. The hybrid III-V/Si laser design ensures a sufficient light confinement in the bonded active gain medium and effective light coupling between the III-V semiconductor layer and silicon photonic layer. Another key advantage is it can provide a great flexibility in general functional photonic circuit development as the III-V is sitting on top of silicon without any trenches or predefined silicon waveguides beneath.

Fabrication

Fabrication details are given including silicon circuits module, III-V to silicon bonding module, III-V process module, and planarization and metallization module.

A. SOI nano-waveguide fabrication

The silicon nanowaveguide is firstly formed on SOI wafer (from SOITEC). The 100 nm thermal grown silicon dioxide (SiO_2) is used as etching hard mask. The waveguides are patterned by Electron Beam Lithography (EBL) with positive resist PMMA. The CHF_3/Ar gas chemistry is used to open the SiO_2 hard mask in an OXFORD reactive ion etching (RIE) chamber. Vertical outgassing channels are then defined using photolithography. The outgassing channels are to direct any bonding produced gas to the substrate during wafer bonding. After patterning of the outgassing channels, SOI is etched down to a depth of around 300 nm using inductively-coupled plasma (ICP) dry etching technique with HBr/Cl_2 chemistry. Fig. 2(a) shows a top-view SEM image of a silicon waveguide after etching. The silicon waveguide is having a very smooth sidewall.

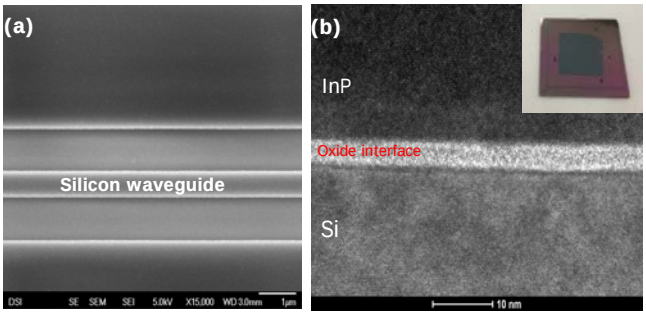

Figure 2: (a) Top-View SEM image of a silicon waveguide after etching. the width of the waveguide is 600nm. (b) TEM image of the bonded III-V to Si pair. The inset shows an image of 10mm*10mm III-V coupon bonded to 20mm*20mm SOI substrate.

B. Low-Temperature Direct Wafer-bonding

After the SOI waveguides formation, both the SOI and the III-V wafers were cleaned by various of chemicals to remove any organic/inorganic particles/contaminations and to make sure the SOI and III-V wafers are clean enough for the bonding. The SOI and III-V bonding pair are activated with oxygen plasma, and then physically joined together and annealed under a pressure of 0.3 MPa at 220 °C for 18 hours. After the bonding, the InP substrate was removed via HCl wet etching. The detailed bonding process descriptions could be found in Ref. [11]. The inset of Fig. 2(b) shows an image of a III-V coupon with a dimension of 10mm*10mm bonded to 20mm*20mm SOI substrate with almost 100% bonding yield. Fig. 2(b) is the TEM image of III-V to Si bonding interface. The interfacial oxide is only about 3nm, which mainly originates from semiconductor native oxide. The InP and Si lattice are clearly seen without any crystal damage or dislocation. The high quality III-V to Si direct wafer bonding is the one of the key challenges of the heterogeneously integration platform development.

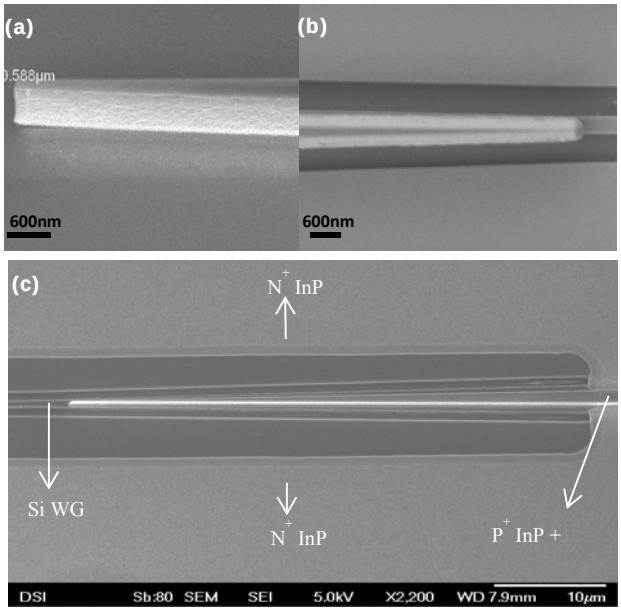

Figure 3: All SEM images are taken at 25°C titled angle. (a) III-V taper after plasma etching of P^+ InP and chemical etching of MQWs. (b) III-V taper and the underneath Si waveguide after patterning and selective dry etching of N^+ InP near the taper tip region. (c) Finished hybrid III-V/Si integration platform after Si waveguide formation, wafer bonding, and multi-step III-V etching process.

C. III-V processing

The III-V mesa was then formed by EBL lithography with negative resist HSQ. In order to make the III-V taper sitting precisely on top of Si taper, the alignment accuracy shall be well controlled within +/- 150nm as the Si waveguide width is only about 600nm wide. The P^+ InP is etched by Cl_2 gas chemistry at elevated temperature of 200°C in inductively coupled plasma (ICP) tool until it reaches the MQWs. The total etching depth is about 1.6um and it's controlled by time. The MQWs are then removed by dipping the sample inside H_2SO_4+H_2O_2+H_2O (1:1:20) solution for 30sec. By chemical etching, damages to the sidewalls of the MQWs can be avoided. In addition, it also ensures the completely removal of the MQWs and to expose the N^+ InP layer, as precise end point control by plasma etch is difficult to achieve. Fig. 3(a) is the 25°C titled SEM image of the III-V waveguide at the coupling region after P^+ InP and MQWs etching. The vertical sidewall profile with

low roughness shows good III-V etching quality. After mesa formation, an additional etching step is required to selectively remove the N^+ InP along the III-V coupling taper and on top of Si nanowaveguide region. The reason is the presence of this thin InP layer will ultimately affect the coupling efficiency and cause light oscillation along the coupling structure. Again, photoresist is used to define the opening area, and Cl_2/BCl_3 is used as the active etching gas at -10°C inside ICP chamber. The low temperature etching is to avoid photoresist overheating and burning. Fig. 3(b) shows an image of the taper tip after low temperature N^+ InP etch. The N^+ InP is completely removed without any residue left on the wafer surface, and exposes the underneath Si waveguide. Fig. 3(c) shows the finished hybrid III-V/Si integration platform after silicon processing, direct wafer bonding, and multi-step III-V etching process. The tapering region is 50um long, and III-V waveguide is sitting on top of silicon without any waveguide structures beneath.

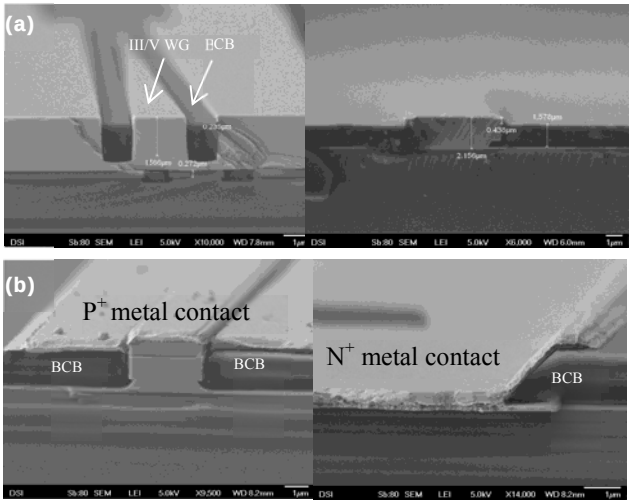

Figure 4: Cross-sectional SEM images of (a) III-V mesa after BCB planarization and etch back; (b) P^+ metal contact and N^+ metal contact to the III-V semiconductor after metallization.

D. Planarization and metallization

After III-V waveguide and taper formation, the whole structure is passivated with 100nm dielectric layer (SiO_2) to protect the side wall of III-V material in order to reduce the surface recombination states. Then the whole chip is spin-coated with CYCLETENE (BCB XU-71918.30 by DOW CHEMISTRY) with a total thickness of 4um. The BCB is subsequently cured in a N_2 oven at a temperature of 250°C for 1 hr. After that, the BCB is etched back to expose the top of P^+ InP inside an ICP chamber with SF_6/O_2 gas mixture. Fig. 4(a) shows the cross-sectional SEM images of a test III-V wafer after BCB etch back. BCB planarization and etching process provides a planarized platform for the subsequent metal layers to sit on, and meanwhile it leaves a very clean and uncontaminated III-V surface for form low resistance ohmic contact. After BCB planarization, the HF chemical clean is applied before any contact metal deposition in order to remove any dielectric / native oxide on sample surface. The P^+ metal consists of Ti/Pt/Au is deposited by E-beam Evaporation on top of III-V mesa. On the other hand, for the N^+ metal side, the BCB is patterned and etched to form a contact via first. The Ni/AuGe/Ni/Au metal stack is deposited then into the via to form the N^+ contact. The final annealing is done at 320°C 60s in a N_2/H_2 gas ambient by Rapid Thermal Processing (RTP) tool. Fig. 4(b) shows the SEM images of the P^+ and N^+ metal contact to the III-V semiconductor after metallization. The final step is to thinning down the substrate to 180um thick and cleaving the chip into 2mm bars for device measurement and characterization.

Fig. 5 shows a microscope image of the fabricated FP laser with compact vertical interconnect access structure. One great advantage of this heterogeneous integration platform is, besides its optical performance, it introduces great flexibility in the fabrication process. In this demonstration, we use bottom-up approach, which starts from silicon waveguide fabrication first. However, the process order could be reversed as the top-down approach, which starts from III-V processing. By reversing the process order, the manufacturing cost, flexibility as well as product yield is able to be further enhanced.

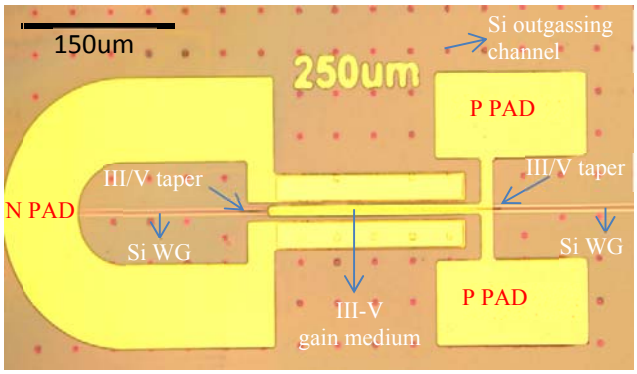

Figure 5: Microscopy image of the fabricated FP laser with compact vertical interconnect access structure.

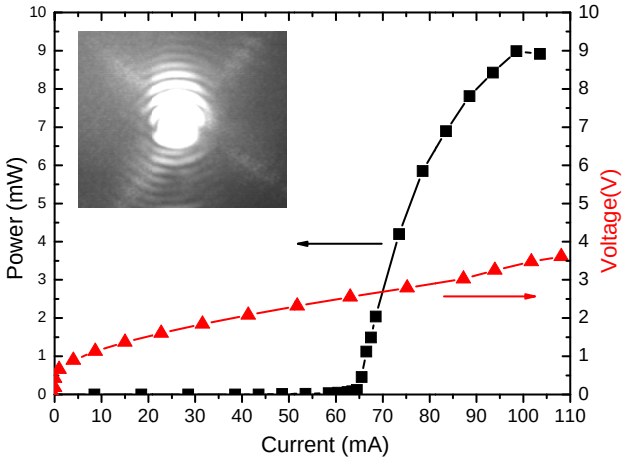

Figure 6: L-I-V curve of the fabricated FP laser with short vertical coupling structure at continuous wave operation. The stage temperature is 20°C. The inset is the lasing light spot at the pumping current of 90mA.

Characterization

The cleaved laser bars are mounted to a copper sub-mount using silver paste for better heat dissipation. It is then placed on a temperature controlled stage set at 20°C for optical characterization. The laser output is focused into an objective lens with N.A. of (), and then coupled into a power meter directly attached at the end of the objective lens. According to theoretical calculation and experimental verification, the light coupling efficiency for the objective lens is about 15% for silicon waveguide dimension of 4um*300nm.

Fig. 6 shows the L-I-V curve of the fabricated laser under continuous wave (CW) operation at a stage temperate of 20°C. The

measured device has a 450um long, 3um wide active III-V gain region. It has two coupling regions with a total length of 100um. The entire cavity length is 2mm defined by the cleaved mirror on silicon nanowaveguide. The threshold current is 65mA under CW. The maximum total collected laser output is close to 9mW at a pumping current of 100mA. The calculated serial resistance of the whole structure is 19Ω, which could possibly be reduced further through process optimization [13]. The slope efficiency is about 33mW/A. The insert of Fig. 6 is the image of the lasing light spot. It shows the laser is operating at single mode regime, as the designed silicon waveguide dimension is 600mm (width) * 300nm (height) which provides strong single mode light confinement.

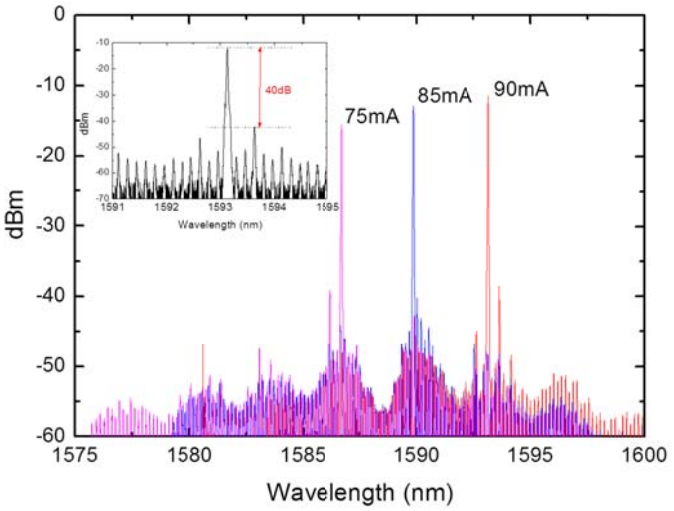

Figure 7: Measured laser spectrum at the pumping current of 75mA, 85mA, and 90mA at 20°C under CW operation. The insert shows the laser spectrum in a smaller wavelength region at the pumping current of 90mA at 20°C.

Fig. 7 shows the laser spectrum collected by a multi-mode fiber placed near the laser facet. The fiber is then connected to the optical spectrum analyzer with a resolution of 0.02nm. The background spectrum is due to spontaneous emission from the gain section coupled to the silicon output waveguide. Another phenomenon observed is the emission wavelength is shifting to higher side at higher pumping current. Similar phenomenon has also been observed by other research groups, and it is believed to be due to the temperature effect [14]. The insert of Fig. 7 shows the laser spectrum in a smaller wavelength range at the pumping current of 90mA. The spectrum clearly shows a Side Mode Suppression Ratio (SMSR) of 30dB at 90mA pumping current.

The further performance improvement could be achieved through two means: 1) process optimization to lower down the overall serial resistance of the device to reduce heating effect; 2) design improvement. In the current heterogeneous III-V/Si platform design, the N+ InP along the III-V taper is removed to have better coupling efficiency. However, it will ultimately affect the pumping efficiency, as there is not sufficient supply of electrons to the III/V tapers due to removed / discontinuous N^+ InP semiconductor. In the other word, the two III-V tapers with a length of 100um only serve as passive waveguide in the current design. Another round of design optimization to overcome this problem is expected to improve the device performance further.

Conclusion

Our recent development of the heterogeneous III-V/Si laser from the design, fabrication to experimental demonstration is presented in this letter. The heterogeneously III-V/Si laser platform design ensures a sufficient light confinement in the bonded active gain medium; effective light coupling been the III-V semiconductor layer and silicon photonic layer; and it also provide a great flexibility in general functional photonic circuits development as the III/V is sitting on silicon without any trenches or predefined silicon waveguide beneath. Fabrication details are given and this heterogeneous III-V/Si Fabry–Pérot (FP) laser with characterized specifications is demonstrated as a proof-of-concept. The fabricated FP laser has a threshold current of 65mA, with the total collected power of 9mW from two facets. Following this proof-of-concept demonstration, more complex laser configuration based on the same platform can be demonstrated.

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