An Optimized Resistance Characterization Technique for the Next Generation Magnetic Random Access Memory

Fei Li, Sunny Yan Hwee Lua, and Aarthy Mani

***Abstract*—This paper presents an accurate resistance characterization technique for magnetic random access memory (MRAM), such as STT-MRAM. By annulling the mismatch effect of CMOS transistors, this technique produces a resistance distribution profile of MRAM devices in a large array that reflects the actual device statistics. A 1Kb array of MTJs with an intrinsic 3σ low resistance state distribution modeled with Verilog-A provides the reference device statistics. Monte Carlo simulation results of popular array configurations show the method's generic advantages of tightened distributions of the mean resistance value and standard deviation (SD) of the characterized 1Kb devices than the reference method. Technology scaling study shows the sustainability of the proposed method with an improvement of the SD of the mean resistance distribution by at least 37.6%. The mean and SD of the standard deviation distribution were improved by at least 25.1% and 67.2% as compared to the reference method, respectively.**

***Index Terms*—Resistance characterization, STT-MRAM, Monte Carlo, Scaling, Distribution**

I. Introduction

NEW generation of magnetic random access memories, such as STT-MRAM, have attracted enormous interests among researchers due to their improved endurance cycle, high speed performance, reduced power consumption and promising scalability, other than Flash memory [1]–[3]. This type of emerging memory technology has been identified to be the candidate for future memory replacement [4]–[6]. Tremendous efforts have been devoted into materials engineering and nano-fabrication to improve the devices' performance and uniformity, and many successful hardware prototypes of these technologies in advanced CMOS process have been demonstrated [5]–[7]. However, the technology is still far from maturity and faces various fundamental challenges [8]–[11]. Mismatch of the MTJ devices' final resistances at both of the logic states poses great challenges in peripheral read/write circuits design for reliable operations.

A holistic approach should be adopted to characterize and examine the MTJ devices' performance together with the CMOS integration. The resistance value of every cell in a memory is essential information for post-fabrication trimming of peripheral circuits, process optimization and yield improvement. It is almost impossible to access every MTJ device inside a memory array, and measure its resistance accurately using the conventional two-point or four-point methods. Under normal operation mode, the master bit line (MBL) and master source line (MSL) of a memory array are normally connected to read/write drivers and sense amplifiers. Under characterization mode, the two-terminals could be multiplexed and accessed externally using laboratory equipment or parametric measurement unit (PMU). However, this method does not reflect the actual resistance value of the MTJ device. Series resistances contributed by the multiplexing switches, column switches and selection transistors, etc. along the access path are also characterized as a whole. Inter-lot, inter-die and intra-die parametric mismatch among CMOS devices exist. The variation of the resistances of the CMOS devices hurdles thorough understanding of the MTJ devices' resistance distribution across all the three levels, delaying the progress of device optimization.

Rao *et al*. proposed a resistance characterization technique that aims to accurately measure the resistance of MTJ devices inside a memory array [12]. A column of replica cells (referred as dummy column (DC) method in the rest of the paper) each containing a transistor same as the selection transistor in the memory cell is added into the memory array. By unifying the circuit components along the access paths to the memory cell and the replica cell, the method indicates a way to cancel out the series resistances along the two paths and characterize the resistances of the MTJ devices. However, the characterization accuracy of this method still suffers from the mismatches of transistors along the two access paths. Transistor mismatch characteristics have been physically characterized to be inversely proportional to the square root of the active gate area, $(1/WL)^{0.5}$, of transistors [13]–[16]. As the technology node scales down, increasing mismatch between transistors complicates the characterization problem further.

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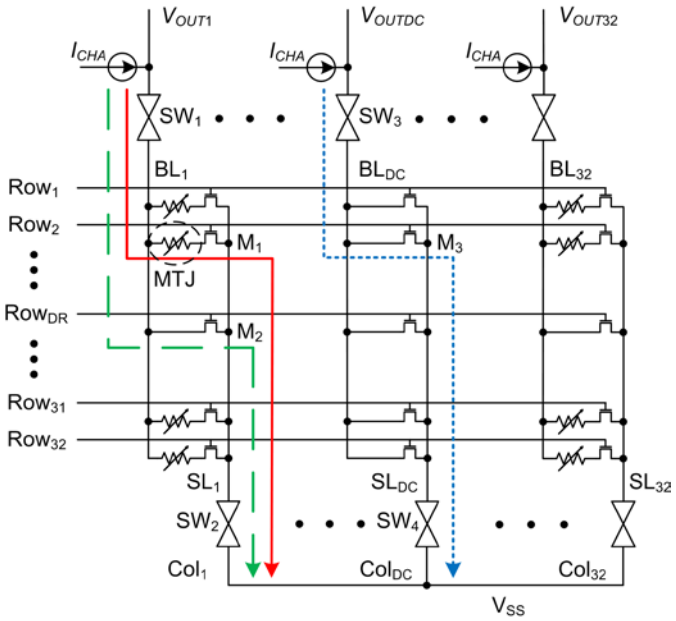

Fig. 1. Simulation setup of the proposed dummy row (DR) and the reference dummy column (DC) resistance characterization techniques.

In this paper, an optimized resistance characterization technique immune to CMOS process variation is proposed by introducing a row of replica cells, referred as dummy row (DR). Section II discusses the working principle of the proposed method. Section III comprehensively presents the results and discussion on the simulation setup, transistor mismatch and technology scaling studies performed using the proposed technique. Conclusions are drawn in Section IV.

II. The Proposed Optimized Resistance Characterization Technique

Fig. 1 depicts the simulation setup and operation principle of the proposed characterization method where STT-MRAM cells are used as a demonstration vehicle. Both the proposed and the reference methods are implemented in the setup to compare their performances. To achieve a balance between an adequate sample size for a representative resistance distribution and a reasonable computation resource, 1Kb normal 1T-1R STT-MRAM cells are arranged in a 32 by 32 array. A row and a column of dummy cells denoted by Row_{DR} and Col_{DC} are inserted at the 17th row and column of the memory array, respectively. Two transmission gate (TG) switches are connected to the bit line (BL) and source line (SL) of each column. A current source is connected to the TG at BL of each column and it pumps in a dc current to the selected memory cell. The TGs at SLs are connected to VSS.

Each transistor in the dummy row is used for characterizing the resistances of the memory devices at the same column. The characterization process of the highlighted MTJ involves the following steps:

1. Select the memory cell and supply current I_{CHA} to this cell. Record the first voltage V_{OUT} at the output node of the current source. V_{OUT} can be expressed as:

$$V_{OUT} = I_{CHA} \times \left(R_{SW1} + R_{MTJ} + R_{M1} + R_{SW2} + R_P \right) \quad (1)$$

TABLE I
Parameters for the Verilog-A MTJ model

MTJ Diameter (nm)		65
JC_0 (MA/cm^2)	LRS➔HRS	4.59
	HRS➔LRS	4.13
RA ($\Omega \cdot \mu m^2$)		7.5
TMR_{mean} (%)		100
Switching (ns)		10
CV		0.0167

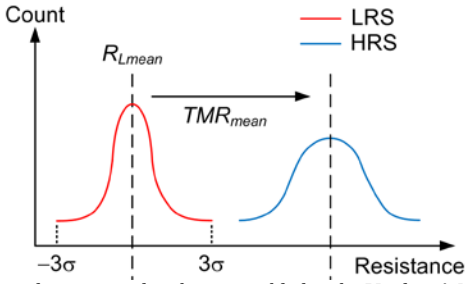

Fig. 2 Statistical resistance distribution enabled in the Verilog-A MTJ model.

where R_{SW1}, R_{MTJ}, R_{M1}, R_{SW2} and R_P are the respective resistances of TG SW_1, MTJ, selector M_1, TG SW_2, and the parasitic resistance of the portion of the BL and SL which the I_{CHA} flows through. The first current path is highlighted by the solid arrow in Fig. 1.

2. Select the dummy cell in the same column of the target MTJ and supply the same current I_{CHA} to this cell. Record the second voltage $V_{OUT}^{'}$ at the same node. $V_{OUT}^{'}$ can be expressed as:

$$V_{OUT}^{'} = I_{CHA} \times \left(R_{SW1}^{'} + R_{M2} + R_{SW2}^{'} + R_P^{'} \right) \quad (2)$$

where R_{M2} and R_{p2} are the respective resistances of selector M_2 and the parasitic resistance of the portion of the BL and SL in which the second I_{CHA} flows. The second current path is highlighted by the dashed arrow. Along this current path, the voltages at the nodes below the MTJ (e.g. the drain of M_2 and the two nodes of SW_2) remain the same as in step 1, therefore, R_{SW2} equals $R_{SW2}^{'}$ and R_{M2} equals R_{M1}.

3. Assuming negligible change of $|V_{DS}|$ and $|V_{GS}|$ for the transistors in SW_1 and M_1 between steps 1 and 2 as well as negligible difference between R_P and $R_P^{'}$, the MTJ resistance of the highlighted cell can be obtained as:

$$R_{MTJ} = \frac{V_{OUT} - V_{OUT}^{'}}{I_{CHA}} \quad (3)$$

In the event of process variation and device mismatch, the only source of variation of the measured MTJ resistance is the mismatch between the two selectors M_1 and M_2 in the proposed DR method. In the case the reference DC method where dummy column is used, the sources of variation include the mismatches between the two pairs of column switches and the two selectors as highlighted by the dotted arrow as shown in Fig. 1. The proposed method is able to reduce the number of transistor mismatch sources by arranging the dummy cells differently. Tighter characterized resistance distribution could be expected using the proposed method. This expectation is verified through Monte Carlo simulation discussed in the next section.

TABLE II
NINE CONFIGURATIONS OF THE TEST ARRAY ARCHITECTURE

Configuration	Column Switch		Selector	
	Type	Width	Type	Width
C1	TG	1.5	NMOS	3
C2		3		1.5
C3		3		3
C4	NMOS	1.5	NMOS	3
C5		3		1.5
C6		3		3
C7	TG	1.5	TG	3
C8		3		1.5
C9		3		3

III. RESULTS AND DISCUSSIONS

STT-MRAM technology with perpendicular anisotropy is used to demonstrate the advantage of our proposed characterization technique. To evaluate the proposed method in improving the resistance characterization accuracy, several designed experiments have been performed and analyzed. The simulation setup and results will be discussed in this section.

A. Statistical MTJ Model

The MTJ characteristics are modeled using Verilog-A language for a balance of simulation accuracy and time. Besides standard MTJ parameters, the Verilog-A model also introduces a location based Gaussian distribution of MTJ resistances that provides a more realistic platform to study the effect of CMOS variation on the characterized MTJ resistances. The parameters for the Verilog-A MTJ model are listed in Table I based on internal process.

The global parameter *CV* defines the location based coefficient of variation of the statistical distribution of low resistance R_L and tunnelling magnetoresistance (*TMR*) over their mean values R_{Lmean} and TMR_{mean}. The two parameters follow a 3σ distribution. The values R_H of high resistance state (HRS) are determined by the values of R_L and *TMR* as in (4); therefore have a larger standard deviation (SD) and smaller maximum count as shown in Fig. 2.

$$R_H = R_L \times (1 + TMR) \tag{4}$$

B. Transistor Mismatch Effect

The mismatches among column switches and selectors have been identified as the key to the accuracy of the characterized MTJ resistances in Section II. To verify the generic advantages of the proposed DR characterization method, nine configurations of the arrays with different types and sizes of column switch and selector are adopted in simulation as listed in Table II. TG and NMOS transistor are selected as the column switch and selector since they have been frequently used in the literature [17]–[19]. The widths of the selectors are chosen to ensure adequate current driving capability to switch the MTJ states.

500 Monte Carlo simulation runs have been conducted for each array configurations using GlobalFoundries 180 nm process library to understand the transistor mismatch effect on the resistance characterization accuracy using the proposed DR, reference DC and direct measurement (DM) methods.

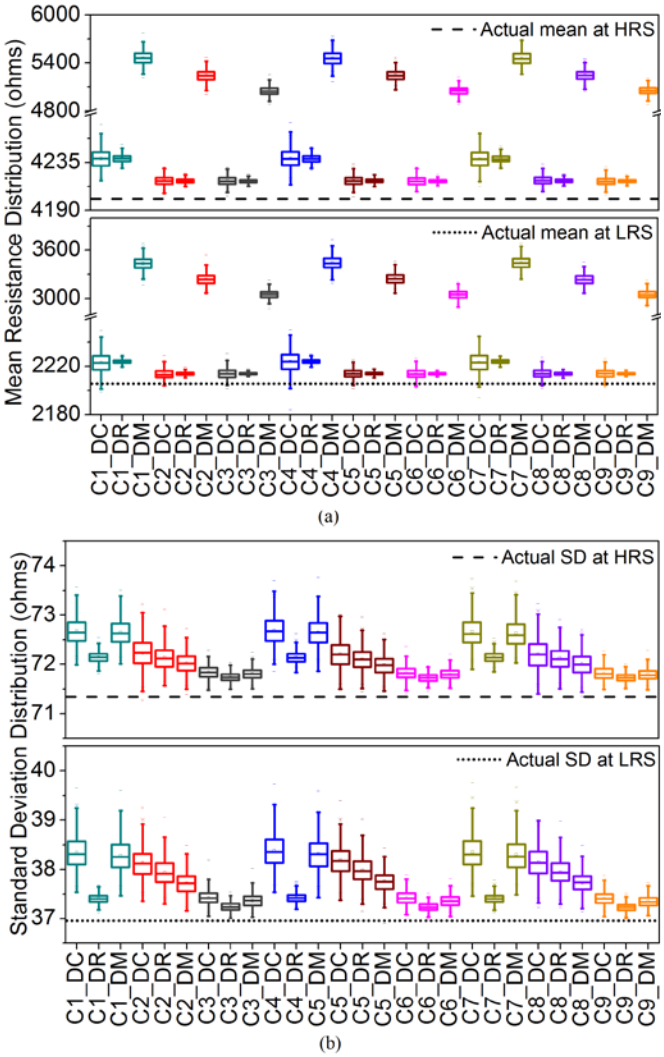

Fig. 3. Distribution plots of (a) the mean value and (b) the standard deviation of the characterized resistance of the 1 Kb MTJ devices at HRS and LRS with nine test configurations using the DR, DC and DM methods, over 500 Monte Carlo runs.

The resistance value for the DM method is obtained by dividing V_{OUT} in (1) with I_{CHA}, therefore it includes the resistances of two column switches and a selector. The distributions of the mean value and SD of the characterized resistance of the 1Kb MTJ devices over 500 runs are used as the indicators of the accuracy of the characterization methods. Characterization current of 30μA is used in this analysis to achieve a balance between low read disturbance and easy read out of analog signals.

Fig. 3(a) depicts the box plots of the distributions of the characterized mean resistances for both HRS and LRS. Each state has nine groups of box plots that correspond to nine test configurations. Each group consists of three box plots using the DC, DR and DM methods. The actual mean resistance values for both states are also plotted. The mean values and SDs of the distributions of both DC and DR methods are much smaller than the DM method. The mean values of the distributions obtained with both DC and DR methods are nearly the same, but the proposed DR method can achieve

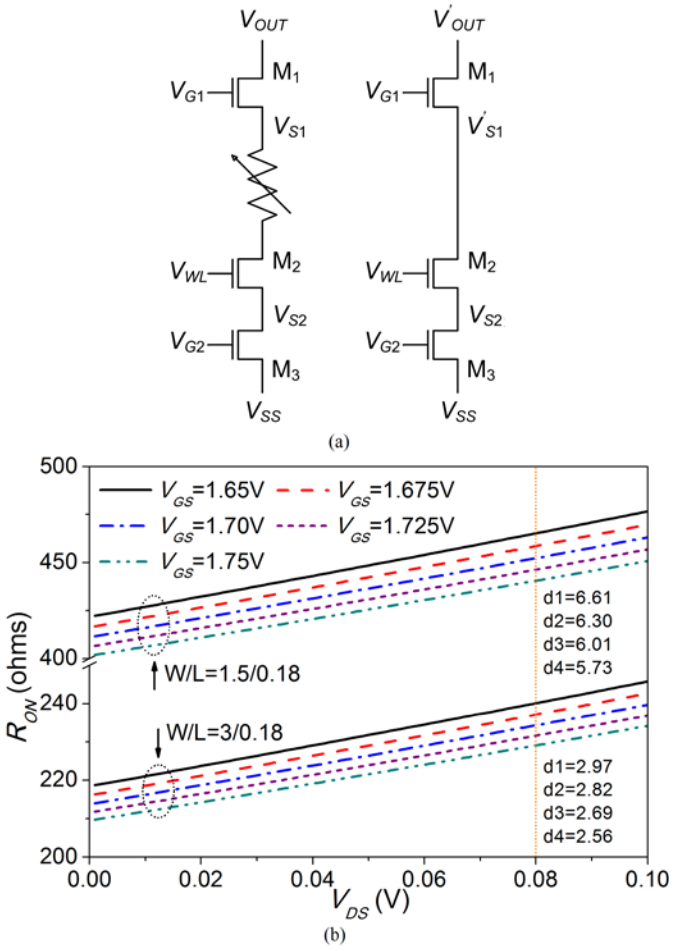

Fig. 4. (a) Schematic of the normal and dummy cell current paths with NMOS as the column switches and selector. (b) Plot of R_{ON} as a function of V_{DS} with five V_{GS} values for transistors with sizes 1.5/0.18 um and 3/0.18 um in triode region during characterization operation The corresponding value difference between R_{ON} at V_{DS} = 0.08 V (with the dotted line serves as a guide to the eyes) for different V_{GS} are displayed.

tighter distributions with an average of 59.1% (76.7%) reduction of the SD at HRS (LRS) states for all the nine test configurations evaluated than the DC method. It also can be observed that the characterized mean values are larger than the actual mean value for the majority of the simulation conditions and runs. This observation will be discussed in Section III.C.

Fig. 3(b) shows the box plots of the standard deviation distributions of the characterized resistance for both HRS and LRS. The actual SD of the 1Kb devices is plotted as well. The figure shows that the proposed DR method can achieve tighter standard deviation distributions with an average of 40.8% (26.5%) reduction in the SD and smaller mean values with an average of 0.34% (1.17%) reduction at HRS (LRS) than the reference DC method for all nine test configurations. The DR method is able to achieve similar improvement over the DM method for most of the configurations. It proves that the DR method is able to reduce the process variation and mismatch by annulling the effects from the column switches.

In the DR method, the widths of the column switch and selector have stronger influence on the characterization accuracy than their types. Test configurations with narrower column switch (C1, C4, and C7) lead to wider difference between the characterized and actual mean resistance. Test configurations with narrower selector (C2, C5 and C8) results in broader spread of the standard deviation distributions. The former observation is related to the assumption (negligible change of $|V_{DS}|$ and $|V_{GS}|$) made in the derivation of (3), and the latter is due to higher effect of process variation and mismatch on smaller transistors.

TABLE III
MTJ AND SIMULATION PARAMETERS
USED IN THE TECHNOLOGY SCALING STUDY

CMOS node (nm)		90	45
V_{DD} (V)		1.2	1.1
MTJ Diameter (nm)		55	45
JC_0 (MA/cm^2)	LRS➔HRS	6.41	9.59
	HRS➔LRS	5.77	8.63
RA ($\Omega\cdot\mu m^2$)		3.58	2.22
I_{CHA} (μA)		20	18.33

C. Validity and the Effect of the Assumptions

Three assumptions have been made to derive the MTJ resistance in (3), which are negligible change of $|V_{DS}|$ and $|V_{GS}|$ of transistors in SW_1 and the selector and negligible difference of parasitic resistances between the normal cell current path and dummy cell current path. The last assumption can be easily achieved through layout techniques. The validity of the first two assumptions directly affects the accuracy level of the characterized resistance. For simplicity purpose, NMOS is used to illustrate the effect of these assumptions. The ON resistance of a NMOS transistor in linear region can be expressed as (5), where it is shown to be proportional and inversely proportional to V_{GS} and V_{DS}, respectively.

$$R_{ON} = \frac{1}{\mu_n C_{ox}(W/L)(V_{GS} - V_{th} - 0.5V_{DS})} \quad (5)$$

Fig. 4(a) shows the schematic of the normal and dummy cell current paths with NMOS selected as the column switches and selector. When the MTJ is removed, V'_{S1} becomes smaller than V_{S1} therefore V'_{GS1} is greater than V_{GS1}. According to (4), the change of V_{GS} and V_{DS} of M_1 causes R'_{M1} to become smaller than R_{M1}. Therefore, (3) can be re-written as:

$$R'_{MTJ} = R_{MTJ} + \left(R_{M1} - R'_{M1}\right) \quad (6)$$

where R_{MTJ} is the theoretical MTJ resistance. This analysis can be applied to the TG based column switches and selector configuration, and the similar observation can be obtained. Eqn. (6) explains the observation of higher characterized mean resistance than the actual value in Fig. 3(a). Fig. 4(b) plots the value of R_{ON} as a function of V_{DS} under five different V_{GS} values for transistor with size 1.5/0.18 and 3/0.18 during the characterization operation. The corresponding value differences between adjacent R_{ON} at V_{DS} = 0.08 V under the five V_{GS} are also shown in the figure. The change of V_{GS} is small due to the small characterization current supplied; therefore the difference in R_{M1} can be neglected as compared to the actual MTJ resistance. Higher value differences between R_{ON} observed with narrower transistors and it explains the higher characterized mean resistances with configuration C1,

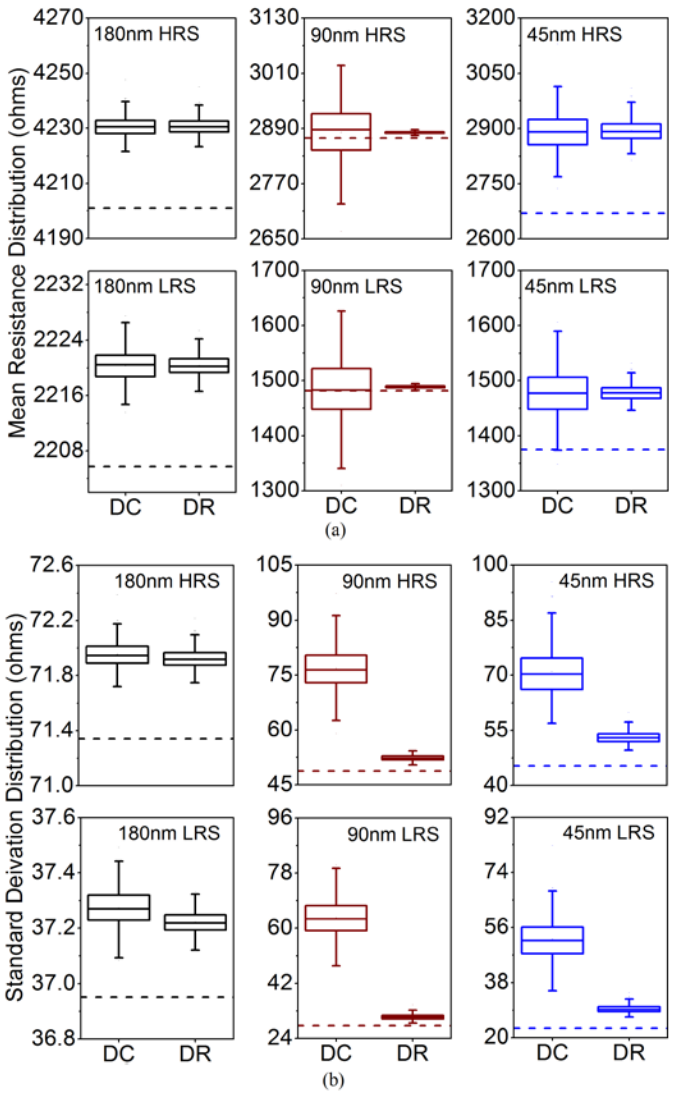

Fig. 5. Distribution plots of (a) the mean and (b) the SD distributions of the characterized resistance of 500 Monte Carlo runs with test array configuration C1 using the DC and DR methods.

C4 and C7 in Fig. 3(a).

D. Technology Scaling Study

To verify the method is able to serve as a scalable solution as the technology node continues to scale down, the experiment in Section II.B was repeated using array configuration C1 at 180nm, 90nm and 45nm technology nodes with Cadence generic BSIM model. A systematic approach with a constant J_{C0}·RA/V_{DD} approach is adopted from [20] to scale the MTJ and circuit parameters. Table III shows the scaled parameters at 90nm and 45nm nodes while the parameters at 180nm remains the same as in Table II. The transistors' W/L ratios are kept constant in this study. Only the DC and DR methods are analyzed in this study as they are able to produce distributions much closer to the true device statistics.

Fig. 5 shows the Monte Carlo simulation results of the distributions of the characterized mean resistance value and standard deviation of the MTJ array for both the HRS and LRS. It can be observed in Fig. 5(a) that the DR method is able to produce a much tighter mean resistance distribution than the DC method as the technology node scales down to 90nm and 45nm for both MTJ states. The characterized mean resistances are higher than the actual mean value as explained previously. At 45nm node, the discrepancy between the measured and actual mean resistance is larger than 180nm and 90nm nodes, showing higher impact of (5) due to smaller devices at the more advanced technology node. Fig. 5(b) shows the increased discrepancy between the characterized and actual values at 90nm and 45nm as compared to 180nm due to higher process variation at advanced technology nodes. However, the DR method has greatly reduced the SD of the measured mean resistance over the DC method for both resistance states. The percentages of reduction in the mean value and SD of the two distributions at 45nm and 90nm nodes are tabulated in Table IV. As compared to the DC method, the proposed DR method greatly tightened the SD of the mean resistance distribution by at least 37.6%. The mean value and SD of the standard deviation distribution were improved by at least 25.1% and 67.2% as compared to the DC method, respectively.

TABLE IV
IMPROVEMENT OF THE MEAN AND SD DISTRIBUTIONS OF THE PROPOSED DR METHOD WITH RESPECT TO THE DC METHOD

		Mean Distribution		SD Distribution	
		HRS	LRS	HRS	LRS
90nm	Mean	0.03%	-0.34%	31.85%	51.16%
	SD	95.92%	95.76%	87.75%	86.43%
45nm	Mean	-0.07%	-0.05%	25.13%	43.60%
	SD	37.58%	67.23%	74.81%	67.23%

IV. CONCLUSION

The knowledge of the true resistance distribution of the resistive MTJ devices in an array plays a key role in the process and material optimization, peripheral circuit design and post fabrication performance trimming of the next generation MRAM technology. This paper proposed an improved resistance characterization technique of integrating a row of dummy cells inside the MRAM array. The technique unifies the current paths of the target MTJ cell and the dummy cell to the same column switches therefore greatly reduces the effect of CMOS process variation and device mismatch on the characterized device resistance. Measured device resistances are closer to the actual values with a tighter distribution than the reference method. The advantages of the technique were verified using nine array configurations of different types and sizes of column switches and selectors through Monte Carlo simulation. Technology scaling study performed demonstrates the sustainability of our proposed method as the CMOS technology scales from 180nm down to 45nm.

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