Dynamic Stress Modeling on Wafer Thinning Process and Reliability Analysis for TSV Wafer

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***Abstract*— Through-silicon-via (TSV) technology permits devices to be placed in the third dimension. Currently, there is a strong motivation for the semiconductor industry to move to 3-D integration using the TSV approach due to its many advantages. However, there are some challenges for TSV wafer processes. One of the challenges is TSV wafer thinning process (WTP). In this paper, a dynamic finite element modeling methodology was established and used to study the TSV WTP-induced wafer stress. It was found that wafer surface roughness, TSV wafer thickness, bonding/debonding material, and TSV feature size have impact on TSV wafer stress under the TSV WTP. The impact of wafer thinning-induced stress on mobility change was also discussed in this paper.**

***Index Terms*— Dynamic modeling, finite element analysis (FEA), reliability, through-silicon via (TSV), wafer thinning.**

I. Introduction

IN A 3-D chip, multiple device layers are stacked together with direct vertical interconnects. Therefore, one of the most important benefits of a 3-D chip over a traditional 2-D design is the reduction on global interconnect. There are various vertical interconnect technologies, including wire bonding, microbump, Cu pillar, and through-via vertical interconnect [1]. The 3-D integration using the through-silicon-via (TSV) approach becomes one promising technology in 3-D packaging due to many advantages [2], such as higher clock rates, lower power dissipation, and higher integration density. However, there are several challenges associated with TSV fabrication and TSV wafer processes. Most of the challenges are process-related, such as reducing Cu overburden with achieving void-free filled Cu TSV [3], Cu protrusion [4], wafer warpage control [5], wafer thinning process (WTP), bonding/debonding process [6], thermal-induced reliability issues [7]–[9], and so on. This paper focuses on the TSV WTP-induced reliability problems.

In this paper, a dynamic finite element analysis (FEA) modeling methodology has been developed for WTP for the first time to study the wafer thinning-induced stress and its effect on TSV wafer reliability. It was found that the wafer surface roughness (WSR) is one of the very important parameters affecting silicon (Si) wafer stress-induced by WTP. From a physical WTP, typical roughness value (Ra) is several hundred nanometers for rough grinding, 20–50 nm for fine grinding. The FEA simulation results showed that large roughness, which usually is related to fast feeding rate and coarse grinding process, leads to high-wafer stress. Wafer thickness is another important parameter affecting TSV wafer stress. Simulation results showed that wafer stress increases with decreasing wafer thickness, which brings a challenge for WTP, because a thinned TSV wafer is prone to brittle failure due to large stress. In this paper, the effect of bonding material and thickness on TSV wafer stress were also modeled. The effects of TSV design, such as via diameter, depth, and pitch, on wafer stress were investigated. Simulation results can be used to understand wafer thinning-induced reliability issues and to optimize the TSV WTP to reduce wafer stress.

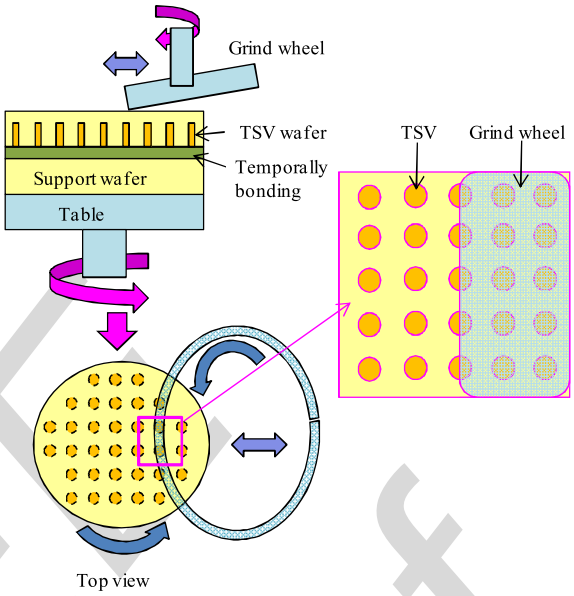

Fig. 1. Schematic diagram of the TSV WTP.

II. Experimental Procedures

The TSV fabrication was done on the eight inch Si wafer with an initial thickness of 750 μm. After that, the TSV wafer was thinned down to the desired thickness, such as 50 or 100 μm, and then the TSV backside was revealed for the subsequent redistribution layer process and interconnection. Fig. 1 shows a schematic view of TSV WTP. The TSV wafer was mounted onto the support wafer using the temporally bonding/debonding process. The support wafer

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TABLE I
PARAMETERS USED IN THE WTP

Parameters	Rough Grind	Fine Grind
Spindle Speed	2500 rpm	3200 rpm
Chuck Speed	150 rpm	150 rpm
Feed Speed 1	150 μm/min	40 μm/min
Feed Speed 2	80 μm/min	20 μm/min
Air Cut	50 μm	50 μm
Removal amount	20 μm to 650 μm	20 μm to 50 μm
Coolant	DI water and Air	DI water and Air

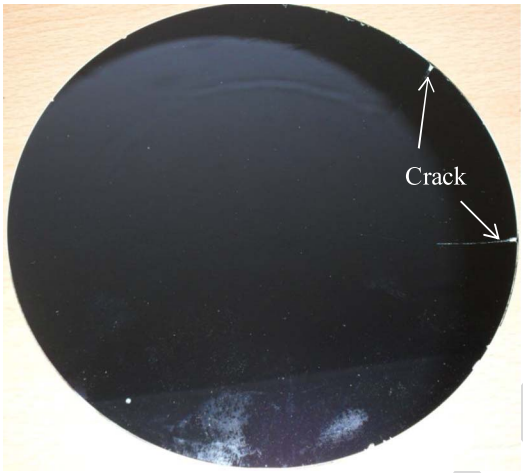

Fig. 2. Wafer cracking due to thinning process.

was then mounted onto the table of the thinning machine. Grinding angle of 20° was used during the thinning process. Table I lists the typical parameters used in the WTP. In the thinning process, coarse grinding was carried out first using a rough grind wheel with mesh sizes of #320 until the TSV wafer thickness reached <150 μm. Then, fine grinding was carried out using a fine grind wheel with mesh sizes of #2000. After fine grinding to 50 μm, stress relief by removing 2-μm silicon through the chemical mechanical polishing (CMP) process was further carried out to smooth the wafer surface. Typical Ra is several hundred nanometers after rough grinding, 20–50 nm after fine grinding and 10 nm or less after the CMP process.

The common defects under the thinning process include edge chipping and wafer cracking, as shown in Fig. 2. For TSV WTP, wafer cracking is along the TSV edges and then the cracks pass through the adjacent TSVs, as shown in Fig. 3. The Cu TSVs have different material properties from the Si die and the vias can be regarded as inclusions embedded in the Si matrix. Extensive studies have shown that inclusions disturb the stress field and can cause stress concentration in their neighborhoods [10], [11]. The evaluation of reliability under TSV WTP is essential to optimize the TSV thinning process. The FEA modeling is one of the desirable tools for optimization studies, which was used in this paper for WTP simulation.

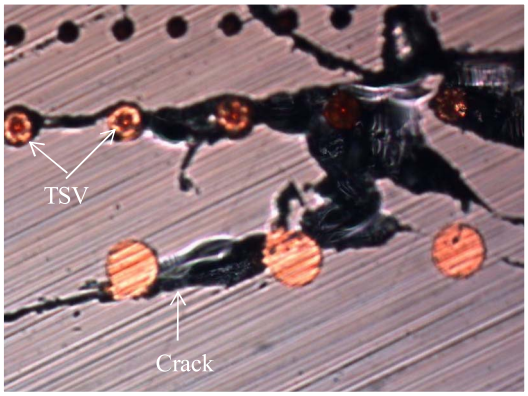

Fig. 3. Cracks along TSVs-induced by WTP.

III. FEA APPROACH

In this paper, a dynamic FEA modeling methodology was developed for the WTP using the ANSYS/LS-DYNA commercial software. To simulate the WTP-induced stresses around TSVs, a dynamic modeling method was established to simulate the effect of surface roughness of the TSV wafer. Different surface roughness represents different grinding processes. Fig. 4 shows a basic 2-D plane strain FE model including one TSV. The WSR effect was modeled by surface bumps with an equivalent height as Ra. The worst case of TSV just located under the bump was simulated. In the FE model, a 700-μm-thick support Si wafer was simulated. A thinned TSV wafer is attached on the support wafer through a bonding material layer of 20-μm thickness. The Cu TSVs are surrounded by Si material. The TSV has a feature size of 20 μm in diameter, 50 μm in depth, and 100 μm in pitch. It can be observed from Fig. 1 that several TSVs were covered by grind head simultaneously. The effect of adjacent TSVs each other should be considered in the FE modeling. Therefore, the simulated stress convergence study was carried out by modeling the different number of TSVs in FE model, as shown in Fig. 5.

Boundary condition was carefully defined in the 2-D plane strain model. The bottom of the support wafer was fixed in all directions. Nodes on the two vertical edges were coupled with displacement in the horizontal direction. The top surface of TSV wafer is free. Grinder was modeled as a rigid body. The maximum relative speed of grinder and wafer occurs at the edge of the TSV wafer. The calculated speed based on thinning parameters was applied onto a grinder as an input constant velocity. Surface-to-surface contact pair between the grinder and wafer surface was defined. The friction effect between grinder and TSV wafer surface was modeled. When the high-speed grinder impacts on the simulated bump on the TSV wafer surface, this impact load introduces dynamic stress in the TSV wafer.

To justify 2-D model is sufficient for WTP simulation, 3-D model was also built for comparison. Fig. 6 shows 3-D FE models including one TSV model and 5 × 5 array TSVs model. Similar with the 2-D model, boundary condition was defined in the 3-D model with the bottom of the support

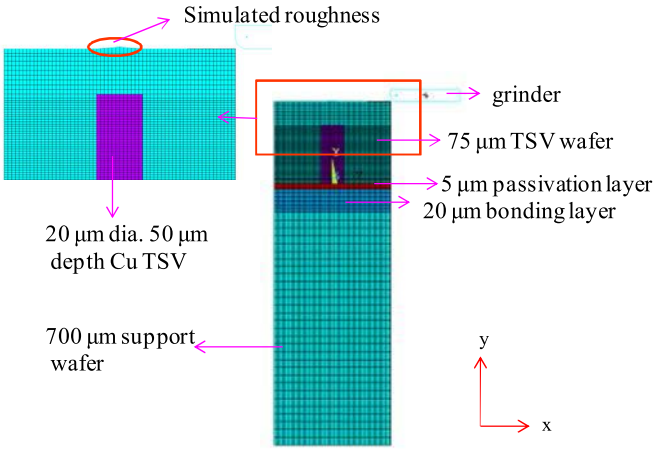

Fig. 4. 2-D FE model with one TSV unit.

TABLE II
MATERIAL PROPERTIES USED IN THE FE MODEL

Materials	Young's modulus (GPa)	Poisson's ratio	Density (kg/m^3)
Silicon	131	0.28	2330
Copper	117	0.35	8960
Dielectric	1.3	0.3	2000
Bonding	1.79	0.35	1500

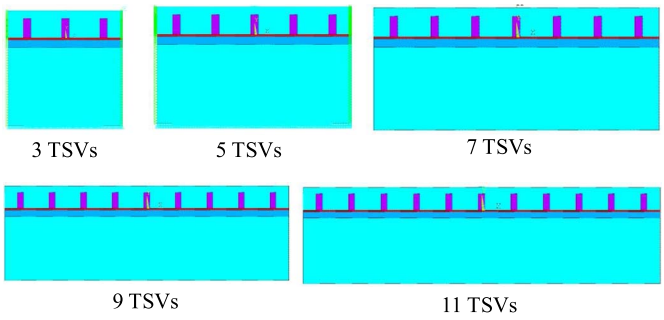

Fig. 5. 2-D FE models with different number of TSVs.

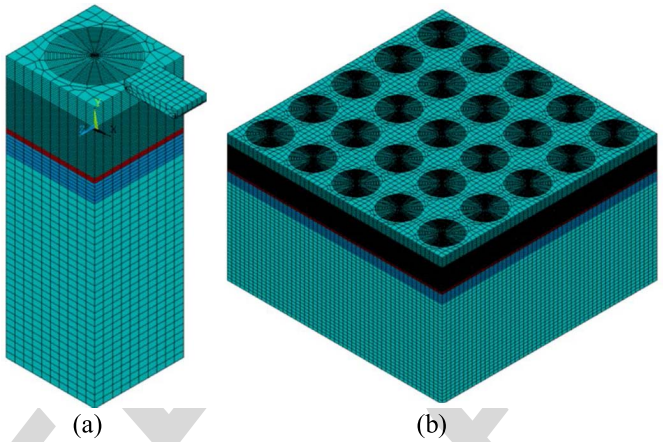

Fig. 6. 3-D FE models. (a) Model with one TSV. (b) Model with 5 × 5 array TSVs.

wafer was fixed and nodes on the four side walls were coupled accordingly. The other parameters in the 3-D model, such as friction, contact pair, and loading condition, were the same as the 2-D model.

During WTP, the heat generated is caused by the friction between the grinding wheel and the wafer surface. Moulik *et al.* [12] developed a model using a heat source and pressure as inputs to study temperature distribution and thermal residual stresses in grinding process. The results showed that temperature is much localized and the surface residual stresses are tensile [12]. The coolant was commonly used in the WTP to prevent tooling damage, remove particle, and importantly remove heat generated by grinding process. Abdelnaby *et al.* [13] simulated the heat generation during silicon wafer back grinding process. It was found that the temperature of the wafer decreases rapidly to the ambient temperature of 23 °C and the coolant temperature does not change during the thinning process [13]. Materials used in the microelectronics usually show the temperature-dependent properties, which affect the stress value when subjected to thermal loading. However, the wafer temperature is similar to the ambient temperature during the WTP due to the coolant application. Therefore, temperature-independent properties were used for all materials. Table II lists the materials and their mechanical properties used in the FE modeling. The Cu TSV was modeled with a bilinear kinematic hardening plastic behavior. Other materials, Si, dielectric, and bonding material, were modeled with only elastic behavior.

IV. RESULTS AND DISCUSSION

A. Effect of the Number of the Modeled TSVs in 2-D Model

The FE model with 800-nm Ra and 75-μm TSV wafer thickness were simulated. Fig. 7 shows the simulation results of first principle stress for the 2-D FE model with five TSVs. The stress concentrates around TSV at the area of the interface between the TSV wafer and bonding material layer. Such high-stress concentration could damage the wafer or devices. Fig. 8 shows the effect of the number of modeled TSVs in one 2-D FE model (refer to Fig. 5) on wafer stress. Modeling one TSV in the 2-D FE model is not enough, because the effect of adjacent TSV is not considered. The maximum TSV wafer stress increases with increasing the number of TSVs included in one 2-D FE model. The maximum stresses of both principal stress (S1) and von Mises stress (Svon) are converged and stable, when modeling five or more TSVs in one 2-D FE model.

B. Comparison Between 2-D and 3-D Models

Fig. 9 shows the comparison of the maximum TSV wafer stresses between 2-D and 3-D models. For FE model with one TSV, both 2-D and 3-D models result in the similar maximum principal stress and the 2-D model leads to slightly larger Svon than the 3-D model. For FE model with five TSVs for 2-D model and with 5 × 5 array TSVs for 3-D model, both 2-D and 3-D models result in the similar maximum

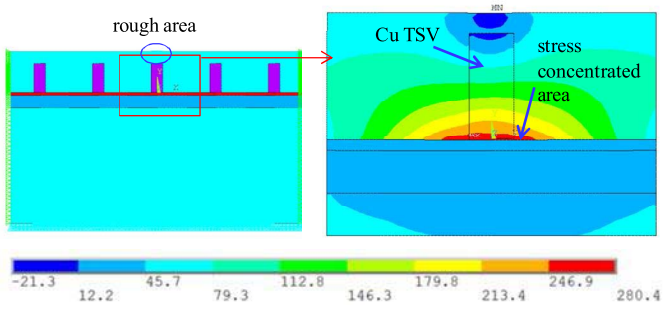

Fig. 7. Stress contour of first principal stress.

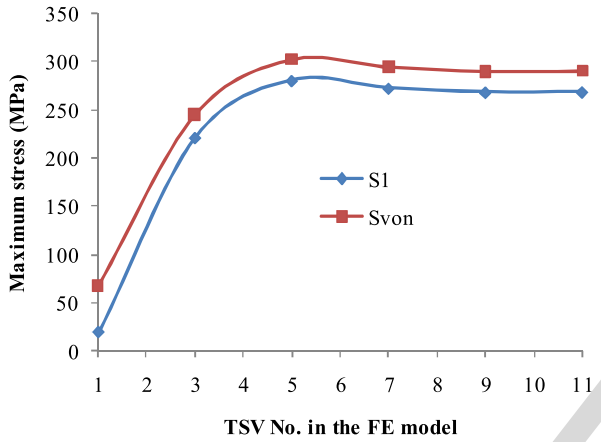

Fig. 8. Effect of the number of modeled TSVs on wafer stress.

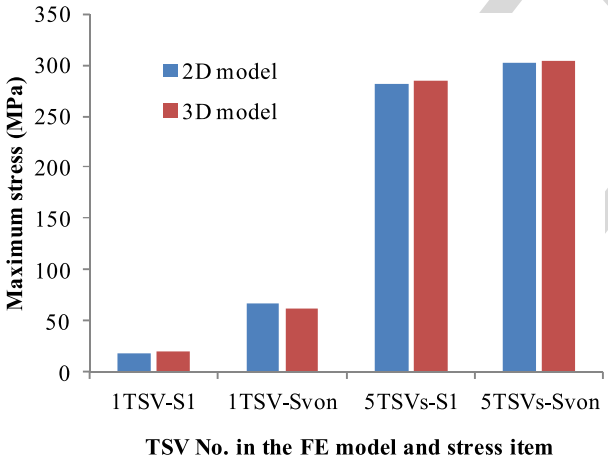

Fig. 9. Comparison of the maximum TSV wafer stresses between 2-D and 3-D models.

principal stress and Svon. When modeling five TSVs for 2-D model and 5 × 5 array TSVs for 3-D model, the TSV wafer stress distribution along the cutting path through five TSVs is almost the same for 2-D and 3-D models, as shown in Fig. 10. Table III lists the relative comparison of computing resources between 2-D and 3-D models by considering 2-D model with one TSV as a reference. It can be seen that computing resources, especially for solving time, increase significantly for 3-D model with more TSVs, which is not realistic to use 3-D model to do parametric study. Based on

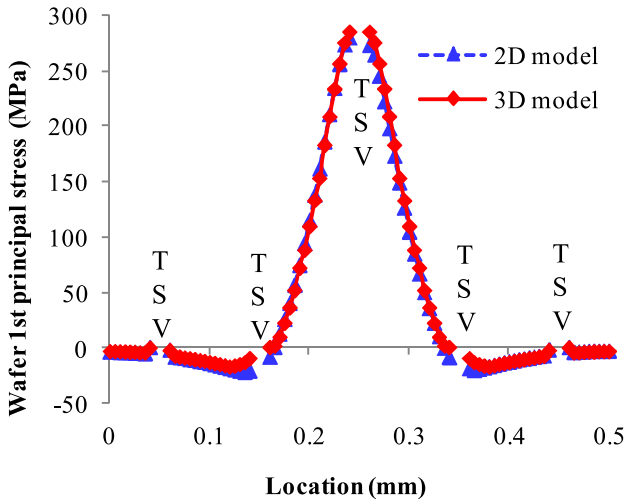

Fig. 10. Comparison of first principal stress along the cutting path through five TSVs between 2-D and 3-D models.

TABLE III
RELATIVE COMPARISON OF COMPUTING RESOURCES BETWEEN 2-D AND 3-D MODELS

FE model	Model size	Solving time	Result file size
2D-1TSV	1	1	1
2D-5TSVs	5	7	13
3D-1TSV	10	15	20
3D-5x5TSVs	250	2000	1100

stress comparison between 2-D and 3-D models and the effect of modeled TSV on the simulated stresses discussed in Section IV-A, the 2-D FE model with five TSVs was sufficient for the TSV WTP simulation due to accurate simulation results and acceptable model size, and short solving time. The 2-D FE model with five TSVs was implemented in the subsequent parametric studies.

C. Effect of TSV WSR

From a physical WTP, typical Ra is several hundred nanometers after rough grinding, and 20–50 nm after fine grinding. In this paper, four different Ras of 800, 400, 200, and 100 nm were simulated to investigate the effect of roughness on TSV wafer stress under WTP. The used FE model consists of five TSVs with 20-μm via diameter, 50-μm depth, 100-μm pitch, 75-μm TSV wafer thickness, and 20-μm bonding thickness. Fig. 11 shows the effect of TSV WSR on wafer stress (first principal stress) along the interface between the TSV wafer and bonding layer. The maximum stress occurs at the edge of TSV with surface roughness setting (bump with an equivalent thickness) above it. It was found that the WSR is one of the critical parameters affecting silicon stress under the WTP. Fig. 12 shows the relationship between the maximum stress and TSV WSR. The principal stress and Svon have the similar value and trend with changing surface roughness. Stress increases significantly with increasing TSV WSR.

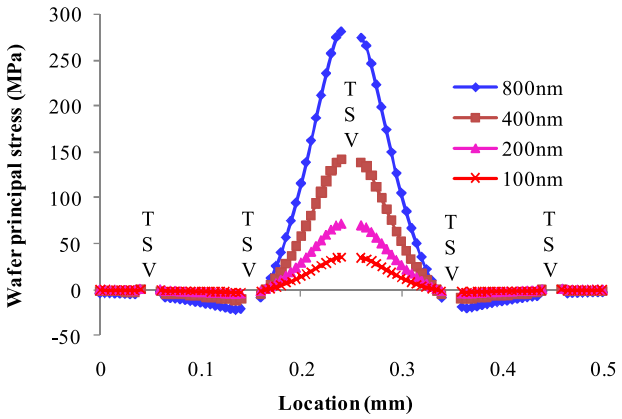

Fig. 11. Effect of surface roughness on TSV wafer stress.

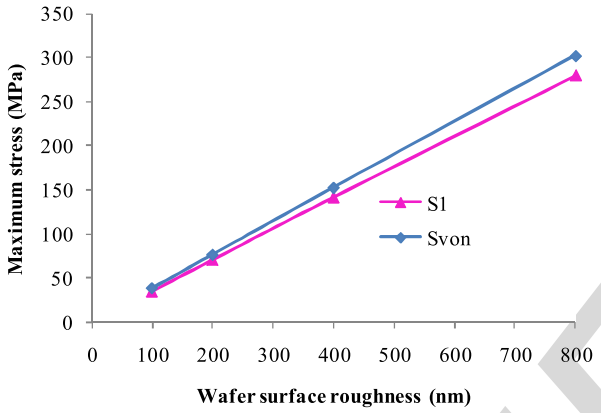

Fig. 12. Effect of surface roughness on the maximum stress.

Large roughness, which is usually related to a coarse grinding process and fast feeding rate, leads to high-wafer stress. Therefore, fine grinding and polishing process are needed for reducing wafer stress when the TSV wafer becomes thinner and thinner.

D. Effect of TSV Wafer Thickness

During the WTP, the TSV wafer was thinned from initial thickness of 750 μm to hundred micrometers by coarse grinding, and then was further thinned to the required thickness by fine grinding. The wafer thickness will affect the silicon stress, because the grinder gradually closes to the interface between the TSV wafer and bonding layer within the thinning process. In this paper, five different TSV wafer thicknesses were chosen to simulate the effect of TSV wafer thickness on silicon stress, including 150, 100, 75, 50, and 25 μm. Fig. 13 shows the effect of wafer thickness on the maximum principal stress with considering different surface roughness. It was shown that wafer stress increases with decreasing wafer thickness, which brings a challenge for WTP because the thinned wafer is prone to brittle failure due to large stress. For example, the wafer stress increases four times when the TSV wafer was thinned from 150 to 25 μm. Therefore, it is recommended to use the fine grinding process to reduce wafer stress when the TSV wafer was thinned down to 100 μm.

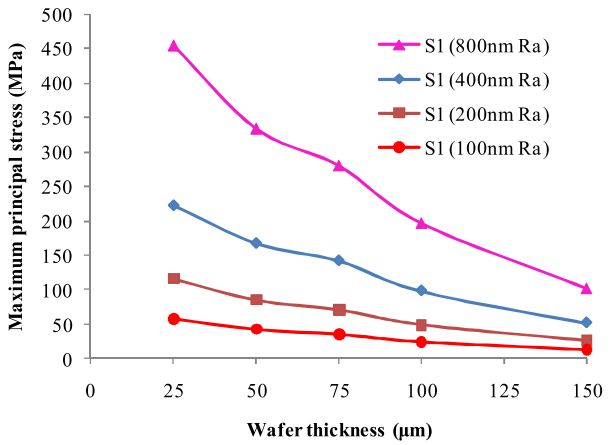

Fig. 13. Effect of wafer thickness on the maximum wafer stress.

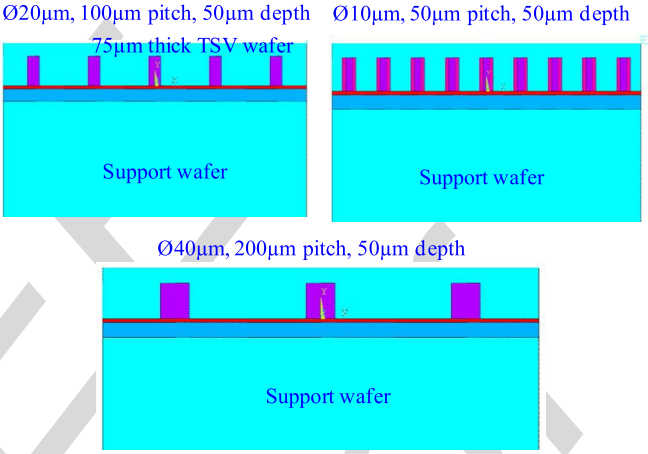

Fig. 14. FE models with different TSV diameters.

E. Effect of TSV Feature Size

The effect of via feature size on wafer stress was investigated. This includes TSV diameter, TSV depth, and TSV pitch. The reference FE model has a TSV wafer with 75-μm thickness, TSV with 20-μm diameter, 50-μm depth, and 100-μm pitch. In the modeling of TSV diameter effect, the same ratio of TSV pitch to TSV diameter was fixed as five for different TSV diameters, as shown in Fig. 14. The wafer stress increases slightly with decreasing TSV diameter, as shown in Fig. 15. For the TSV wafer with small TSV diameter, the TSV distribution is denser if the same ratio of TSV pitch to TSV diameter is applied, so that the effect of adjacent TSVs on each other is significant, which leads to high-wafer stress. This effect of TSV density on wafer stress under WTP is similar to that of TSV wafer subjected to thermal stress loading [4]. Therefore, careful treatment and handling are required for the TSV wafer with denser TSV design.

In the modeling of TSV depth effect, TSV wafers have the same thickness of 75 μm so that the TSV is not exposed for all cases. The TSV diameter and pitch are the same as that in the reference model. The TSV depth was chosen as 10, 20, 30, and 50 μm, as shown in Fig. 16. Fig. 17 shows the effect of TSV depth on the maximum first principal wafer stress.

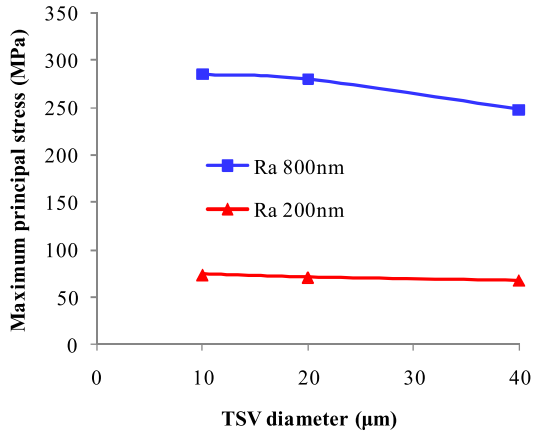

Fig. 15. Effect of TSV diameter on the maximum wafer stress.

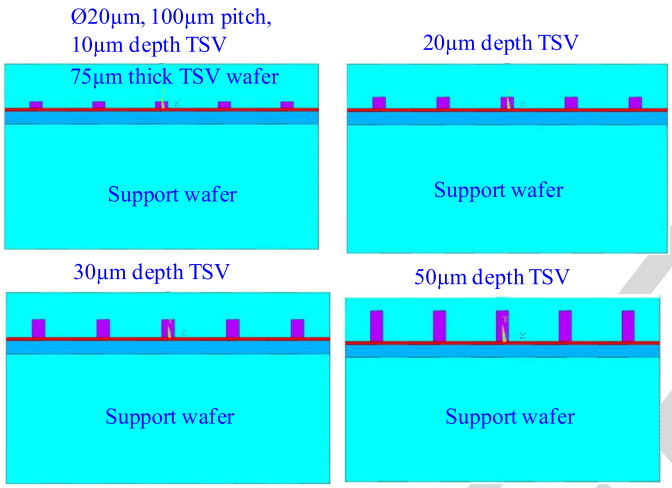

Fig. 16. FE models with different TSV depths.

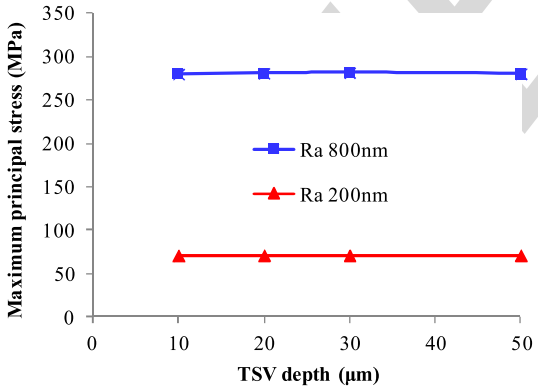

Fig. 17. Effect of TSV depth on the maximum wafer stress.

The effect of TSV depth on wafer stress can be ignored when TSVs are not exposed during WTP.

In the modeling of TSV pitch effect, TSV wafers have the same thickness of 75 μm and TSVs have the same diameter of 20 and depth of 50 μm. Different TSV pitches modeled include 50, 100, 200, and 400 μm. Fig. 18 shows the effect of TSV pitch on wafer stress. Wafer stress increases with decreasing TSV pitch, especially for the rough wafer.

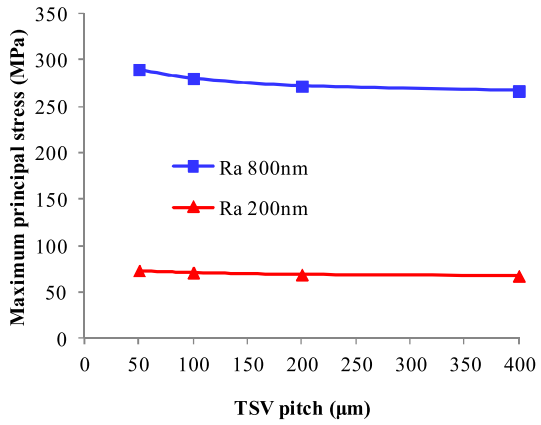

Fig. 18. Effect of TSV pitch on the maximum wafer stress.

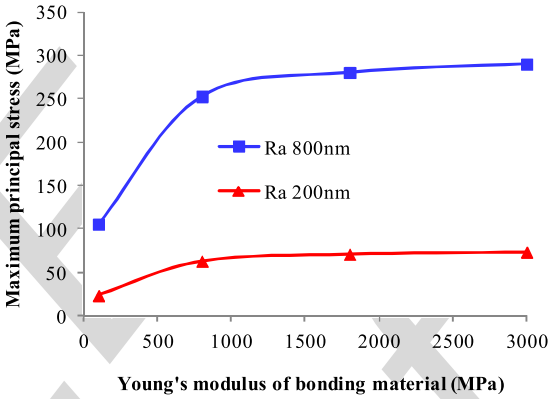

Fig. 19. Effect of Young's modulus of the bonding material on wafer stress.

The smaller TSV pitch results in higher TSV density, which leads to higher wafer stress due to the effect of the adjacent TSVs on each other. Considering results mentioned above for the effect of TSV diameter on wafer stress, a conclusion can be drawn that the denser the TSV design, the higher the wafer stress when subjected to the WTP.

F. Effect of Bonding Material and Bonding Layer Thickness

Before WTP, the TSV wafer should be attached onto a support wafer using bonding material. In this paper, the effects of bonding material and thickness on TSV wafer stress were investigated. The different elastic moduli of the bonding material were simulated, including 100, 800, 1800, and 3000 MPa. The bonding material layer thickness keeps a constant value of 20 μm, when investigating the effect of material properties on wafer stress. Fig. 19 shows the effect of Young's modulus of the bonding material on wafer stress. Wafer stress increases with increasing elastic modulus of bonding material. Lower elastic modulus indicates that the bonding layer is softer and this layer functions as a buffer layer, so that the wafer thinning-induced stress can be partially absorbed by this buffer layer. Especially for rougher wafer surface, this effect is significant. When the elastic modulus of bonding material increases to a certain level, e.g., 2000 MPa as shown in Fig. 19, TSV wafer stress becomes saturation. To reduce wafer stress during TSV WTP, the relatively soft bonding material

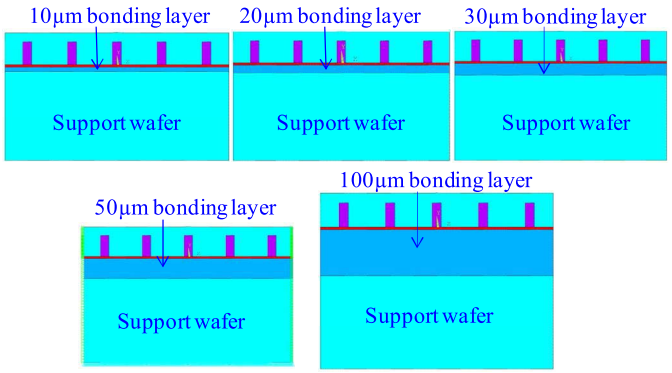

Fig. 20. FE models with different bonding layer thicknesses.

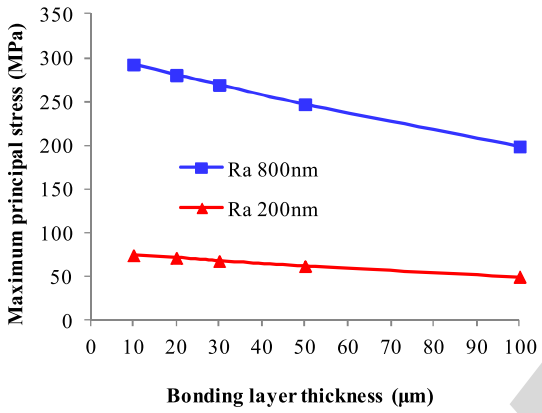

Fig. 21. Effect of bonding layer thickness on wafer stress.

is recommended. However, support function maybe degrades, if the bonding material is much softer. Therefore, it is a challenge to select temporally bonding/debonding material for the successful WTP and debonding process.

Fig. 20 shows the FE models with different bonding layer thicknesses of 10, 20, 30, 50, and 100 μm. The bonding material with elastic modulus of 1800 MPa was applied for bonding thickness study. Fig. 21 shows the effect of bonding thicknesses on wafer stress. Wafer stress decreases with increasing bonding layer thickness due to bonding layer functioning as a buffer layer. Using soft bonding material and relatively thick bonding layer can dramatically reduce TSV wafer stress during the WTP.

G. Effect of WTP on Mobility Change

It was found that the maximum stress usually occurs on the TSV wafer front surface (active side) when subjected to the WTP, as shown in Fig. 7. The devices closing to the wafer surface will subject large stress or stress variation, which makes the devices under potential failure or large mobility change [14], [15]. Therefore, it is necessary to investigate the effect of TSV WTP on the performance of the devices. The mechanical stress effect on the mobility change is expressed as follows:

$$\Delta\mu/\mu \approx |\pi_{\parallel}\sigma_{\parallel} + \pi_{\perp}\sigma_{\perp}| \quad (1)$$

TABLE IV
PIEZORESISTANCE COEFFICIENTS OF SILICON WAFER

(001) wafer [110] channel	Piezoresistance coefficients (Pa^{-1})	
Polarity	$\pi_{\parallel}$	$\pi_{\perp}$
n-MOSFET	-3.16×10^{-10}	-1.76×10^{-10}
p-MOSFET	-7.18×10^{-10}	-6.63×10^{-10}

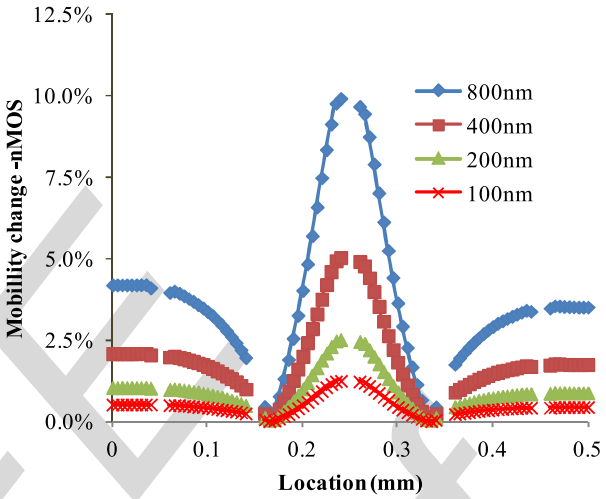

Fig. 22. Effect of thinning process-induced stress on mobility change of n-type wafer.

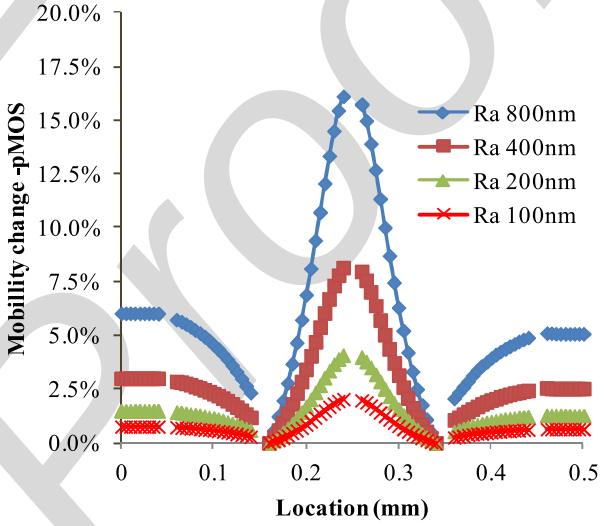

Fig. 23. Effect of thinning process-induced stress on mobility change of p-type wafer.

where $\Delta\mu/\mu$ is the fractional change in mobility, $\sigma_{\parallel}$ and $\sigma_{\perp}$ are the longitudinal and transverse stresses, and $\pi_{\parallel}$ and $\pi_{\perp}$ are the longitudinal and transverse piezoresistance coefficients (refer to Table IV) expressed in Pa^{-1}, respectively.

The longitudinal and transverse stresses around TSVs were obtained from the simulation results. Then, the mobility change can be calculated using (1). From (1) and Table IV,

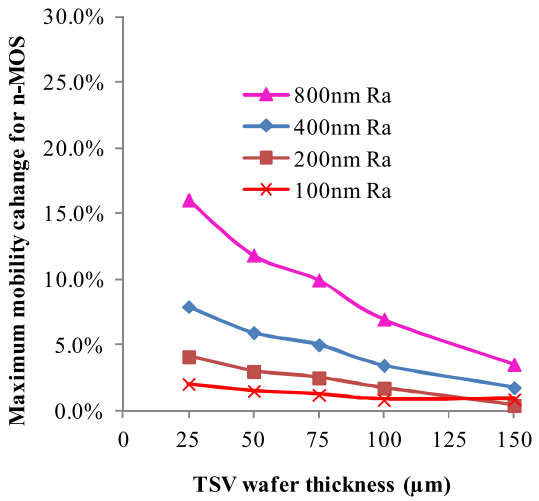

Fig. 24. Effect of TSV wafer roughness and thickness on the maximum mobility change of n-type wafer.

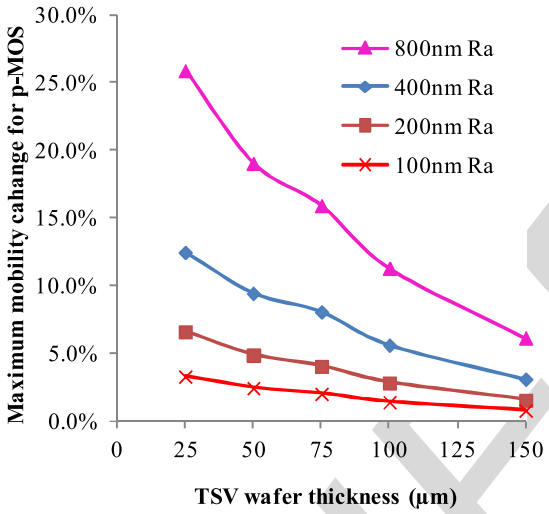

Fig. 25. Effect of TSV wafer roughness and thickness on the maximum mobility change of p-type wafer.

p-MOSFET and n-MOSFET show the different mobility changes, when they are subjected to the same stress condition due to different piezoresistance coefficients. Figs. 22 and 23 show the effect of thinning process-induced stress on mobility change for n-type and p-type wafers, respectively. The mobility change is larger for p-MOSFET than for n-MOSFET under the same stress condition. The maximum mobility change locates at the edge of the TSV with a rough bump defined above it. The mobility change increases with increasing wafer roughness. The maximum mobility change is more than 5% for the TSV wafer with large roughness. The stress and mobility change studies are necessary to define keep-away zone for devices to prevent devices from higher stress and performance degradation.

The maximum mobility change was also investigated when the TSV wafer was thinned down to different thicknesses, which can be used to mimic the dynamic thinning process impact on mobility change. Figs. 24 and 25 show the maximum mobility change for n-type and p-type wafers under different TSV WTPs, respectively. The mobility change increases with reducing wafer thickness and increasing WSR. Therefore, when the wafer thickness becomes thinner and thinner, it is essential to change coarse grinding process to fine grinding process for a thin wafer to reduce stresses and mobility change.

V. Conclusion

Wafer cracking is one common failure mode for TSV wafer under the WTP due to thinning-induced large stress. In this paper, a dynamic FEA modeling methodology for the WTP was developed and used for TSV wafer stress analysis under thinning process. It was justified that the 2-D model with modeling five TSVs is sufficient to do WTP simulation. Some conclusions can be drawn based on the simulation results and analyzes.

1) WSR is one of the critical parameters affecting TSV wafer stress under the WTP. Larger wafer roughness, which is usually related to faster feeding rate and coarser grinding process, leads to higher wafer stress.
2) Wafer stress increases with decreasing wafer thickness, which poses a challenge for WTP because the thinned wafer is prone to brittle failure due to large stress.
3) The denser the TSVs design, the higher the wafer stress during the TSV WTP. The effect of TSV depth on wafer stress is not significant when TSVs are not exposed.
4) Wafer stress decreases with increasing bonding thickness and decreasing bonding material modulus because bonding material functions as a buffer layer.
5) The mobility change is larger for p-MOSFET than for n-MOSFET under the same stress condition. Mobility change of devices increases with reducing wafer thickness and increase with increasing WSR.

Acknowledgment

This work is the result of core project related to TSV wafer thinning process (WTP) in IME. The authors would like to thank W. S. V. Lee for his support and discussion in the physical WTP.

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Dynamic Stress Modeling on Wafer Thinning Process and Reliability Analysis for TSV Wafer

Fa Xing Che

***Abstract*— Through-silicon-via (TSV) technology permits devices to be placed in the third dimension. Currently, there is a strong motivation for the semiconductor industry to move to 3-D integration using the TSV approach due to its many advantages. However, there are some challenges for TSV wafer processes. One of the challenges is TSV wafer thinning process (WTP). In this paper, a dynamic finite element modeling methodology was established and used to study the TSV WTP-induced wafer stress. It was found that wafer surface roughness, TSV wafer thickness, bonding/debonding material, and TSV feature size have impact on TSV wafer stress under the TSV WTP. The impact of wafer thinning-induced stress on mobility change was also discussed in this paper.**

***Index Terms*— Dynamic modeling, finite element analysis (FEA), reliability, through-silicon via (TSV), wafer thinning.**

I. Introduction

IN A 3-D chip, multiple device layers are stacked together with direct vertical interconnects. Therefore, one of the most important benefits of a 3-D chip over a traditional 2-D design is the reduction on global interconnect. There are various vertical interconnect technologies, including wire bonding, microbump, Cu pillar, and through-via vertical interconnect [1]. The 3-D integration using the through-silicon-via (TSV) approach becomes one promising technology in 3-D packaging due to many advantages [2], such as higher clock rates, lower power dissipation, and higher integration density. However, there are several challenges associated with TSV fabrication and TSV wafer processes. Most of the challenges are process-related, such as reducing Cu overburden with achieving void-free filled Cu TSV [3], Cu protrusion [4], wafer warpage control [5], wafer thinning process (WTP), bonding/debonding process [6], thermal-induced reliability issues [7]–[9], and so on. This paper focuses on the TSV WTP-induced reliability problems.

In this paper, a dynamic finite element analysis (FEA) modeling methodology has been developed for WTP for the first time to study the wafer thinning-induced stress and its effect on TSV wafer reliability. It was found that the wafer surface roughness (WSR) is one of the very important parameters affecting silicon (Si) wafer stress-induced by WTP. From a physical WTP, typical roughness value (Ra) is several hundred nanometers for rough grinding, 20–50 nm for fine grinding. The FEA simulation results showed that large roughness, which usually is related to fast feeding rate and coarse grinding process, leads to high-wafer stress. Wafer thickness is another important parameter affecting TSV wafer stress. Simulation results showed that wafer stress increases with decreasing wafer thickness, which brings a challenge for WTP, because a thinned TSV wafer is prone to brittle failure due to large stress. In this paper, the effect of bonding material and thickness on TSV wafer stress were also modeled. The effects of TSV design, such as via diameter, depth, and pitch, on wafer stress were investigated. Simulation results can be used to understand wafer thinning-induced reliability issues and to optimize the TSV WTP to reduce wafer stress.

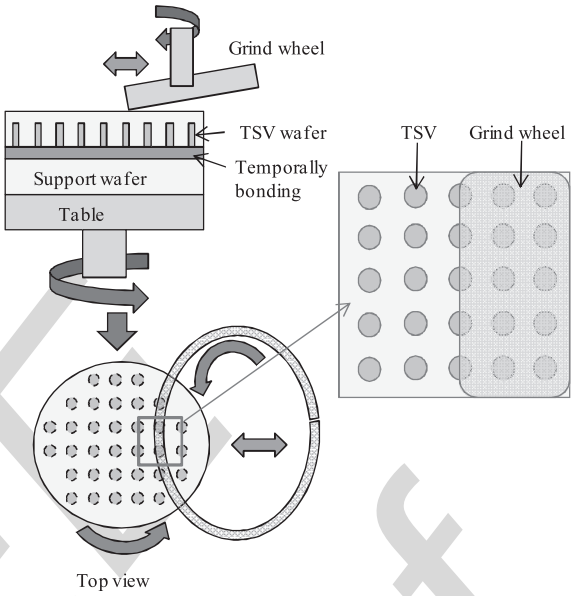

Fig. 1. Schematic diagram of the TSV WTP.

II. Experimental Procedures

The TSV fabrication was done on the eight inch Si wafer with an initial thickness of 750 μm. After that, the TSV wafer was thinned down to the desired thickness, such as 50 or 100 μm, and then the TSV backside was revealed for the subsequent redistribution layer process and interconnection. Fig. 1 shows a schematic view of TSV WTP. The TSV wafer was mounted onto the support wafer using the temporally bonding/debonding process. The support wafer

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TABLE I
PARAMETERS USED IN THE WTP

Parameters	Rough Grind	Fine Grind
Spindle Speed	2500 rpm	3200 rpm
Chuck Speed	150 rpm	150 rpm
Feed Speed 1	150 μm/min	40 μm/min
Feed Speed 2	80 μm/min	20 μm/min
Air Cut	50 μm	50 μm
Removal amount	20 μm to 650 μm	20 μm to 50 μm
Coolant	DI water and Air	DI water and Air

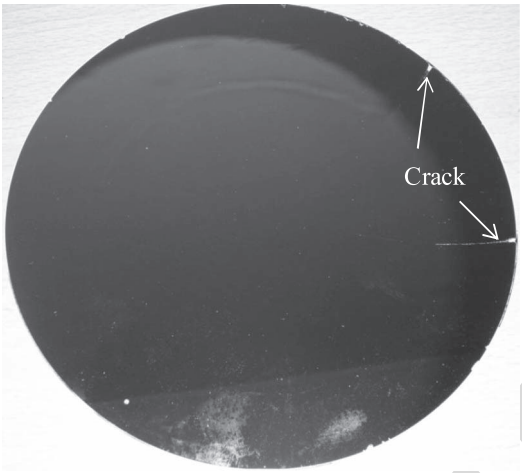

Fig. 2. Wafer cracking due to thinning process.

was then mounted onto the table of the thinning machine. Grinding angle of 20° was used during the thinning process. Table I lists the typical parameters used in the WTP. In the thinning process, coarse grinding was carried out first using a rough grind wheel with mesh sizes of #320 until the TSV wafer thickness reached <150 μm. Then, fine grinding was carried out using a fine grind wheel with mesh sizes of #2000. After fine grinding to 50 μm, stress relief by removing 2-μm silicon through the chemical mechanical polishing (CMP) process was further carried out to smooth the wafer surface. Typical Ra is several hundred nanometers after rough grinding, 20–50 nm after fine grinding and 10 nm or less after the CMP process.

The common defects under the thinning process include edge chipping and wafer cracking, as shown in Fig. 2. For TSV WTP, wafer cracking is along the TSV edges and then the cracks pass through the adjacent TSVs, as shown in Fig. 3. The Cu TSVs have different material properties from the Si die and the vias can be regarded as inclusions embedded in the Si matrix. Extensive studies have shown that inclusions disturb the stress field and can cause stress concentration in their neighborhoods [10], [11]. The evaluation of reliability under TSV WTP is essential to optimize the TSV thinning process. The FEA modeling is one of the desirable tools for optimization studies, which was used in this paper for WTP simulation.

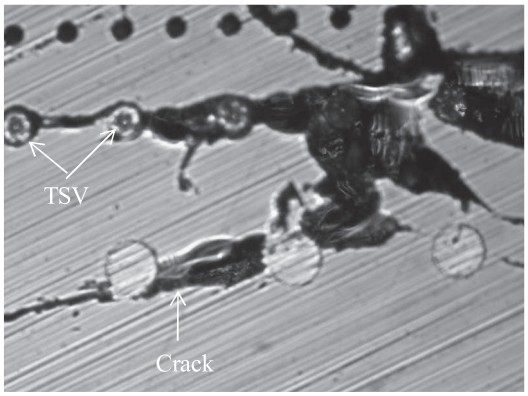

Fig. 3. Cracks along TSVs-induced by WTP.

III. FEA APPROACH

In this paper, a dynamic FEA modeling methodology was developed for the WTP using the ANSYS/LS-DYNA commercial software. To simulate the WTP-induced stresses around TSVs, a dynamic modeling method was established to simulate the effect of surface roughness of the TSV wafer. Different surface roughness represents different grinding processes. Fig. 4 shows a basic 2-D plane strain FE model including one TSV. The WSR effect was modeled by surface bumps with an equivalent height as Ra. The worst case of TSV just located under the bump was simulated. In the FE model, a 700-μm-thick support Si wafer was simulated. A thinned TSV wafer is attached on the support wafer through a bonding material layer of 20-μm thickness. The Cu TSVs are surrounded by Si material. The TSV has a feature size of 20 μm in diameter, 50 μm in depth, and 100 μm in pitch. It can be observed from Fig. 1 that several TSVs were covered by grind head simultaneously. The effect of adjacent TSVs each other should be considered in the FE modeling. Therefore, the simulated stress convergence study was carried out by modeling the different number of TSVs in FE model, as shown in Fig. 5.

Boundary condition was carefully defined in the 2-D plane strain model. The bottom of the support wafer was fixed in all directions. Nodes on the two vertical edges were coupled with displacement in the horizontal direction. The top surface of TSV wafer is free. Grinder was modeled as a rigid body. The maximum relative speed of grinder and wafer occurs at the edge of the TSV wafer. The calculated speed based on thinning parameters was applied onto a grinder as an input constant velocity. Surface-to-surface contact pair between the grinder and wafer surface was defined. The friction effect between grinder and TSV wafer surface was modeled. When the high-speed grinder impacts on the simulated bump on the TSV wafer surface, this impact load introduces dynamic stress in the TSV wafer.

To justify 2-D model is sufficient for WTP simulation, 3-D model was also built for comparison. Fig. 6 shows 3-D FE models including one TSV model and 5 × 5 array TSVs model. Similar with the 2-D model, boundary condition was defined in the 3-D model with the bottom of the support

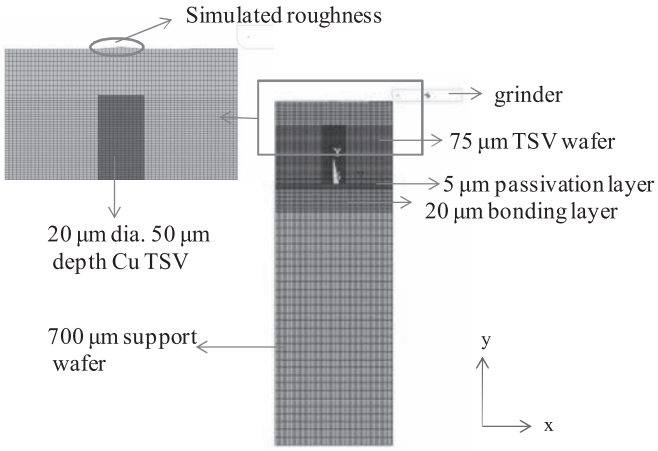

Fig. 4. 2-D FE model with one TSV unit.

TABLE II
MATERIAL PROPERTIES USED IN THE FE MODEL

Materials	Young's modulus (GPa)	Poisson's ratio	Density (kg/m^3)
Silicon	131	0.28	2330
Copper	117	0.35	8960
Dielectric	1.3	0.3	2000
Bonding	1.79	0.35	1500

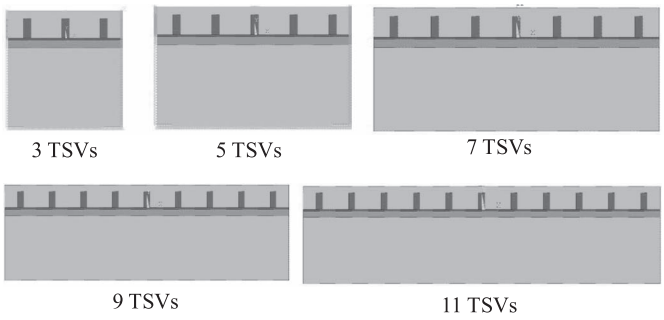

Fig. 5. 2-D FE models with different number of TSVs.

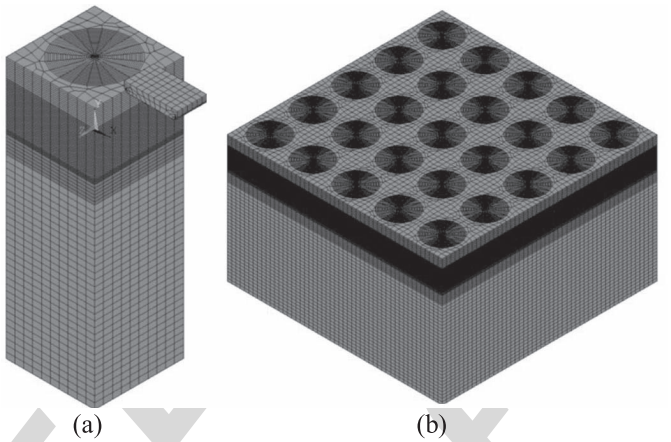

Fig. 6. 3-D FE models. (a) Model with one TSV. (b) Model with 5×5 array TSVs.

wafer was fixed and nodes on the four side walls were coupled accordingly. The other parameters in the 3-D model, such as friction, contact pair, and loading condition, were the same as the 2-D model.

During WTP, the heat generated is caused by the friction between the grinding wheel and the wafer surface. Moulik *et al.* [12] developed a model using a heat source and pressure as inputs to study temperature distribution and thermal residual stresses in grinding process. The results showed that temperature is much localized and the surface residual stresses are tensile [12]. The coolant was commonly used in the WTP to prevent tooling damage, remove particle, and importantly remove heat generated by grinding process. Abdelnaby *et al.* [13] simulated the heat generation during silicon wafer back grinding process. It was found that the temperature of the wafer decreases rapidly to the ambient temperature of 23 °C and the coolant temperature does not change during the thinning process [13]. Materials used in the microelectronics usually show the temperature-dependent properties, which affect the stress value when subjected to thermal loading. However, the wafer temperature is similar to the ambient temperature during the WTP due to the coolant application. Therefore, temperature-independent properties were used for all materials. Table II lists the materials and their mechanical properties used in the FE modeling. The Cu TSV was modeled with a bilinear kinematic hardening plastic behavior. Other materials, Si, dielectric, and bonding material, were modeled with only elastic behavior.

IV. RESULTS AND DISCUSSION

A. Effect of the Number of the Modeled TSVs in 2-D Model

The FE model with 800-nm Ra and 75-μm TSV wafer thickness were simulated. Fig. 7 shows the simulation results of first principle stress for the 2-D FE model with five TSVs. The stress concentrates around TSV at the area of the interface between the TSV wafer and bonding material layer. Such high-stress concentration could damage the wafer or devices. Fig. 8 shows the effect of the number of modeled TSVs in one 2-D FE model (refer to Fig. 5) on wafer stress. Modeling one TSV in the 2-D FE model is not enough, because the effect of adjacent TSV is not considered. The maximum TSV wafer stress increases with increasing the number of TSVs included in one 2-D FE model. The maximum stresses of both principal stress (S1) and von Mises stress (Svon) are converged and stable, when modeling five or more TSVs in one 2-D FE model.

B. Comparison Between 2-D and 3-D Models

Fig. 9 shows the comparison of the maximum TSV wafer stresses between 2-D and 3-D models. For FE model with one TSV, both 2-D and 3-D models result in the similar maximum principal stress and the 2-D model leads to slightly larger Svon than the 3-D model. For FE model with five TSVs for 2-D model and with 5×5 array TSVs for 3-D model, both 2-D and 3-D models result in the similar maximum

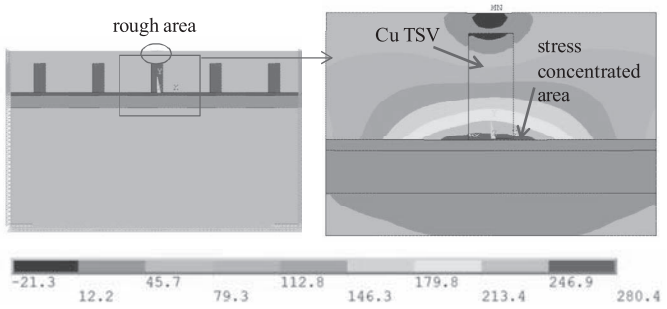

Fig. 7. Stress contour of first principal stress.

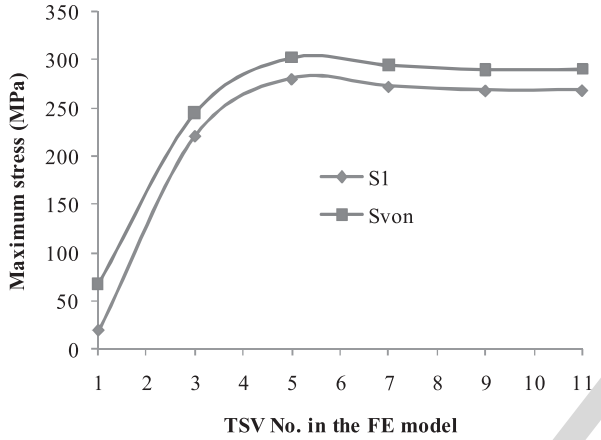

Fig. 8. Effect of the number of modeled TSVs on wafer stress.

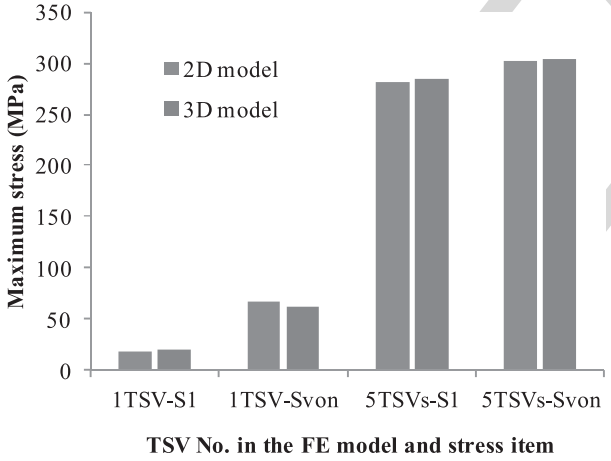

Fig. 9. Comparison of the maximum TSV wafer stresses between 2-D and 3-D models.

principal stress and Svon. When modeling five TSVs for 2-D model and 5 × 5 array TSVs for 3-D model, the TSV wafer stress distribution along the cutting path through five TSVs is almost the same for 2-D and 3-D models, as shown in Fig. 10. Table III lists the relative comparison of computing resources between 2-D and 3-D models by considering 2-D model with one TSV as a reference. It can be seen that computing resources, especially for solving time, increase significantly for 3-D model with more TSVs, which is not realistic to use 3-D model to do parametric study. Based on

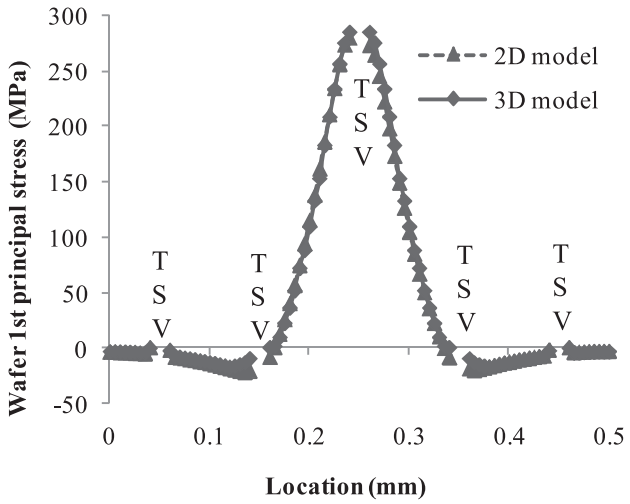

Fig. 10. Comparison of first principal stress along the cutting path through five TSVs between 2-D and 3-D models.

TABLE III
RELATIVE COMPARISON OF COMPUTING RESOURCES BETWEEN 2-D AND 3-D MODELS

FE model	Model size	Solving time	Result file size
2D-1TSV	1	1	1
2D-5TSVs	5	7	13
3D-1TSV	10	15	20
3D-5x5TSVs	250	2000	1100

stress comparison between 2-D and 3-D models and the effect of modeled TSV on the simulated stresses discussed in Section IV-A, the 2-D FE model with five TSVs was sufficient for the TSV WTP simulation due to accurate simulation results and acceptable model size, and short solving time. The 2-D FE model with five TSVs was implemented in the subsequent parametric studies.

C. Effect of TSV WSR

From a physical WTP, typical Ra is several hundred nanometers after rough grinding, and 20–50 nm after fine grinding. In this paper, four different Ras of 800, 400, 200, and 100 nm were simulated to investigate the effect of roughness on TSV wafer stress under WTP. The used FE model consists of five TSVs with 20-μm via diameter, 50-μm depth, 100-μm pitch, 75-μm TSV wafer thickness, and 20-μm bonding thickness. Fig. 11 shows the effect of TSV WSR on wafer stress (first principal stress) along the interface between the TSV wafer and bonding layer. The maximum stress occurs at the edge of TSV with surface roughness setting (bump with an equivalent thickness) above it. It was found that the WSR is one of the critical parameters affecting silicon stress under the WTP. Fig. 12 shows the relationship between the maximum stress and TSV WSR. The principal stress and Svon have the similar value and trend with changing surface roughness. Stress increases significantly with increasing TSV WSR.

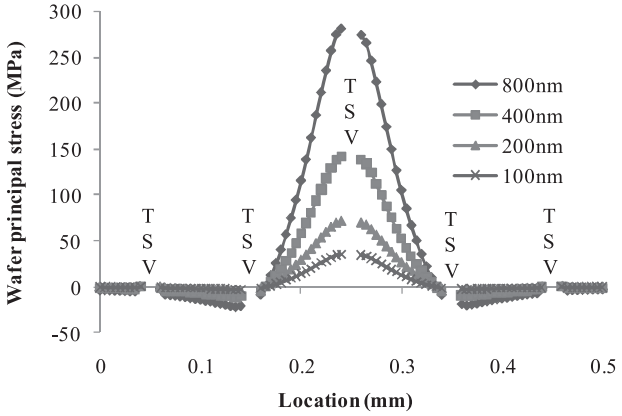

Fig. 11. Effect of surface roughness on TSV wafer stress.

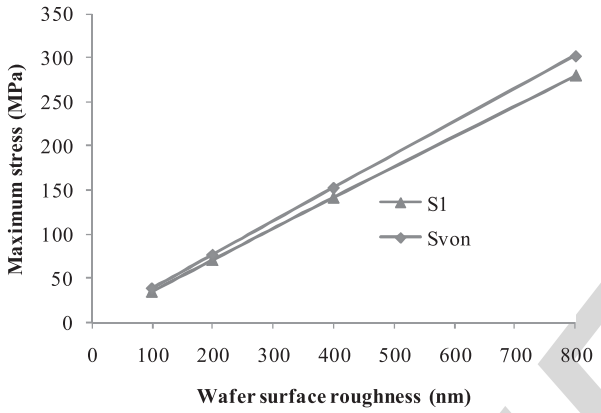

Fig. 12. Effect of surface roughness on the maximum stress.

Large roughness, which is usually related to a coarse grinding process and fast feeding rate, leads to high-wafer stress. Therefore, fine grinding and polishing process are needed for reducing wafer stress when the TSV wafer becomes thinner and thinner.

D. Effect of TSV Wafer Thickness

During the WTP, the TSV wafer was thinned from initial thickness of 750 μm to hundred micrometers by coarse grinding, and then was further thinned to the required thickness by fine grinding. The wafer thickness will affect the silicon stress, because the grinder gradually closes to the interface between the TSV wafer and bonding layer within the thinning process. In this paper, five different TSV wafer thicknesses were chosen to simulate the effect of TSV wafer thickness on silicon stress, including 150, 100, 75, 50, and 25 μm. Fig. 13 shows the effect of wafer thickness on the maximum principal stress with considering different surface roughness. It was shown that wafer stress increases with decreasing wafer thickness, which brings a challenge for WTP because the thinned wafer is prone to brittle failure due to large stress. For example, the wafer stress increases four times when the TSV wafer was thinned from 150 to 25 μm. Therefore, it is recommended to use the fine grinding process to reduce wafer stress when the TSV wafer was thinned down to 100 μm.

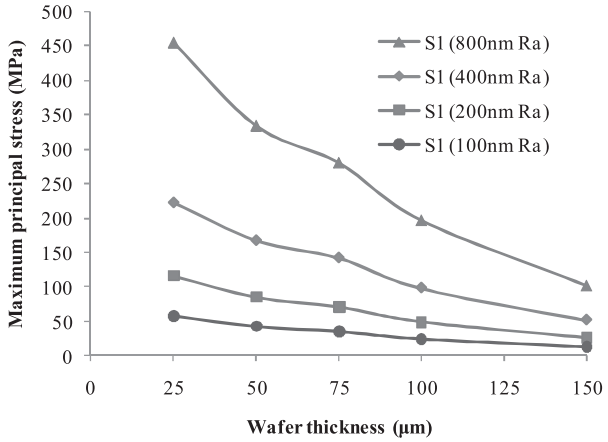

Fig. 13. Effect of wafer thickness on the maximum wafer stress.

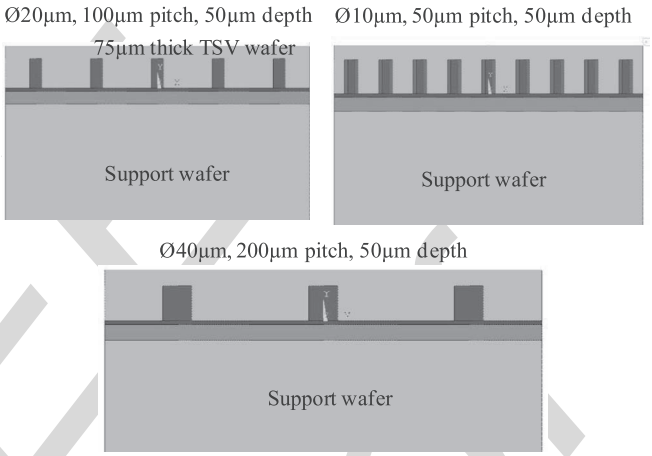

Fig. 14. FE models with different TSV diameters.

E. Effect of TSV Feature Size

The effect of via feature size on wafer stress was investigated. This includes TSV diameter, TSV depth, and TSV pitch. The reference FE model has a TSV wafer with 75-μm thickness, TSV with 20-μm diameter, 50-μm depth, and 100-μm pitch. In the modeling of TSV diameter effect, the same ratio of TSV pitch to TSV diameter was fixed as five for different TSV diameters, as shown in Fig. 14. The wafer stress increases slightly with decreasing TSV diameter, as shown in Fig. 15. For the TSV wafer with small TSV diameter, the TSV distribution is denser if the same ratio of TSV pitch to TSV diameter is applied, so that the effect of adjacent TSVs on each other is significant, which leads to high-wafer stress. This effect of TSV density on wafer stress under WTP is similar to that of TSV wafer subjected to thermal stress loading [4]. Therefore, careful treatment and handling are required for the TSV wafer with denser TSV design.

In the modeling of TSV depth effect, TSV wafers have the same thickness of 75 μm so that the TSV is not exposed for all cases. The TSV diameter and pitch are the same as that in the reference model. The TSV depth was chosen as 10, 20, 30, and 50 μm, as shown in Fig. 16. Fig. 17 shows the effect of TSV depth on the maximum first principal wafer stress.

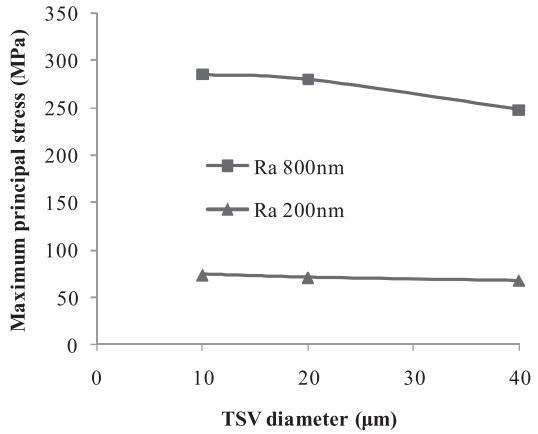

Fig. 15. Effect of TSV diameter on the maximum wafer stress.

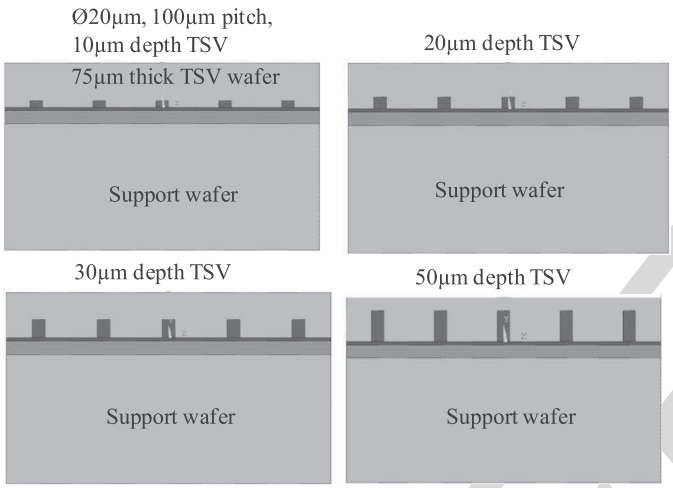

Fig. 16. FE models with different TSV depths.

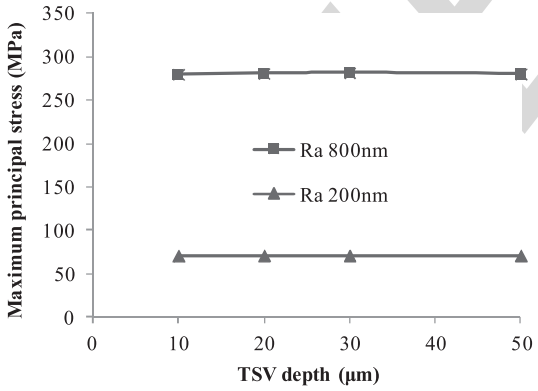

Fig. 17. Effect of TSV depth on the maximum wafer stress.

The effect of TSV depth on wafer stress can be ignored when TSVs are not exposed during WTP.

In the modeling of TSV pitch effect, TSV wafers have the same thickness of 75 μm and TSVs have the same diameter of 20 and depth of 50 μm. Different TSV pitches modeled include 50, 100, 200, and 400 μm. Fig. 18 shows the effect of TSV pitch on wafer stress. Wafer stress increases with decreasing TSV pitch, especially for the rough wafer.

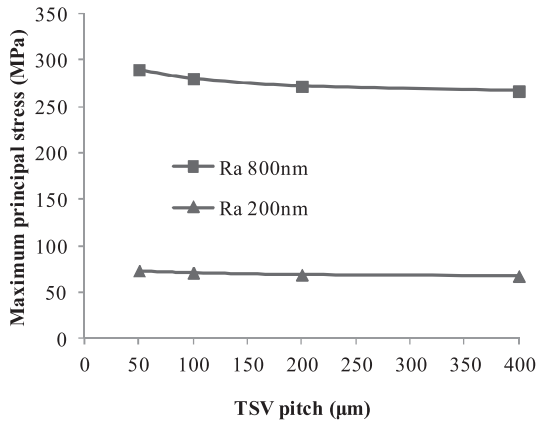

Fig. 18. Effect of TSV pitch on the maximum wafer stress.

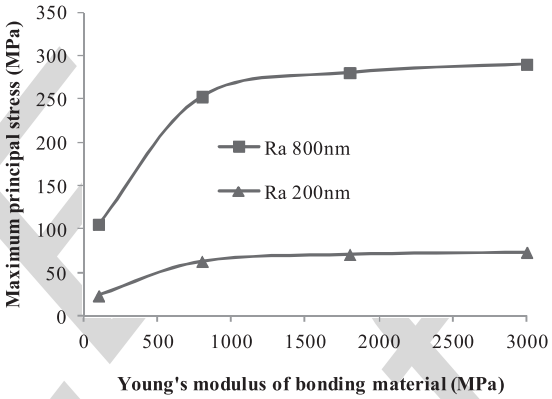

Fig. 19. Effect of Young's modulus of the bonding material on wafer stress.

The smaller TSV pitch results in higher TSV density, which leads to higher wafer stress due to the effect of the adjacent TSVs on each other. Considering results mentioned above for the effect of TSV diameter on wafer stress, a conclusion can be drawn that the denser the TSV design, the higher the wafer stress when subjected to the WTP.

F. Effect of Bonding Material and Bonding Layer Thickness

Before WTP, the TSV wafer should be attached onto a support wafer using bonding material. In this paper, the effects of bonding material and thickness on TSV wafer stress were investigated. The different elastic moduli of the bonding material were simulated, including 100, 800, 1800, and 3000 MPa. The bonding material layer thickness keeps a constant value of 20 μm, when investigating the effect of material properties on wafer stress. Fig. 19 shows the effect of Young's modulus of the bonding material on wafer stress. Wafer stress increases with increasing elastic modulus of bonding material. Lower elastic modulus indicates that the bonding layer is softer and this layer functions as a buffer layer, so that the wafer thinning-induced stress can be partially absorbed by this buffer layer. Especially for rougher wafer surface, this effect is significant. When the elastic modulus of bonding material increases to a certain level, e.g., 2000 MPa as shown in Fig. 19, TSV wafer stress becomes saturation. To reduce wafer stress during TSV WTP, the relatively soft bonding material

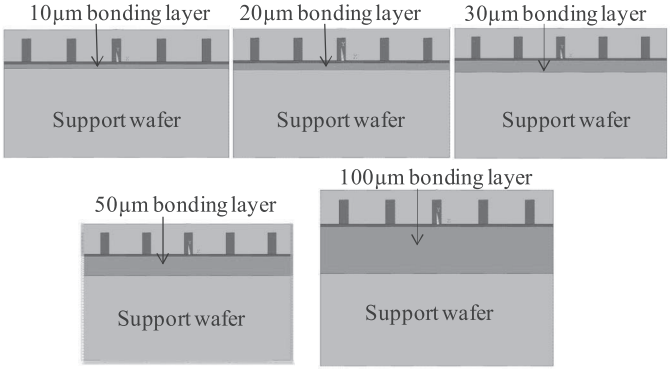

Fig. 20. FE models with different bonding layer thicknesses.

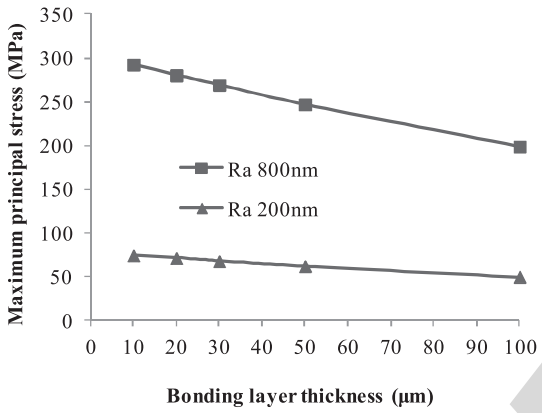

Fig. 21. Effect of bonding layer thickness on wafer stress.

is recommended. However, support function maybe degrades, if the bonding material is much softer. Therefore, it is a challenge to select temporally bonding/debonding material for the successful WTP and debonding process.

Fig. 20 shows the FE models with different bonding layer thicknesses of 10, 20, 30, 50, and 100 μm. The bonding material with elastic modulus of 1800 MPa was applied for bonding thickness study. Fig. 21 shows the effect of bonding thicknesses on wafer stress. Wafer stress decreases with increasing bonding layer thickness due to bonding layer functioning as a buffer layer. Using soft bonding material and relatively thick bonding layer can dramatically reduce TSV wafer stress during the WTP.

G. Effect of WTP on Mobility Change

It was found that the maximum stress usually occurs on the TSV wafer front surface (active side) when subjected to the WTP, as shown in Fig. 7. The devices closing to the wafer surface will subject large stress or stress variation, which makes the devices under potential failure or large mobility change [14], [15]. Therefore, it is necessary to investigate the effect of TSV WTP on the performance of the devices. The mechanical stress effect on the mobility change is expressed as follows:

$$\Delta\mu/\mu \approx |\pi_{\parallel}\sigma_{\parallel} + \pi_{\perp}\sigma_{\perp}| \quad (1)$$

TABLE IV
PIEZORESISTANCE COEFFICIENTS OF SILICON WAFER

(001) wafer [110] channel	Piezoresistance coefficients (Pa^{-1})	
Polarity	$\pi_{\parallel}$	$\pi_{\perp}$
n-MOSFET	-3.16×10^{-10}	-1.76×10^{-10}
p-MOSFET	-7.18×10^{-10}	-6.63×10^{-10}

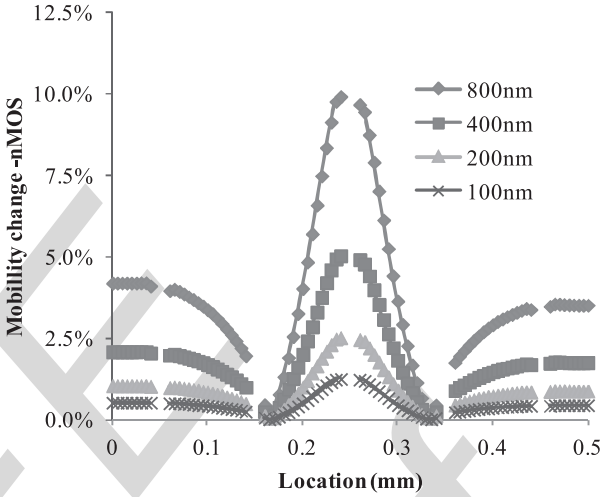

Fig. 22. Effect of thinning process-induced stress on mobility change of n-type wafer.

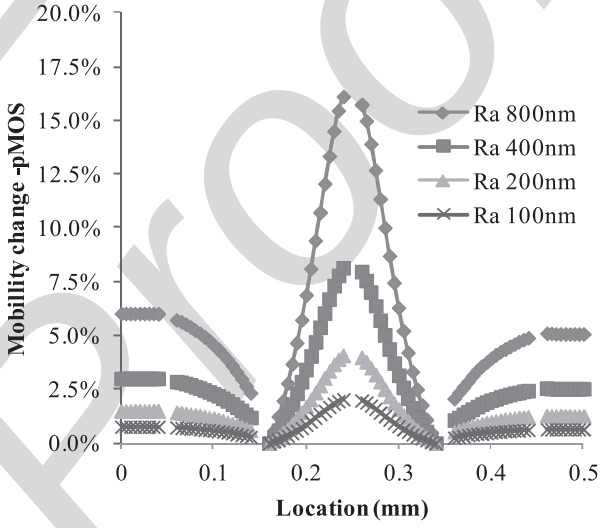

Fig. 23. Effect of thinning process-induced stress on mobility change of p-type wafer.

where $\Delta\mu/\mu$ is the fractional change in mobility, $\sigma_{\parallel}$ and $\sigma_{\perp}$ are the longitudinal and transverse stresses, and $\pi_{\parallel}$ and $\pi_{\perp}$ are the longitudinal and transverse piezoresistance coefficients (refer to Table IV) expressed in Pa^{-1}, respectively.

The longitudinal and transverse stresses around TSVs were obtained from the simulation results. Then, the mobility change can be calculated using (1). From (1) and Table IV,

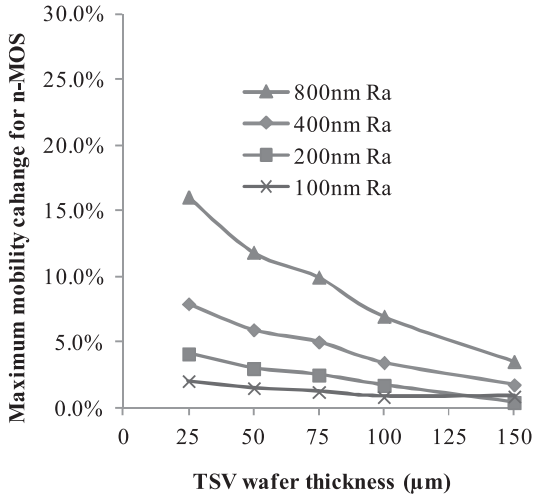

Fig. 24. Effect of TSV wafer roughness and thickness on the maximum mobility change of n-type wafer.

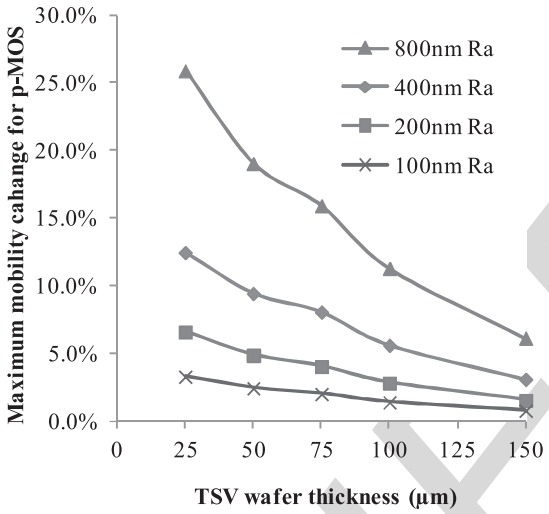

Fig. 25. Effect of TSV wafer roughness and thickness on the maximum mobility change of p-type wafer.

p-MOSFET and n-MOSFET show the different mobility changes, when they are subjected to the same stress condition due to different piezoresistance coefficients. Figs. 22 and 23 show the effect of thinning process-induced stress on mobility change for n-type and p-type wafers, respectively. The mobility change is larger for p-MOSFET than for n-MOSFET under the same stress condition. The maximum mobility change locates at the edge of the TSV with a rough bump defined above it. The mobility change increases with increasing wafer roughness. The maximum mobility change is more than 5% for the TSV wafer with large roughness. The stress and mobility change studies are necessary to define keep-away zone for devices to prevent devices from higher stress and performance degradation.

The maximum mobility change was also investigated when the TSV wafer was thinned down to different thicknesses, which can be used to mimic the dynamic thinning process impact on mobility change. Figs. 24 and 25 show the maximum mobility change for n-type and p-type wafers under different TSV WTPs, respectively. The mobility change increases with reducing wafer thickness and increasing WSR. Therefore, when the wafer thickness becomes thinner and thinner, it is essential to change coarse grinding process to fine grinding process for a thin wafer to reduce stresses and mobility change.

V. Conclusion

Wafer cracking is one common failure mode for TSV wafer under the WTP due to thinning-induced large stress. In this paper, a dynamic FEA modeling methodology for the WTP was developed and used for TSV wafer stress analysis under thinning process. It was justified that the 2-D model with modeling five TSVs is sufficient to do WTP simulation. Some conclusions can be drawn based on the simulation results and analyzes.

1) WSR is one of the critical parameters affecting TSV wafer stress under the WTP. Larger wafer roughness, which is usually related to faster feeding rate and coarser grinding process, leads to higher wafer stress.
2) Wafer stress increases with decreasing wafer thickness, which poses a challenge for WTP because the thinned wafer is prone to brittle failure due to large stress.
3) The denser the TSVs design, the higher the wafer stress during the TSV WTP. The effect of TSV depth on wafer stress is not significant when TSVs are not exposed.
4) Wafer stress decreases with increasing bonding thickness and decreasing bonding material modulus because bonding material functions as a buffer layer.
5) The mobility change is larger for p-MOSFET than for n-MOSFET under the same stress condition. Mobility change of devices increases with reducing wafer thickness and increase with increasing WSR.

Acknowledgment

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