A Battery-input Hysteretic Buck Converter with 430nA Quiescent Current and 5×10^4 Load Current Dynamic Range for Wearable Biomedical Devices

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***Abstract*—This paper presents a battery-input hysteretic buck converter with 430nA quiescent current for wearable biomedical devices. The converter input range is 2.5–4.2 V for rechargeable Li-ion battery and the output is fixed at 1.2 V. To reduce the quiescent power consumption and enhance the power efficiency at light load condition, the PFM controlled buck converter employs a hysteretic comparator with dynamic biasing circuit to reduce the current consumption during idle state. A delay compensation circuit is optimized for the comparator in zero current detector (ZCD) to maximize the overall power efficiency. This converter is implemented in a standard 55nm CMOS BCDLITE process with active circuit area of 0.8mm×0.8mm. Postlayout simulations show the circuit can achieve 5×10^4 load current dynamic range in 2 µA– 100 mA, and higher than 85% efficiency is maintained between 10 µA and 100mA with a peak efficiency of 88.6%.**

Keywords— DC-DC converter, buck converter, low quiescent, hysteretic control, discontinuous conduction mode (DCM)

I. INTRODUCTION

Wearable devices are playing a prominent role in modern healthcare system, especially in an ageing society [1]. By sensing the body potential signals such as electrocardiogram (ECG), electroencephalography (EEG), electromyography (EMG), etc., comprehensive physical condition of the human body can be monitored [2]. Multiple applications such as vital sign monitoring, remote rehabilitation supervision can be realized [3, 4], which facilitate the diagnosis and treatment of diseases at an earlier stage. Due to these uniques advantages, there are increasing demands for miniaturized, easy-to-wear Internet of Thing (IoT) biomedical sensors.

Voltage regulators such as low-dropout regulators [5, 6], buck converters [8, 9, 13,14] or buck-boost converters [7] are essential power management unit in a battery powered system. Li-ion rechargeable battery is a widely used power source for IoT sensor because of its high energy density and low cost. It has an output voltage in the range of 4.2 V to 2.5 V, depending on the battery charging condition [8]. On the other hand, with the process scaling of modern submicron CMOS technology, the integrated circuit supply voltage is reduced to 1.2 V or below. Therefore, to achieve a prolonged battery life, a high efficiency DC-DC converter is required to down convert the variable battery output voltage to a stable supply for wearable IoT device. Moreover, since most of the time the IoT sensors operate in sleep mode, the load current for the DC-DC converter can be reduced to microampere level. In such light load scenarios, quiescent power loss becomes dominant and many existing power management circuits [9, 17, 18] have poor power efficiencies. When the sensor is activated for data transmission, the load current of DC-DC converter can increase to tens of milliampere, depending on the communication protocol. Therefore, the buck converter must be able to handle a wide range of load current with high conversion efficiency.

This work was supported by the Agency for Science, Technology and research (A*STAR), Singapore under the Nanosystems at the Edge programme, grant no.A18A1b0055.

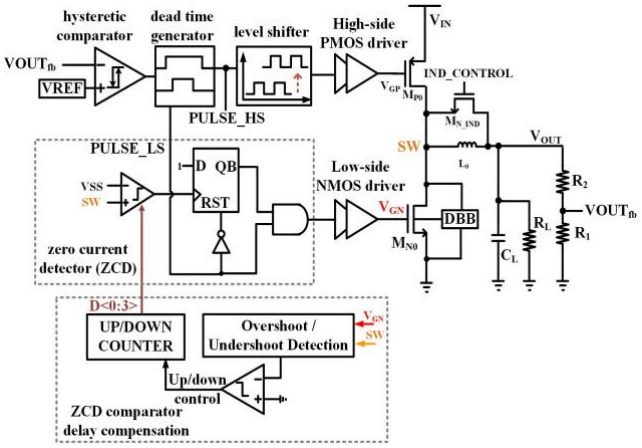

Fig. 1. Top-level architecture of the proposed hysteretic buck converter with PFM controller.

In this paper, we present a battery-input buck converter operating in discontinuous conduction mode (DCM), with a pulse frequency modulation (PFM) controller to down convert the battery voltage. The design is implemented in a standard 55nm BCDLITE process and achieves an 88.6 % peak efficiency with a 430nA quiescent current. The rest of this paper is arranged as follow. Section II presents the top-level architecture of the proposed buck converter and the hysteretic control. Section III describes the circuit implementation of key controller blocks. Post-layout simulation results are then presented in Section IV and Section V provides the conclusion.

II. ARCHITECTURE

Fig. 1 shows the overall buck converter architecture which consists of the power switches, gate drivers, external inductor and resistive feedback network and the controller circuitry, including a hysteretic comparator, dead time generator, capacitively cross couple level shifter and the zero current detector with a control loop to compensate for the ZCD comparator propagation delay and further reduce the power loss caused by the reverse current conduction.

The voltage-mode hysteretic control [9, 10] for buck converters relies on a hysteretic comparator to turn on PMOS

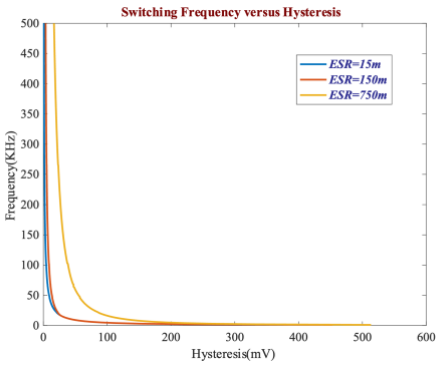

Fig. 2. Relationship between switching frequency and hysteresis at different ESR.

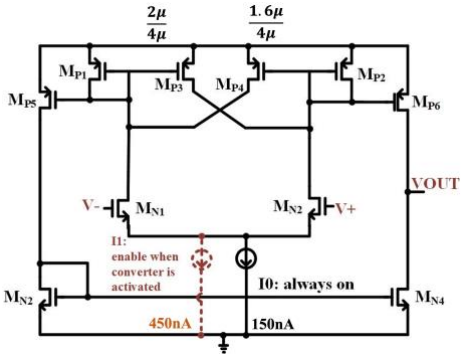

Fig. 3. Cross-coupled hysteretic comparator with dynamic biasing current.

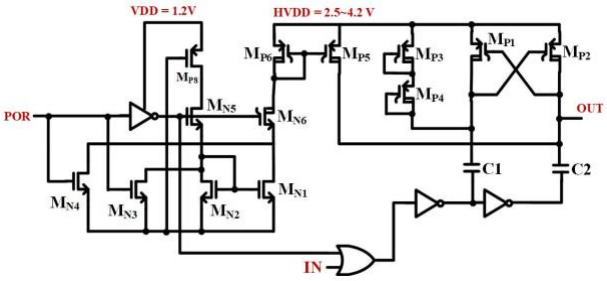

Fig. 4. Capacitively cross-coupled level shifter.

switch once the output voltage drops below the lower bound of the hysteretic band and turns it off once the output voltage rises above the higher bound of the hysteretic band. At steady state, the peak-to-peak value of output voltage ripple $\Delta V_{OUT\_p\text{-}p}$ equals to the effective hysteretic band V_{He},

$$V_{He} = \Delta V_{OUT\_p\text{-}p} \tag{1}$$

The capacitor current I_{CL} during on time is expressed as:

$$I_{CL}(t) = \alpha_1 t - I_L \tag{2}$$

where I_L is load current, $\alpha_1 = I_P / T_{ON}$ is the charging rate of the inductor, and I_P is inductor peak current, T_{ON} is the on time. The peak-to peak value across the output capacitor C can be expressed as the integration of capacitor current from 0 to T_{ON}:

$$V_{C\_p\text{-}p} = \frac{I_P^2}{2\alpha_1 C} - \frac{I_L I_P}{\alpha_1 C} \tag{3}$$

In reality, the output capacitor can be modelled as an ideal capacitor C in series with an equivalent series resistance

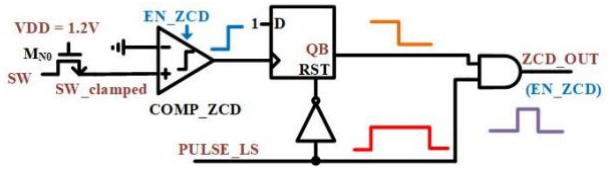

Fig. 5. Zero current detector

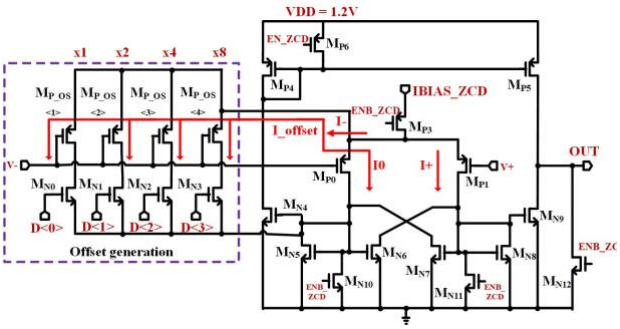

Fig. 6. ZCD comparator with imbalanced input pair

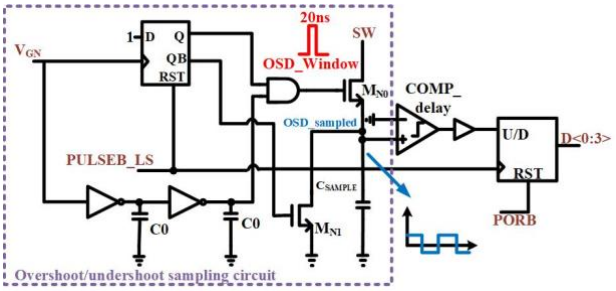

Fig. 7. Delay compensation circuit for ZCD comparator

(ESR). The composite equation of output ripple voltage can be expressed as:

$$\Delta V_{OUT\_p\text{-}p} = \frac{I_P^2}{2\alpha_1 C} - \frac{I_L I_P}{\alpha_1 C} + I_P * ESR \tag{4}$$

While the switching frequency f_{SW} can be represented by

$$f_{SW} = \frac{2\alpha_1 I_L}{\left(1+\frac{\alpha_1}{\alpha_2}\right) I_P^2} \tag{5}$$

where $\alpha_2 = I_P / T_{OFF}$ is the discharging rate of the inductor. From Equation (1) (4) and (5), the relationship between the hysteresis and switching frequency at steady state can be corelated and shown in Fig. 2.

III. Controller Circuit Implementation

A. Hysteretic Comparator with Dynamic Biasing Current

The schematic of the cross-coupled hysteretic comparator is shown in Fig. 3. Adaptive biasing is introduced to allow the comparator to be biased dynamically subjected to the input condition [11]. When the buck converter is disabled, a 150 nA biasing current will be turned on to monitor the output and wait for the starting point of the next cycle. After V+ drops below V-, VOUT falls from 1 to 0 and an additional 450nA biasing current will be enabled to enhance the comparator speed. As a result, the rising and falling edges of VOUT are imbalanced but the quiescent current can be reduced to 25% of the normal biasing. However, the limited

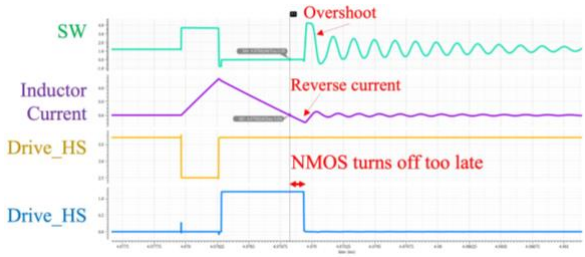

Fig. 8. Overshoot observed due to PMOS body diode conduction

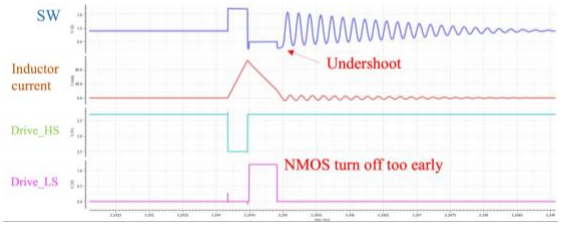

Fig. 9. Overshoot observed due to PMOS body diode conduction

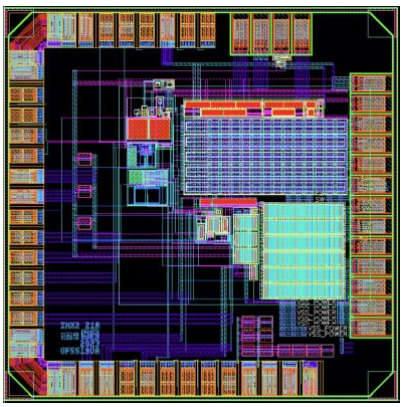

Fig. 10. Layout of the proposed buck converter

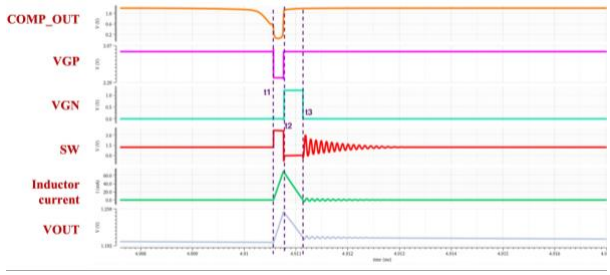

Fig. 11. Operational waveform of buck converter

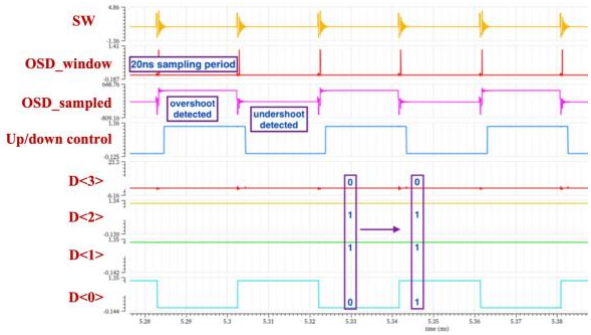

Fig. 12. waveform of the ZCD comparator delay compensation circuit

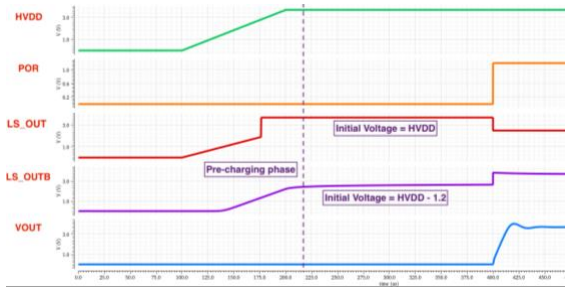

Fig. 13. Startup waveform of the level shifter

slew rate of the falling edge will cause voltage glitches. Therefore, to eliminate the glitch, a one-side hysteresis of 8 mV is added so that the 0 to 1 output change can only happen after getting over the hysteresis. This additional hysteresis will cause a drop in switching frequency, and result in smaller switching loss.

B. Capacitively Cross-coupled Level Shifter

As the interface between different supply voltage domain of the controller circuit and power switches, the 1.2V ground-referenced control signal is shifted up to be HVDD referenced by the level shifter, as shown in Fig. 4. The capacitively cross coupled level shifter has the advantage of zero static power consumption and negligible propagation delay [12, 13], compared with the conventional level shifter topology with differential cascode voltage switch (DCVS) [14], which consumes static power.

During initial startup phase, proper charging of the capacitors C_1 and C_2 from 0 to appropriate voltages is crucial to the reliability of the gate driver and the operation of the power converter. Moreover, LS_OUT is designed to follow the ramp-up of HVDD to keep the PMOS switch off during startup and protects the gate of HV PMOS devices.

C. Zero Current Detector with Delay Compensation

To prevent reverse current conduction loss, a zero current detector is necessary for the buck converter in DCM operation. Fig. 5 shows the schematic of zero current detector which utilizes a comparator to detect the crossing point where the voltage of the switching node SW drops to zero. Since switching node voltage SW has exceeded gate voltage limitation, SW is clamped by an always-on NMOS switch MN0 at (1.2-V_{TH}), otherwise MN0 will be turned off. Therefore, low-voltage devices can be used as the input pair of COMP_ZCD. At the zero-crossing point of inductor current, the output of COMP_ZCD will change from 0 to 1. The D flip-flop will sense this rising edge and ZCD_OUT will be generated to turn off the NMOS switch when reverse conduction happens.

However, the reverse current conduction cannot be eliminated thoroughly due to the delay of ZCD comparator. therefore, an imbalanced input pair technique [15,16] is adopted to purposely create an offset at the input of COMP_ZCD, as shown in Fig. 6. Due to this offset, the comparator output will rise from 0 to 1 before the actual zero crossing point to compensate for the propagation delay. The amount of the offset is decided by the control loop of the delay compensation circuit.

As shown in Fig. 8 and Fig. 9, when NMOS switch is turned off too late, the reverse current conducts. When the NMOS switch is turned off, the reverse current will continue to flow from output to SW. The body diode of PMOS switch is forward-biased and therefore an overshoot can be observed at the switching node. On the other hand, when NMOS switch is turned off too early, the current continues to flow from ground to output. The body diode of NMOS switch will be

TABLE I. PERFORMANCE SUMMARY

	[8]	[9]	[17]	[18]	This Work
Technology	180nm	90nm	130nm	130nm	55 nm
Control scheme	DCT + PWM	HA-AMOT	SBHC	RM+PFM+PWM	Hysteretic control
Input voltage (V)	2-5	1.8-4.2	1.8-3.3	2.2-3.3	2.5-4.2
Output voltage (V)	0.8, 1, 1.2,1.8, 3	0.9-1.4	1.2	1.7	1.2
Load current	1μA -50mA	40mA (Maximum)	100nA-2.65mA	10μA-20mA	2 μA-100mA
Inductor (μH)	2.2	4.7-10	18	3	6.8
Output capacitor (μF)	4.7	2.2-10	0.056	3	2.2
Quiescent current (nA)	470	12000	440 (w/o bandgap)	500	430 (w/o bandgap)
Efficiency (%)	85.6 @ 10 μA 92.7 @ 100 μA 93 @ 10 mA	78.5 @ 200 μA 83 @ 1mA 85.7 @ 10mA 85.6 @ 40mA	62 @ 10 μA 85 @ 100 μA 92.2 @ 2.65 mA	74.2 @ 10 μA 82.7 @ 100 μA 92.4 @ 20mA	71.7 @ 2μA, 77.8 @ 3.3μA 85.1 @ 10μA, 88.3 @ 100μA 88.6 @ 1mA, 86.3 @ 10mA 85 @ 50mA, 86 @ 100mA
FOM[a] (pA/%)	11	N.A.	26.8	337	10.83
Area	1.1	0.1	0.14 (w/o pad ring)	0.66	1.69

[a]FOM [8] $=I_{LOAD\_min} \times I_Q / (I_{LOAD\_max} \times \eta@10\mu A)$, where I_{LOAD_min}, I_{LOAD_max}, $\eta@10\mu A$ represents the maximum and minimum load current value and efficiency at 10μA. (smaller value is better)

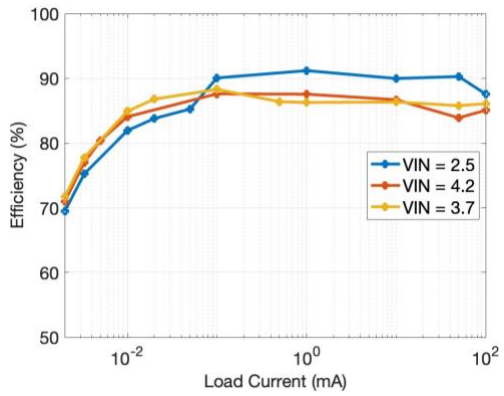

Fig. 14. Efficiency v.s. input voltage and load current conditions

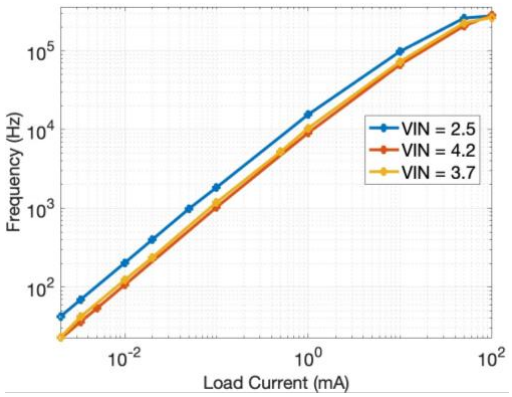

Fig. 15. Switching frequency v.s. input voltage and load current conditions.

forward-biased and an undershoot at the switching node will be observed. Therefore, switching node voltage is a good indicator to find the optimal timing to turn off NMOS switch.

The delay compensation circuit is shown in Fig. 7. The overshoot/undershoot of switching node voltage is sampled by a 20ns sampling window, after NMOS switch is off. The sampled voltage will then be compared to 0 and then become the up/down control of the counter, and the counter output will adjust the offset by a 5mV step.

IV. POST-LAYOUT SIMULATION RESULTS

The proposed buck converter has been implemented in a 55nm CMOS BCDLITE process. The layout is shown in Fig. 10, which is 1.3 mm × 1.3 mm including pads and the core circuit size is 0.8 mm × 0.8 mm. Fig. 11 shows converter core waveform operating in typical condition, i.e., V_{IN} = 3.7 V, V_{OUT} = 1.2 V, I_{LOAD} = 1mA. The buck converter operates at 12.5 kHz, and the output ripple is 56 mV. When V_{OUT} drops below the lower bound of hysteretic window, COMP_OUT falls at a limited slew rate. High-side control signal V_{GP} is generated to turn on M_{P0} at t_1. At t_2, when V_{OUT} exceeds the upper bound of the hysteretic window, after a 4 ns deadtime, a low-side control signal V_{GN} will rise to turn on M_{N0} until t_3, when the reverse current is detected and M_{N0} is switched off. The buck converter will be deactivated until the start of next cycle. Fig. 12 shows the waveform of the delay compensation circuit for ZCD at steady state. The overshoot/undershoot of the switching node voltage is sampled during the 20ns window, and the counter output oscillates between two adjacent points 0110 and 0111, which indicates the optimal timing has been achieved. Fig. 13 shows the startup operation of the level shifter, as HVDD ramp up from zero.

The efficiency plot across full load current and input voltage range is shown in Fig. 14. The converter has achieved a peak efficiency of 91.2 %, 88.6 % and 87.6 % at 2.5V, 3.7V and 4.2V input respectively. The switching frequency of PFM controller has been plotted in Fig. 15, which ranges from 20Hz to 300 kHz. The linearity of switching frequency at 100 mA is not as good as lower load current conditions. Because the converter is entering continuous conduction mode (CCM), while the proposed controller is optimized for DCM operation. The results are summarized and compared with prior works in Table I. It has achieved a higher than 85% efficiency between 10 μA and 100mA load current, with a 430nA quiescent current. The design has achieved a light load efficiency that is comparable to [8] and higher than [9], [17] and [18], with a simple hysteretic PFM controller.

V. CONCLUSION

In this paper, a battery input buck converter applied with power saving techniques for light-load efficiency enhancement and delay compensation loop for ZCD has been proposed. It has achieved a higher than 85% efficiency between 10 μA and 100mA load current, with a 430nA quiescent current.

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