Emerging Opportunities for Ferroelectric Field-effect transistors: Integration of Two-dimensional Materials

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Abstract: The rapid development in information technologies necessitate rapid advancements of their supporting hardware. In particular, new computing paradigms are needed to overcome the bottleneck of traditional von Neumann architecture. Bottom-up innovation, especially at the materials and devices level, have the potential to disrupt existing technologies through their emergent phenomena. As a new type of conceptual device, 2D ferroelectric field-effect transistor (FeFET) is highly sought after due to the potential integration with modern semiconductor processes. Its low power consumption, area efficiency, and ultra-fast operation provides an extra edge over traditional technologies. This review highlights recent developments in 2D FeFET, covering their device construction, working mechanisms, 2D ferroelectric polarization mechanism, multi-functional applications and prospects. In particular, the combination of 2D semiconductor and ferroelectric semiconductor for multi-functionality applications is discussed. This includes non-volatile memories (NVM), neural network computing, non-volatile logic operation, and photodetectors. As a novel device platform, 2D semiconductor and ferroelectric interfaces are bestowed with plethora of emergent physical mechanisms and applications.

1. Introduction

Ferroelectric materials have attracted extensive research interest due to their unique properties such as polarization hysteresis, non-volatility, semiconducting, and multiferroicity (Figure 1a).[1-3] Through the strong modulation of ferroelectric dynamics on the semiconductor channel conductance state, FeFET has become a promising candidate for next-generation multi-functionality FET.[4-6]

Traditionally, FeFET was considered as a type of non-volatile memory for the storage of binary data (0, 1) depending on the direction of ferroelectric polarization, that is either up or down (Figure 1b).[7, 8] Driven by the external electric field, the FeFET-based memory can not only read and write data in a non-destructive way, but also has better compatibility with the current Complementary Metal Oxide Semiconductor (CMOS) platform.[1, 9]

Owing to the rapid development of information technology in the past decade, especially with the rise of artificial intelligence (AI), the internet of things and machine vision, traditional hardware are struggling to keep up with the rapidly evolving requirements of these technologies.[10, 11] Take massive-data tasks for example, computing systems now require batch parallel

processing to frequently access results and interact with the memory domain simultaneously (Figure 1c).[11, 14] Moreover, the emerging robotics technology, autonomous driving, and satellite remote sensing require highly sensitive, fast, broad-range vision systems as well as photodetectors (Figure 1d).[15, 16] However, due to the separation between computing and memory modules in traditional von Neumann architecture, this process becomes both energy and time consuming.[17] As such, the requirements for massive data processing, ultra-fast computing speed, ultra-low power consumption and high accuracy present challenges for traditional Si-based FeFETs. For example, epitaxial growth of ferroelectric oxides at the Silicon-like interface, chemical potential difference, surface dangling bonds, lattice mismatch and incompatibility with the incumbent CMOS processes (high temperature with excess O_2) hinder/limit their practical application (Figure 1e).[4] These challenges stimulated a bottom-up innovation, especially at the low-level hardware (materials and devices level). As a three-terminal device with unique ferroelectric field control and an atomically thin channel, 2D FeFETs allow for a wide gamut of circuit designs to efficiently address the diverse needs of emerging computing paradigms and multi-applications (Figure 1 f).[18- 21]

The emergence of two-dimensional (2D) vdW materials is timely because they provide new opportunities for the FeFET platform. 2D-materials-based FETs exhibit a number of major advantages over traditional FETs. Firstly, carriers are confined in an atomically thin channel where carrier concentration can be uniformly modulated by gate voltage, thereby greatly suppressing leakage current as well as the short-channel effect.[22] Secondly, the dangling bond-free surface and clean vdW interface are not only beneficial for high-quality integration but also lead to stable and long retention time memories (Figure 1f).[23] Consequently, these atomically thin channels enable ultralow energy consumption and ultrafast computing.[18] Third, the tunable bandgap of 2D materials and intrinsic low-dark current are desirable for high-sensitivity, broadband vision systems as well as photodetectors. [24-28] Fourth, compared to traditional bulk materials, atomically thin channels of 2D materials enable multilayer stacking and are transferable to various substrates (e.g., flexible substrate), allowing high integration and multi-functional applications.[29] And finally, generous novel ferroelectric polarization mechanisms such as interlayer-charge-transfer, dipole-locking effect, sliding ferroelectric and strain effects have been found in 2D materials, all of which promote the development of 2D ferroelectric semiconductor FET (FeSm-FET).[30- 34] The discovery of 2D FeSm-FET holds promise in truly overcoming the bottleneck in ferroelectric dielectrics, which includes the inability for continuous scaling down in vertical and planar dimensions and thus withhold immerse potential for high-density, low-consumption, fast computing in memory（CIM）.[18-35] The benchmarks

for the standard logic/memory technology with 2D FeFET are summarized in Table 1. [14, 19, 35-37] As observed, the 2D FeFET bears competitive advantages,including relatively low operating voltage (1.5 V), steep-slope logic switching (< 60 mV/dec), ultra-fast operating speed (0.1-1 GHz), low power consumption (< 10 fJ), and extended memory retention time (> 10 years). These characteristics position it as an exceptionally promising candidate for future advanced electronics applications.

In this review, we provide an in-depth examination of 2D FeFET advancements over recent years, including the working mechanism, structural evolution, as well as the diverse applications within the realm of 2D ferroelectrics ranging from NVM, CIM, and vision systems to photodetectors. Finally, the review concludes with a summary of ongoing research efforts and offers further perspectives on the emerging opportunities for 2D ferroelectrics.

2. Combining 2D Semiconductors with Ferroelectric Dielectrics

Since the first demonstration of 2D FeFET, enormous progress has been achieved in the understanding and combination of 2D semiconductors and ferroelectric dielectrics. Here, we briefly discuss the concept of ferroelectrics, followed by the working principles of the 2D FeFET. Ferroelectrics are materials with an intrinsic non-centrosymmetric phase that induces spontaneous electric polarization within a certain temperature range.[3, 38] In ferroelectric materials, an electric dipole moment can exist naturally and the polarization direction is reversible by applying an external electric field.[3] Even after removing the applied electric field, the polarization can still be retained over long periods, that is, the state is non-volatile. The promising employed ferroelectric material is $HfZrO_2$ (HZO), which was first reported in 2011 and can be easily grown using Atomic Layer Deposition (ALD).[41] Owing to its intrinsic high dielectric constant, HZO holds great promise for realizing nonvolatile memories, such as ferroelectric-random-access-memory (FeRAM), FeFET, ferroelectric tunneling junction (FTJ) and is conducive to the integration with exsiting CMOS technologies for industrialization.[43] Until now, HZO remains one of the frontiers and a focal point in the realm of modern semiconductor technology research.[41] Here, typical methods used to characterize ferroelectricity encompass polarization-bias voltage hysteresis loop, dielectric permittivity, second harmonic generation (SHG), and piezoresponse force microscopy (PFM).[38] In addition to HZO, common ferroelectric dielectrics include perovskite-oxide ($BaTiO_3$), $Pb(Z_rXTi_{1-X})O_3$ (PZT), organic-polymer (P(VDF-TrFE)), and novel 2D vdW ferroelectrics. As shown in Figure 2a, the dipole of $BaTiO_3$ originates from the displacement of the central Ti ion. PZT demonstrates a low coercive field, high polarization, and a high dielectric constant, but it suffers

from a low bandgap, low crystal quality and environmental issues. PVDF is an organic ferroelectric material that exhibits good flexibility but poor thermal stability and can be obtained by solution process such as spray printing techniques.[4] Notably, in 2016, the identification of the 2D vdW ferroelectrics $CuInP_2S_6$ (CIPS), with its clean interfaces and ultrathin ferroelectricity limit (as low as 4 nm), opens up numerous possibilities for diverse applicationsutilizing vdW heterostructures (Figure 2b).[42] In general, the combination of 2D semiconductor and ferroelectric dielectric materials can be typically classified into three configurations: Metal Ferroelectric Semiconductor (MFS), Metal-Ferroelectric-Insulator-Semiconductor (MFIS) and Metal Ferroelectric Metal Insulator Semiconductor (MFMIS) (Figure 2c).[44] In the following sections, we discuss these configurations and their working mechanisms, as well as in-memory applications.

2.1 Structure of 2D FeFET

In the introduction of this chapter, we first compare the different device structures (MOS, MF(I)S, MFMIS). In MOSFET, the channel conductance (switch on or off) can be controlled by applying a gate voltage via a high-quality dielectric layer.[22] However, the memory function is lacking in MOSFET. In the FeFETs based on the MFS structure, the dielectric layer is replaced with a ferroelectric layer which enables the device to possess memory functionality by controlling the ferroelectric polarization through an applied voltage.[44] However, it has a short retention time and high leakage current.[44] By inserting a buffer layer (insulator layer) between the ferroelectric layer and the channel layer, MFIS structured FeFETs can effectively improve retention time and reduce leakage current.[1] Although the operation voltage of the MFIS structure is relatively high, it can be effectively reduced by independently designing the MFM (metal ferroelectric metal) and MIS (metal insulator semiconductor) structures which also simultaneously improves retention time.[45, 46] The MFMIS structure is relatively complex and introduces additional fabrication processes, which may delay the progress of advanced nodes.[1] To date, the MFIS and MFMIS structures are commonly used. For a more intuitive comparison of MOS-, MF(I)S-, and MFMIS-FET, a radar map is presented in Figure 2d, showcasing key parameters such as operation voltage, R_{on}/R_{Off}, switching speed, and energy consumption.[1]

2.1.1 MFS or MFIS Structure

The MFS configuration represents the most basic structure of FeFET and it only contains the metal, ferroelectric and semiconductor layer.[7] The working mechanism of a FeFET is different from that of a general FET. In a FET, the channel conductance decreases or increases

with the magnitude of an applied electric field. Once the external electric field is removed, the carriers within the channel are no longer manipulated, leading to the loss of information. Whereas in FeFET, the distinguishing factor is the controllability of channel carriers by its ferroelectric polarization after the gate voltage has been removed. To better understand this process, we look deeper into its band structure (Figure 3a). Taking an n-type FeFET as an example, polarization is achieved by applying a positive voltage greater than the coercive voltage (V_c). This aligns the ferroelectric polarization into a single direction, which induces a rapid change in surface potential and channel conductance. In this state, electrons accumulated in the interface between the ferroelectric layer and the semiconductor layer result in a low channel resistance (ON state). Thereafter, the high conductance state is maintained by the persistent ferroelectric domains even if the external electric field is gradually withdrawn. This enables nondestructive reading and writing operations. Only by applying a negative poling voltage exceeding the negative V_c can the ferroelectric domains be reversed, leading to a sharp increase of channel resistance that erases the ON state and switches to the OFF state. The result is a clear hysteresis loop observed in the I_d-V_g curve. The ON/OFF states can be easily programed or erased by selectively applying the required poling voltage, thereby forming the binary memory states. As a result, non-volatile memories are obtained via the remnant ferroelectric polarization field. Figure 3b shows the polarization-electric field (P-E) loop of a 2D FeFET based on 2D transition metal chalcogenides (TMDs) as the channel and a ferroelectric dielectric layer made of PVDF, with its optical image shown in the inset.[25] The coercive field and remanent polarization of PVDF are 22.5 V and 7 $\mu C\ cm^{-2}$, respectively, and a large memory window is oberserved (Figure 3c).[25] It is worth noting here that the memory window is very sensitive to the actual operation, and employing different reading operations can exert substantial influence on its behavior. The polarization up (P_{up}) and down (P_{down}) states are achieved by applying poling voltages of 40V and −40V, where the MoS_2 channel becomes fully accumulated and depleted, respectively (Figure 3d). The memory window of the FeFET is mainly determined by the V_c of the ferroelectric layer. Since the operating voltage is proportional to the V_c and a lower operating voltage corresponds to a smaller memory window, scaling the thickness of the ferroelectric layer is a feasible way to maintain the memory window and reduce the operating voltage.

For practical applications, the MFS structure experiences various problems such as large leakage current and short memory retention time. In the MFS structure, the leakage current through the interface of the ferroelectric/semiconductor reduces apparent dielectric polarization and promotes the degradation of the retention time, thereby leading to the gradual decrease of

the ON/OFF ratio.[44] To mitigate these problems, an insulating layer is usually inserted between the ferroelectric layer and semiconductor layer, forming the MFIS structure. The MFIS structure provides a better interface and thus lower leakage current, substantially extending the memory retention time (improvement of at least one order of magnitude in many studies). Inevitably, however, insertion of an insulating layer between the ferroelectric layer and the semiconductor layer results in the MFIS structure being configured as a dual capacitor structure. The working mechanism and energy band of the MFIS structure are similar to that of MFS structure. Figure 3e shows the schematic diagram of a constructed MFIS structure with an additional h-BN layer.[49] Figure 3f shows the transmission electron microscopy (TEM) image of fabricated vdW CIPS / h-BN / In_2Se_3 heterostructure which revealed the high-quality interface within the 2D FeFET.[49] Excellent memory performance is demonstrated through the stable source-drain current in both P_{up} state and P_{down} state for more than 10^4 s (Figure 3g).

2.1.2. MFMIS Structure

The performance of FeFETs can be further improved by employing the MFMIS structure, where a metal layer is inserted between the insulator layer and the ferroelectric layer to act as a floating gate.[46] The Benchmarks of MFMIS-structure FeFET with flash were listed in table 2. To obtain a high performance FeFET, the matching of ferroelectric polarization with the induced charge in MIS is crucial. However, in MFS and MFIS structures, the remanent polarization of ferroelectrics such as PVDF (~ 7.8 $\mu C/cm^2$) is usually much larger than the maximum charge that can be induced in the dielectric layer such as SiO_2 (approximately 3.5 $\mu C/cm^2$).[46] This sizeable charge difference means that only a small part of polarization can be used. In other words, one of the minor P-E loops (below maximum charge induced in dielectric layer) substitutes for the saturated P-E loop and correspond to a smaller V_c. In that case, the memory window (~2 V_c) will be much smaller. More importantly, the incomplete charge compensation will induce a large depolarization field that destroys the memory state resulting in short retention times. The merit of MFMIS structures is that MIS and MFM modules can be designed independently. By carefully designing the area ratio of MFM and MIS modules, ferroelectric polarization and induced charge in MIS can be well-matched, leading to a larger memory window corresponding to the saturated P-E loop and longer memory retention time due to the smaller depolarization field.

Based on the MFMIS structure, Liu et al. constructed a 2D vdW FeFET device using only vdW crystals with MoS_2 as a channel layer, h-BN as a dielectric layer, CIPS as a ferroelectric layer and graphene as a floating metal layer (Figure 4a).[23] Figure 4b shows the PFM amplitude

image of the device. A typical *n*-type behavior exhibits a counterclockwise hysteresis loop. With increased sweep range of the gate voltage, a large memory window of 3.8 V is achieved (Figure 4c), much larger than the corresponding CIPS FeFET made using the MFS structure. A high program/erase ratio of 10^7 is are realized, contributing to a low OFF-state leakage current and sufficiently compensating ability of graphene floating gate layer. In FeFET, the loss of memory retention time mainly originates from incomplete charge compensation-induced depolarization and carrier charge trapping.[4] From the band diagram in Figure 4d, the MFMIS structure makes the compensation charge closer to the surface of the ferroelectric layer, thereby reducing the effect of the residual depolarization field. This enables the vdW FeFET to operate with a major ferroelectric hysteresis loop and be less vulnerable to the internal depolarization field. Furthermore, leakage current is suppressed using the high tunneling barrier from h-BN and an ideal trap-free interface between MoS_2/h-BN/graphene/CIPS. Figure 4e shows the calculated trap concentration and E_d/E_c ratio of vdW stacking with common ferroelectrics HZO, PZT, PVDF.[51, 52] 2D vdW structure exhibits much lower E_d/E_c ratio and trap concentrations, which prevents retention loss. As a result, memory deterioration is negligible even after 10^4 cycles and a long retention time of 10 hours extrapolated (linear extrapolation) to more than 10 years is achieved (Figure 4f).

2.2 Scalability of the 2D FeFET

The scalability of 2D FeFET will be discussed in two application scenarios, including logic devices and memory devices. For logic device, scalability arises from device scaling down, and improved device performance (like small subthreshold swing value, high on current, high carrier mobility). Firstly, 2D FeFETs offer a unique advantage in vertical and planar continuous scaling since 2D vdW materials maintain ferroelectricity even at atomic-level thicknesses.[3] While traditional ferroelectric materials exhibit a disordered polycrystalline microstructure at thicknesses below 10 nm, 2D materials do not suffer from randomly distributed structural grains which greatly improves the stability of the devices. Secondly, the negative capacitance (NC) effect gives 2D FeFETs a subthreshold swing (<60 mV/dec) that is less than the theoretical limit, which is crucial for achieving low-power logic computation. Thirdly, 12-inch single-layer uniform MoS_2 has been successfully synthesized, and the MoS_2-based FET arrays exhibit a high mobility of 122 $cm^2V^{-1}s^{-1}$ and a on current of 1.27 mA/μm, which exceeds the target performance of the FETs in 2028. These advancements have also facilitated the scalability of 2D FeFET to industrial-level mass production. However, there are some challenges, such as hysteresis issues with NCFETs, the variability of growing large area 2D materials directly on

the target substrate, and the fact that wafer-scale 2D ferroelectric materials are not currently available.

For memory device scalability, it involves 3D stacking, high-density integration, and vertical device architecture. vdW interface allows arbitrary stacking without fear of lattice mismatch and is one of the main advantages for 2D FeFETs. By utilizing vdW integration, adjacent functional layer devices can be seamlessly bridged. Despite the great promise, immature wafer-level 2D material transfer techniques still limit 3D vertical high-density integration of 2D FeFETs. (Although some breakthroughs have been made, such as vdW template-assisted growth and large-area 2D material transfer).

3. FeFET based on 2D Ferroelectric Semiconductors

With artificial intelligence and the Internet of Things poised to disrupt the semiconductor industry, devices with ultra-efficiency, ultra-low-power, sustainable miniaturization and full integrability and compatibility with existing semiconductor technologies are urgently needed.[10, 11] To pave the way for expanding artificial intelligence and sensing capabilities, ferroelectric semiconductors are a promising candidate by combining ferroelectric technology with traditional components in computers and smartphones.[34] Different from the forementioned structures based on 2D semiconductor channels and ferroelectric dielectric, the emerging FeSm-FET combines ferroelectric semiconductor channels and the mature dielectric gating technology.[54] In FeSm-FET, the ferroelectric polarization charges accumulate on both the top and bottom surfaces of the ferroelectric semiconductor rather than the ferroelectrics/semiconductor interface. This aids in further optimizing the long-standing interface complexity of ferroelectric-dielectric/semiconductor by replacing them with a high-quality, well-established dielectric process that reduce charge trapping and leakage current. Moreover, the mobile charges can screen the depolarization field across the ferroelectric semiconductor and improve the device stability. In this section, we provide an overview of the unique properties of 2D ferroelectrics and the working mechanism of 2D FeSm-FET.

3.1. Unique Properties of 2D vdW Ferroelectrics

Distinct from conventional oxide-based ferroelectrics, 2D ferroelectric materials with weak interlayer interactions and periodic vdW gaps exhibit unprecedented ferroelectric physics. One of the most unique ferroelectricity mechanisms in 2D vdW materials is the interlayer-charge-transfer-induced polarization demonstrated in bilayer WTe_2 in 2018 where the coexistence of ferroelectricity and metallicity was first proven in the 1960s.[30] This unique effect

allows ferroelectricity to even exist in centrosymmetric materials, which greatly broadened the range of ferroelectric materials. For example, in 2D paraelectric materials such as h-BN, switchable polar ordering can be produced by twisting or sliding a single layer on another single layer.[54] This ferroelectricity is widely existed in 2D vdW stacked layers such as InSe, ZrI_2, TMDs, where vertical polarization is switched through in-plane interlayer sliding. At present, the remnant polarization of twist bilayer h-BN (P_r≈0.68 μC/cm^2) is lower than that of traditional ferroelectric materials such as HZO (~30 μC/cm^2), PVDF (~7.8 μC/cm^2), and $BaTiO_3$ (~10 μC/cm^2). However, this unique mechanism exhibits an ultralow switching barrier, enabling high-speed data writing with low energy cost and ensuring the memory's robustness at the atomic scale.[15] The physical mechanisms and applications of sliding ferroelectrics need to be further investigated. In addition, doping is one of the effective strategy to modify the lattice structure of 2D materials to induce ferroelectricity. For instance, Zhu et al. demonstrated that doping rare earth element Y into γ-InSe results in room-temperature spontaneous polarization of out-of-plane and in-plane ferroelectric properties. The suitable bandgap (1.0-1.6 eV) and high electron mobility (~1000 cm^{2}v^{-1}s^{-1}) of γ-InSe have propelled the advancement of ferroelectric semiconductors.

In traditional ferroelectrics, when the thickness falls below a critical value, the depolarization field increases significantly, resulting in an unstable intrinsic polarization.[55] But in 2D vdW materials, a novel stabilization mechanism allows switchable polarization to be maintained even in the monolayer limit. This stabilization mechanism originates from the simultaneous locking of in-plane and out-of-plane dipoles (Figure 5a). For example, in α-In_2Se_3, the asymmetric position of the central Se atom stacked by five covalent bonds of Se-In-Se-In-Se spontaneously breaks the central symmetry and shares the common origin of polarization in both directions. The electrical switching of each dipole can cause the reversal of the other dipole. The interlayer influence could be ignored due to the vdW gap. More importantly, in the out-of-plane (or in-plane) direction, the structural instability caused by the depolarization field is offset or reduced by the in-plane (or out-of-plane) covalent bonds, ensuring that ferroelectric polarization is maintained within the monolayer limit.

Zhu et al. revealed the dynamic process of polarization reversal in α-In_2Se_3 through first-principal density-function theory (DFT) calculations in a three-step process (Figure 5b).[58] α-phase FE-ZB' (ABBCA) is one of two stable low-energy degenerate ground states in α-In_2Se_3.[54] In the first step, the α-phase FE-ZB' structure transforms to a metastable β-phase fcc' structure with a lateral shift of the top three atomic layers under an externally applied electric field. In the second step, the middle Se atoms rotate 60° along the c-axis to the degenerate fcc'

structure. Finally, the top two atoms shift toward the negative lateral direction that is rotated 60° away from the second step and an equivalent FE-ZB structure with reversed polarization is achieved. After the three-step process, the out-of-plane polarization is reversed from downwards to upwards and the in-plane polarization is reversed from [110] to $[\bar{1}\bar{1}0]$ simultaneously. The activation of this three-step process is only 0.066 eV/unit, which is comparable to conventional ferroelectric materials $PbTiO_3$ (0.07 eV/unit).[57] While the polarization reversal of α-In_2Se_3 exhibits a low activation energy through a three-step process, further studies are still required to assess the reliability of the polarization switching dynamics.

These DFT calculations were further corroborated with experimental breakthroughs where the out-of-plane and in-plane polarizations were examined by PFM. As shown in Figure 5c, the phases of out-of-plane and in-plane polarizations were acquired after writing two square patterns with opposite tip voltages (-7V and +6V).[58] It is observed that the out-of-plane polarization phase changes simultaneously with that of the in-plane polarization, which demonstrates the dipole-locking effect. Xiao et al. examined this effect by SHG and also showed that polarization fields are sensitive to changes in in-plane symmetry.[31] Figure 5d shows a uniform SHG intensity pattern of α-In_2Se_3. Next, a square region was scanned by an out-of-plane electric field with negative bias. After the writing process, an obvious square dark perimeter with low SHG intensity is observed that completely overlaps with the writing area. The destructive interference of in-plane nonlinear optics by an out-of-plane electric field patterning further proves the strong dipole-locking effect.

To provide a more comprehensive understanding of various ferroelectric materials, their key parameters are highlighted in Table 3.

3.2. Ferroelectric Semiconductor FET

Albeit the advantages of FeFET, its commercialization is restricted by two main reasons, namely depolarization field effect and leakage currents.[44] In response to these restrictions, the FeSm-FET configuration is proposed as a new device concept capable of fast operation speeds, low power requirements and non-destructive read/write capability.

The working mechanism of FeSm-FET is distinct from that of FeFET. In FeFET, the polarization charges accumulate at the interface between the ferroelectric layer and the semiconductor (Figure 6a), where exhibits a counterclockwise in I_d-V_g curve.[34] In FeSm-FET, the accumulation of polarization charges occurs at both the bottom and top surfaces of the ferroelectric semiconductor, which then determines the drain current I_d as shown in Figure 6a. For example, in the P_{up} (P_{down}) state, negative (positive) charges accumulate at the top (bottom) surface. This coupling of semiconducting nature and ferroelectricity makes the transport

mechanism more complex. On one hand, the mobile carriers in the channel allow non-uniformity of the electric field in different layers of α-In_2Se_3. On the other hand, the electric field within the channel determines the extent of ferroelectric polarization in α-In_2Se_3. As a result, the direction of I_d-V_g hysteresis curve is determined by the electric field in the channel where two different cases should be considered.

The strength of the electric field across the semiconductor is determined by the effective oxide thickness (EOT). For example, the EOT for a 15 nm HfO_2 dielectric layer is about 3 nm ($EOT=t_{HfO2}(\varepsilon_{SiO2}/\varepsilon_{HfO2})$). The maximum voltage applied for HfO_2 is 5V and the ratio of the maximum voltage applied to the EOT can reach up to 1.7 MV/cm, corresponding to a low EOT. [41] In comparison, the same ratio in a 90 nm SiO_2 layer is only about 0.56 MV/cm, corresponding to a high EOT. For high EOT, the crossed electric field is insufficient to penetrate into the top surface, thus only partial ferroelectric switching happens near the bottom of α-In_2Se_3 (Figure 6b). Therefore, the mobile carriers only accumulate at the bottom surface because of band bending in the P_{down} state which then results in a low channel resistance. In the P_{up} state, the channel carriers are depleted, leading to a high resistance state (HRS). Here, P_{down} and P_{up} states are realized by applying a negative gate voltage below the V_c and a positive gate voltage over the V_c, respectively. Therefore, a clockwise I_d-V_g curve is achieved. In low EOT, a ferroelectric switch occurs in the entire α-In_2Se_3 due to the sufficient electric field (Figure 6c) and the top surface becomes conducting. In the P_{up} state, mobile carriers accumulate at the top surface and exhibit a low resistance state (LRS). Similarly, a HRS is shown in the P_{down} state. As a result, a counterclockwise I_d-V_g curve in low EOT is observed.

Figure 6d shows the V_d-I_d curve at different gate voltages with the α-In_2Se_3 channel and SiO_2 insulator layer. A maximum current of 671 μA/μm and high mobility of 488 $cm^2V^{-1}s^{-1}$ is achieved, which indicates the good semiconducting nature of α-In_2Se_3. As expected, a clockwise I_d-V_g curve is observed with the high EOT (SiO_2) insulating layer, achieving a large memory window of 70 V. With HfO_2 as gate dielectric, a counterclockwise I_d-V_g curve with low supply voltage and high ON/OFF ratio over 10^8 is instead observed (Figure 6e) with a low leakage current down to 10^{-13} A/μm. In addition to α-In_2Se_3, the introduction of a tunable Schottky barrier in the γ-InSe-based sliding FeSm-FET has achieved high performance with a wide memory window and a large on/off ratio. These results open up a new pathway for the development of FeFET where the FeSm-FET exhibits a dazzling performance in long retention time memories, ultrafast switching and low power dissipation neural computing, which will be discussed in the following sections.

A summary of representative advances in 2D FeFET memories is provided in Table 4 which contains information on structure, ferroelectric layer, channel layer and device performance (ON/OFF ratio, memory window, endurance, retention time, operation speeds, power consumption) for different device configurations.

Among these devices, the MFMIS structure demonstrates the most superior device performance, such as low operating voltage and long retention time, albeit with a slight increase in its manufacturing process complexity. The 2D FeSm-FET offers significant advantages in terms of compatible with mature CMOS technology. However, the retention time and endurance of the device requires further investigation. To further improve device performance, an effective method is the scaling of both the channel thickness and ferroelectric layer thickness although there is a trade-off decrease in endurance. For 2D ferroelectric materials, α-In_2Se_3 and γ-InSe are promising ferroelectric channel materials for FeSm-FETs. And $CuInP_2S_6$ are promising ferroelectric insulator material for MF(I)S and MFMIS structure. Nevertheless, there remains a necessity for more extensive investigation to determine their ferroelectric stability and durability at atomic-level thicknesses, a crucial factor for future scaling down. Furthermore, the issue of depolarization field in 2D materials warrants additional attention, and a deeper understanding of the coexistence between ferroelectric fields and charge carriers is required.

4. 2D FeFET for Computing in memory

Ferroelectric materials typically exhibit piezoelectric effects, thermoelectric and electrocaloric responses, electro-optical and nonlinear optical activity, and other properties. As well as the outstanding performance exhibited by 2D FeFETs, they showcase attractive application prospects across various domains, including standard logic circuits utilizing NC FETs, standard memory arrays, CIM architectures, photonics, and flexible electronics.[5, 19, 26] Versatility underscores the potential of 2D FeFETs to enhances computing performance, energy efficiency, and data storage capabilities, as well as facilitate the development of new and innovative electronic/optoelectronic products. More importantly, in the emerging landscape of data-centric applications, 2D FeFETs offer distinct advantages in terms of power efficiency, speed, durability, and area utilization, both in logical and neural form computing.[18, 21] They provide a promising solution for efficiently processing vast datasets and overcoming bottleneck in memory logic interconnections. This section of our review will focus on recent developments in 2D FeFET for CIM.

4.1. Spiking Neural Networks and Artificial Neural Networks

Traditional computing platforms face many bottlenecks in processing complex information and exhibit inefficiencies in terms of time latency and energy cost. [10, 11] To move beyond the traditional route of relying on the separation of computation and storage under the von Neumann architecture, neural computing is proposed as a new computing paradigm to model the biological brain where information processing and memory function are strongly intertwined.[10] Neural networks composed of an enormous number of neurons and synapses are capable of processing multiple streams of complex information while being versatile, adaptive and power efficient.[62] By tightly integrating memory and processing units, a modular, parallel, distributed, and scalable computing system with low power consumption and large bandwidth can be achieved.

Two major neural computing methods commonly used are ANN (artificial neural networks) and SNN (spiking neural networks).[63, 64] ANN is a biomimetic-based machine learning model consistings of multiple layers of neurons that learn to extract features from input data to generate outputs. Each neuron receives inputs from the other neurons and processes them using an activation function. The connections between neurons have weights that adjust the importance of input data and their impact on the model. The training process for ANN typically involves the use of a backpropagation algorithm, which calculates the partial derivatives of each weight with respect to the loss function and updates the weight values in the direction of the gradient. Through iterative training, the neural network can optimize the weights to better fit the training data and make accurate predictions. ANN has a certain nonlinear modeling capability and can handle data with complex relationships. It has wide applications in image recognition, speech recognition, natural language processing and other fields. However, ANN also faces some challenges, such as the need for a large amount of training data, the complexity of the model structure, and the tendency to overfitting (the model to learn the noise or non-generalizable patterns present in the training data).[63, 65]

SNN is a neural network model based on the transmission of neural spikes and temporal encoding.[64, 66] Unlike ANN, SNN simulates the spikeing signals transmission between neurons, which is closer to the working principles of the biological brain. In an SNN, information is encoded in the form of spikes. Each neuron in an SNN accumulates incoming spikes over time and generates the output spike when a certain threshold is reached.[66] SNNs capture the temporal dynamics of information processing, allowing for more precise modeling of neuronal behavior. This makes them particularly suitable for tasks involving time-dependent data, such as speech recognition, event forecasting, or motion detection. Compared to ANNs, SNNs have been shown to exhibit more energy-efficient processing capabilities, as they emit spikes only when

necessary, mimicking the sparse firing patterns observed in biological neurons. However, SNNs also come with challenges. Training SNNs is more complex than training traditional ANNs due to the temporal nature of spiking signals. It requires specialized learning algorithms, such as spike-time-dependent plasticity (STDP), which adjust the synaptic weights based on the relative timing of pre- and postsynaptic spikes.[64, 66]

The strong residual polarization, subtle electrical current controllability, and weak depolarization effect of 2D ferroelectrics make them a promising solution to address the existing limitations in neuromorphic devices.[3] The overall low power consumption, fast memory state switching, good linear weight update, multiple conductance states, long memory stability, and high accuracy of FeFETs, therefore, provide an excellent platform for further development of ANN and SNN.[5, 9, 20]

Zhou et al. constructed a 2D FeSm-FET to investigate neural computing.[18] The schematic diagram of the device is shown in Figure 7a. Here, α-In_2Se_3 was used is used as the ferroelectric semiconductor channel layer. The channel resistance can be switched from a HRS to a LRS under a 40 ns ultrafast spike voltage and the memory state can be retained for a long period of time (over 500s), demonstrating the ultra-fast programmability of 2D FeFETs (Figure 7b). Next, neural computing based on such a device configuration is explored. In a biological neural network, the transmission of information is achieved through the release and transmission of neurotransmitters, which is triggered by spike action potentials. (Figure 7a).[21] In 2D FeFET-based neural computing, gate voltage pluses simulate pre-synaptic inputs, and the channel current is monitored as post-synaptic current (PSC). Long-term potentiation (LTP) and long-term depression (LTD) corresponding to progressive excitatory and inhibitory PSC modulation are the basic functions in ANN (Figure 7c). The ultralow input pulses amplitude of 0.5 V indicates ultra-low energy consumption. Next, a typical short-term plasticity simulation, which is an important part of SNN, is performed as depicted in Figure 7d. By applying negative short spikes from -8V to -5V with 1V steps, the PSC increased with incremental spike amplitude and quickly restored to the initial state. Figure 8e shows the spiking rate-dependent plasticity (SRDP) in neural computing, which refers to the ability of synapses to enhance or weaken their response to neural activity or spiking at a range of frequencies, playing a crucial role in learning and memory. Figure 7e shows the spike rating-dependent plasticity (SRDP) in neural computing, where the gain of SRDP is proportional to the stimulation frequency. In high-frequency (low-frequency) stimulation, it exhibits a significant (weaker) inhibitory effect.[66] The energy consumption of simulated excitatory and inhibitory per spike is calculated to be about 234 and 40 fJ respectively, close to the energy consumption of biological synapses (~ 10 fJ),

demonstrating the immerse potential of 2D FeFETs in neural computing. In addition, the thermal configuration of the device for neuromorphic computing is shown in Figure 7f. Thermal assistance can provide a larger dynamic range for network weight mapping, which can help improve computational accuracy. For LTP, the mean PSC is increased with rising temperatures and strengthened LTP. Whereas LTD is inhibited with increasing temperatures. Thus, a standard ANN, including the input layer, hidden layer, and output layer, is constructed for training iris recognition and classification. The synergistic interaction of electric and thermal modulation is reflected in ANN. There are 5 input neurons corresponding to the length and width of the iris's calyx and petal and 1 bias in simulation (Figure 7g). And 3 output neurons are corresponding to 3 classes of iris flower. Software training and test are designed to the weight matrix in optimal recognition accuracy.[65] By mapping the channel conductance to the weight matrix, the mapped network can be obtained. Lastly, the recognition and classification of the mapped network are retested after the conductance weight matrix mapping. The training result of different temperature mapping is shown in Figure 7h, with the highest recognition accuracy reaching 94.74%, which is close to the software result, demonstrating the great potential of 2D FeFETs in neural network optimization.

4.2. Machine Learning based on SNN

As processes become increasingly complicated, an alternative method to process big data to uncover trends, patterns and correlations with enhanced energy and timing efficiency is desired.[67] One such alternative method is the reward-modulated spike timing dependent plasticity (R-STDP) based on SNN, which represents an important learning rule in AI technology inspired by human brain learning.[68] SNN tends to catch brain-like features, for example using spike compution, which is different with traditional deep learning approaches (neuronal models with static nonlinearities).[69] This is expected to continue to improve the computing energy efficiency. The learning rule of R-STDP is to modulate STDP via external environment to achieve SNN-based reinforced learning. For R-STDP, when pre- and post-pulse signals are generated, the weight updates are temporarily stored in the non-volatile eligibility trace. The eligibility trace aids in updating neural network weights and determining which states and actions contribute to changes in the current strategy. In R-STDP, the modulated weight changes only receiving the reward signal, and positive (negative) reward will lead to R-STDP (anti-R-STDP). Positive (negative) reward signals can strengthen (weaken) the connections between related neurons. Two opposite polarities are needed in one unit. Based on this, Cai et al. designed a 2T (two synaptic transistors) unit connected by two FeFETs in a parallel

configuration with WSe_2 channel and PVDF dielectric layer (Figure 8a),[81] where a typical bipolar behavior is observed (Figure 8b).[20] Hence, the two terminals can accept both positive and negative rewards, as shown in the designed circuit in Figure 8c. A triangular-shaped gate voltage pulse V_e is used as the eligibility trace and is only connected to the circuit upon the arrival of the reward signal (Figure 8d). When the positive (negative) reward arrives, V_e is connected to gate1 (gate2). The non-volatile nature of the FeFET allows the channel current to be stored in the eligibility trace even after V_e is removed. Figure 8e, f shows the experiment results of the measurements. When a positive (negative) signal arrives, the device effectively demonstrates the corresponding STDP (anti-STDP) behavior. The shorter the time interval between the reward signal and the pre-signal, the larger the change in conductance. When the time interval exceeds the time window of the eligibility trace, the conductance remains unchanged. To further adopt R-STDP implemented by 2T FeFETs to train SNN, a standard control task: cart-pole problem is used to evaluate the performance of RL algorithms and the hardware design (Figure 8g).[70] In the cart-pole problem, there are 4 environment variables: cart position x, dx, pole angle θ, $d\theta$ and the pole is balanced only if both θ and x below thresholds. Each variable is represented by multiple input neurons and once the simulated value of a variable falls within the particular encoded range, that neuron will sent out a spike as an input. The carting forces $\pm F$ are encoded by output neurons (Figure 8h). According to simulation results, the pole is successfully balanced after 500 steps (Figure 8i) and the energy consumption is 32 pJ, proving the potential of 2D FeFETs in building low-power consumption, area-efficient SNN hardware chips. The specific type of the neural network, learning accuracy, writing speed, and energy consumption for each type of FeFET are summarized in Table 5. Accordingly, it can be seen that 2D FeFET, especially the FeSm structure, not only has high learning accuracy but also ultra-fast writing speed and low power consumption in neuromorphic computing, providing an excellent platform for ANN and SNN.

4.3. Artificial Optoelectronic Synapses

Neuromorphic biological vision systems serve as a core part of AI technology in applications such as robotics and autonomous driving to perceive, memorize and process complex optical information.[73, 75] In order to mimic retinal-like neuromorphic vision sensors for image recognition and deep learning, integrating biometric sensing and synaptic learning functionalities of optoelectronic synapses are important hardware foundation.[75, 76] In a biological visual system, optical information received by the eyes is transmitted to the neuron through synapses, then processed and memorized in the neural network.[77] The learning process

is achieved through the weight update caused by light-induced neural activity. In a visual neural network, the combination of short-term plasticity and LTP is needed to realize light detection and synaptic plasticity learning simultaneously.

Based on this, Marin et al. constructed a 2D FeFET to simulate a biological vision system. Here, few-layer WS_2 is used as a channel layer, which has been demonstrated to possess excellent optoelectronic performance (Figure 9a).[24] In the WS_2/PZT heterostructure, light can effectively switch ferroelectric polarization and the device can simulate complex emulate complex light-controlled neuromorphic synaptic functionalities. Figure 9b shows superior multilevel optoelectronic memory switching performance. The input light pulse amplitude / width is 10 μW, 100 ms and each pulse train contains 5 light pulses. After each light pulse, the conductance remains stable for over 30 s. With increased light pulse training, the channel conductance gradually increases and reaches saturation. To understand this mechanism, light-assisted PFM measurements of the evolution of ferroelectric domain with increasing exposure time are shown in Figure 9c. After light illumination, WS_2 covered PTZ area and bare PZT area shown different domain patterns. This light-driven ferroelectric switching originates from the interaction between photo-generated charges of 2D semiconductor and ferroelectric polarization charges (Figure 9d). For example, when PZT is in P_{up} state, a built-in electric field (E_{in}) directed towards the bottom is present. Under light illumination, the light absorption in WS_2 eventually leads to the formation and decay of interlayer excitons. This brings positive charges to the WS_2/PTZ interface which compensates the negative charges and screens the upward polarization field, thereby facilitating the reversal of polarization driven by E_{in}. It is important to note that light cannot destroy the P_{down} state. This behavior of non-volatile light-induced increase in conductance and electrical-induced decrease in conductance can simulate LTP and LTD functions in biological synapses. Figure 9e shows the PSC as a function of pulse number and optical LTP, where the optoelectrical LTP synaptic functions in 2D FeFET are demonstrated when the electrical LTD process is successfully simulated. In addition to long-term synaptic plasticity, short-term plasticity also plays an important role in learning and memories. Short-term plasticity refers to the ability to relax back to the original state quickly, corresponding to STDP plasticity.[79] In this device, under low power illumination, the light-induced conductance decays rapidly (Figure 9f). Once the light-pulse is terminated, the current decays to 0.05% within a time period of 10 s. In contrast, under high power illumination, the relaxation time exceeds 100s which exhibits an obvious light-intensity-dependent decay process. This behavior arises from the persistent photoconductivity (PPC) effect where the low-intensity light is insufficient to induce permanent PZT domain change. Switchable light-

induced LTP and short-term plasticity unlock the possibility of simulating brain-like learning and memory, and thus ferroelectric-based optoelectronic memories can be extended to demonstrate efficient artificial synaptic devices, therefore proving the great potential of 2D FeFETs in future optoelectronic neural network systems.

The Benchmarks for 2D FeFET-based optoelectronic synapses are summarized in Table 6. Clearly, 2D FeFETs demonstrate the ability to accurately sense and process broadband optical information with high power efficiency.

4.4 2D FeFET-based logic gates

The shift to a distributed computing paradigm, in which multiple systems acquire and process data in real-time, presents challenges such as response time and bandwidth that must be addressed. Emerging high-performance CIM combines logic operations and data storage to significantly improve data processing efficiency and reduces power consumption.[17] However, conventional silicon CMOS-based static random-access memory (SRAM) cells suffer from complex circuit design increasing leakage power and low integration density due to the scaling limitation.[84, 85] Novel non-volatile memory technologies (e.g., 2D FeFET) that simultaneously perform logic operations and store the computational state are driving the miniaturization and simplicity of memory and computing component designs. This allows for the realization of high-integration artificial intelligence applications without CMOS-concerned static power dissipation. In addition, their robust remanent polarization and absence of depolarization effect offer a host of compelling advantages, including ultra-low power consumption, rapid write speeds, non-destructive readout, high endurance, and non-volatility, thus making 2D FeFET superior for next-generation non-volatile logic operation in emerging data-centric applications.

To simplify the circuit structure and improve the area and operational efficiency, multi-functional CIM units that can be customized on demand may be the ultimate pursuit so that logic and neural synaptic operations can be carried out simultaneously in a single multi-functional device. Luo et al. designed a 2D dual-gate FeFET as the basic unit for performing digital and analog CIM (Figure 10a), where unipolar MoS_2 and ambipolar $MoTe_2$ were employed as active channel materials.[21] Here, PVDF is used as the bottom and top ferroelectric layers. Based on the dual-ferroelectric coupling effect, the MoS_2 channel is in the low-resistance state only when both the bottom and top gates are under a positive voltage pulse (20 V) as shown in Figure 10b. For other voltage pulses, the channel usually shows high resistance behavior. Due to the ambipolar nature of $MoTe_2$, the channel exhibits a LRS when the dual-gate voltage pulses are both negative and/or both positive (Figure 10c). The truth table can be

constructed using two input states, IN1 and IN2 which represent the applied voltage pulses (±20 V) applied to the top and bottom gates of digits '1' and '0'. Two output states: low resistance and high resistance are defined as binary states '1' and '0' respectively. The input logic states (0, 0), (0, 1), (1, 0), (1, 1) will result in the output states '0', '0', '0', '1' in MoS_2 which corresponds to the AND logic behavior, and the output states '1', '0', '0', '1' in $MoTe_2$ corresponds to the XNOR logic behavior. The logic states are non-volatile and do not require additional static power consumption needed for CMOS technology. In CMOS-based memory technology, the implementation of the XNOR and AND logic functions require at least 11 and 5 transistors, respectively, highlighting the high area utilization of FeFET. [86] To further explore the potential of FeFET for applications in logic circuits, non-volatile logic half-adders, another important unit in logic circuits, were constructed using the heterojunction of MoS_2 and $MoTe_2$ FeFETs. The input waveforms A and B are shown in Figure 10d. In the logic half-adder, the additional globe input (common bottom gate) V_{in3}=A is added together with inputs (top gate) V_{in1} = B and V_{in2}= $\overline{B}$ are used for MoS_2 and $MoTe_2$ respectively. In the designed circuit, the MoS_2 FeFET is functioned as an AND logic gate to produce the Sum signal and the $MoTe_2$ FeFET is functioned as an XOR logic gate to generate the Carry value (Figure 10e). Figure 10e shows the output conduction states of the AND and XOR logic operations for different combinations of A and B pulses. Figure 10f is a truth table that clearly shows the function of the half-adder. In 2D FeFET, only two transistor structures are needed to achieve a non-volatile half-adder, eliminating the need for 16 transistors in conventional CMOS circuits.[86] In summary, the 2D FeFET offers significant advantages over conventional CMOS circuits in terms of non-volatility, circuit complexity, and power consumption.

5. 2D FeFET Photodetector

Photodetectors play essential roles in many fields and applications, such as imaging, satellite remote sensing, robot vision, autonomous driving, satellite remote sensing and security checking.[28, 87, 88] Photodetectors incorporating ferroelectric materials have recently attracted interest because of their scalability, self-terminated surfaces and low defect densities, which provides an additional degree of freedom to achieve more possibilities in optoelectronics application.[87] In addition, some 2D ferroelectrics are semiconductors with suitab band gaps, so that FeFET-like devices can be fabricated without additional semiconductor channel layers, thereby largely increasing device integration. Overall, these characteristics can improve light absorption and reduce photocarrier recombination, providing a pathway to higher photoelectric

conversion efficiency. In this section, we review the recent advancements in 2D FeFETs for photodetection applications.

5.1. Ferroelectric Band Engineering

Heterojunctions based on 2D vdW materials play an important role in high-speed, sensitive broadband photodetection due to the bandgap design and richness of 2D materials.[90] Three types of band alignments exist in 2D heterojunctions: straddling (type I), staggered (type II), and broken (type III), which can be employed to modulate bandgaps to realize multifunctional applications.[27, 91] However, only the tuning of the Fermi level by an electric field is insufficient to cause band offset. In FeFETs, the non-volatile remanent ferroelectric field is large enough to tune the band structure such that switching of band alignment can be attained to satisfy the optimal performance needed in photodetectors. Based on this, Wang et al. fabricated a heterojunction FeFET based on n-type MoS_2, p-type GeSe and PVDF ferroelectrics (Figure 11a) to investigate ferroelectric band engineering for high-performance photodetector.[27] Three series connection parts are contained: n-type FeFET, p-type FeFET, p-n junction FeFET (Figure 11b). The hysteresis transfer curve of GeSe/MoS_2 heterojunction is shown in Figure 11c. Figure 11d shows the bandgap of GeSe and MoS_2 and the bandgap offset of the conduction band and valence band are 0.1 eV and 0.2 eV, respectively. In the Fresh state, the GeSe/MoS_2 heterojunction formed a type II band structure. In the P_{up} state, hole accumulation in GeSe and electron depletion in MoS_2 lead to an upward band bending in GeSe. The drift current of minority carriers is restricted at both sides which suppresses the reverse current. In the P_{down} state, the reverse current is increased under a large bias which originates from Fowler-Nordheim tunneling. It indicates the presence of a triangle barrier that may be a result of the bandgap reduction in the P_{down} state. Generally, the electric field narrows the bandgap by moving the bottom of the conduction band while the top is nearly constant. So, the conduction band offset of GeSe changes from 0.1 eV to negative values, resulting in type I band alignment. After the effective band alignment tuning by the ferroelectric field, the optoelectronic performance is further investigated. As shown in Figure 11e, the heterojunction exhibits a sensitive optical response under visible light illumination with different incident power. In the P_{up} state, the type II band alignment not only benefits from separating photo-generated carriers to realize high-speed photoresponse but also acts to suppress the dark current. As a result, a 14 μs fast response accompanied by an extremely low dark current of 1.5 pA and a high detectivity of $4.7*10^{12}$ Jones in the visible light wavelengths is

realized. In commercial integrated photodetectors, the near-infrared photoresponse is an important index, especially within the communication band of 1300nm and 1550nm (E_g=0.8 eV).[92] However, due to the bandgap of MoS_2 (1.2 eV) and GeSe (1.1 eV), the application space of MoS_2/GeSe heterojunction is limited. The ferroelectric field narrows the bandgap according to the Stark effect and the MoS_2/GeSe FeFET is still sensitive to lower energy photons (Figure 11f). In the P_{up} state, the band alignment of GeSe changes from type II to type I, exhibiting stable photocurrent switch characteristics under 1500 nm illumination (Figure 11g). Therefore, ferroelectric band engineering broadens the range of photodetection and withholds its potential in the field of telecommunications.

5.2. Ferroelectric Driven High-sensitive Photodetector

In 2D photodetectors, the intrinsic high dark current leads to low optical switching ratios and responsivities, which greatly limits their practical application. [28, 87] Moreover, the application of V_g and V_{ds} are needed in order to maintain high sensitivity. Consequently, the application of V_g and V_d will induce a leakage current between gate / source and a large dark current in the channel which results in large power consumption as well as low sensitivity and detectivity. In 2D FeFET-based photodetectors, the channel carriers can be depleted by the remnant polarization field in ferroelectric layers to suppress dark current. The large localized electrostatic field (≈ 1 nm/V) provided by ferroelectric layers can keep the channel in a fully depleted state which significantly improves sensitivity and detectivity even at zero bias.[89]

Based on this, Wang et al. constructed a MoS_2-P(VDF-TrFE)-based FeFET for photodetection, in which a few layers of MoS_2 were used as the photosensitive semiconductor channel, and the residual polarization of P(VDF-TrFE) was used to suppress the dark current of the MoS_2 semiconductor channel (Figure 12a). The stable residual polarization of P(VDF-TrFE) can provide an ultra-high local electrostatic field in the semiconductor channel, which is larger than the electric field generated by conventional gate in the FET. Under such an ultra-high electrostatic field, the channel of the few-layer MoS_2 remains in a fully depleted state (Figure 12b). However, a large V_g (± 40V) is required to fully accumulate and deplete the channel carriers, scaling the thickness of the ferroelectric layer is a feasible method to reduce the operating voltage. The device has a light response of up to 2570AW^{-1} and a detection rate of 2.2×10^{12} Jones (Figure 12c). Moreover, the signals were stable even after 90,000 operation cycles, which demonstrates the excellent reliability of the 2D FeFET photodetector (Figure 12d).

5.3. Reconfigurable Ferroelectric 2D Photodetector

Devices based on p-n junctions are self-powered and exhibit fast photoresponse and high-gain photodetectors, which are crucial features of optoelectronics.[93] However, the tunable

construction of p-type and n-type modules in 2D materials is still challenging.[93] In FeFETs, 2D semiconductor carrier-type modulation can be achieved by non-volatile electrostatic fields at the interface. The use of carrier implantation through the ferroelectric field can achieve arbitrary n-p junction, p-n junction, and n-p-n junction. Figure 13a shows the defined doping regions achieved by the PFM-controlled ferroelectric field.[94] A conductive atomic force microscopy probe is used to polarize the covered ferroelectric polymers. The p-type doping originates from the accumulation of holes in the bipolar 2D channel to screen the P_{up} state and n-type doping occurs under the P_{down} state. Figure 13b shows a lateral p-n-p-n structure and the corresponding band diagram after ferroelectric patterning. Figure 13c shows the I_d-V_d curves of ferroelectric-patterned n-n, p-p, n-p, and p-n junctions. Under the illumination of 532 nm light, the as-fabricated p-n diode exhibits obvious self-driven photocurrent under zero bias (Figure 13d).[26] The open-circuit voltage (V_{oc}) of the ferroelectric p-n junction is 650 mV, which indicates efficient charge separation in devices enabled by the intense lateral built-in electric field across the p-n junction. A fast photoresponse within 20 μs was observed, which is about 6 orders of magnitude faster than the pristine device. Based on the p-n diode, a n-p-n bipolar phototransistor with large photocurrent amplification is constructed. The typical bipolar transistor contains 3 parts: emitter (E), base (B), collector (C) corresponding to ferroelectric doped n, p, n regions, respectively.[95] The working mechanism is shown in Figure 13e, with the equivalent circuit shown in Figure 13f. The formula for current amplification is $I_c=(1+\beta)I_{ph}$, where β is the gain factor that quantifies the performance of bipolar transistor.[26] Figure 13g shows the photodetection performance of a ferroelectric-patterned n-p-n transistor. Compared to conventional photodiodes, the photocurrent is remarkably improved along with a fast photoresponse under 532 nm laser illumination, which is consistent with the high-gain amplified photocurrent of bipolar transistor.[26] The ferroelectric-based n-p-n bipolar junction exhibits a large gain factor of 1,000 compared to photodiodes, which is superior to the buried gate-based bipolar transistor, lateral heterojunction.[96-98] Figure 13h summarizes the performance of photodetectors based on 2D FeFETs. It is evident that various types of 2D FeFET-based photodetectors, including p-n diodes and phototransistors, demonstrate high responsivity and fast response time.

6. Summary and Perspectives

The application space of 2D FeFETs spans a wide range of important domains marked by exciting breakthroughs. Leveraging on their unique layered structure, 2D materials hold the potential to be unaffected by short channel effects and to overcome scaling limitations

encountered in traditional Si-based transistors. This paves the way for the realization of an area-efficient transistor architecture that seemlessly integrates computation and memory, fostering operational efficiency. The pristine surface of 2D materials without dangling bonds presents a highly desirable platform for engineering trap-free interfaces, a factor critical in preventing memory performance degradation. Remarkably, the memory performance of 2D FeFET has approached or even surpassed mainstream memory technologies such as SRAM, DRAM, and flash in certain aspects as shown under Table 7. Together with their unique ferroelectric polarization mechanisms (such as sliding ferroelectricity and dipole-locking effect), 2D FeFETs are capable of operating at low voltage, achieving ultra-fast operating speed, and exhibit extremely low power consumption in CIM applications.

While 2D FeFETs offer significant advantages, they are not without their share of drawbacks and challenges in various aspects that necessitate further exploration. Firstly, the key challenge faced by 2D FeFETs is the consistent preparation of large-area single crystalline 2D materials. Although it is possible to grow multiple 2D materials into large-area single crystals, the prevention of defects, impurities, and grain boundaries during the growth process remains a complex task, which can significantly impact device performance. Secondly, the compatibility of 2D FeFET with CMOS technology requires further exploration. Thirdly, concerning 2D ferroelectric channels, challenges persist in growing natural oxide layers or forming seed layers of atomic layer deposition high-k oxides. Lastly, the stability of 2D ferroelectricity, particularly at the atomic level thickness, still demands extensive research efforts. This aspect holds significant importance for future scalability of these processes and technologies.

For future developments:

At the physics level, 2D ferroelectricity-like dipole-locking effect, interlayer charge transfer promotes the rapid development of 2D FeSm-FET. These advantages of 2D ferroelectrics thus overcome the challenges in ferroelectric dielectrics which include the inability for continuous scaling in vertical and planar dimensions for multifunctional applications. However, with such rapid development, the interaction between the 2D semiconductor and the ferroelectric dielectric as well as the mechanism of 2D ferroelectric semiconductor still lacks comprehensive understanding and requires further studies. Moreover, emerging new 2D ferroelectric mechanisms such as Moiré ferroelectricity (twisting a small angle of vdW materials forms a moiré ferroelectric with alternating polarization.), sliding ferroelectricity, and unconventional robust multiferroic coupling

(such as ferromagnet, ferroelectrics), may provide high-speed energy-saving data storage and efficient CIM. Moreover, emerging new 2D ferroelectric mechanisms such as Moiré ferroelectricity, sliding ferroelectricity, switchable metallic ferroelectricity and unconventional robust multiferroic coupling, may provide high-speed energy-saving data storage and efficient CIM strategies. For example, in sliding ferroelectricity, the interlayer barrier is much lower than the traditional ferroelectric barrier, which may benefit ultra-low energy consumption integrated memory computing systems. From the perspective of applications and novel functionalities 2D FeFET can be further leveraged on emerging areas like miniaturized spectrometers with a tunable van der Waals junction, quantum cascade lasers in the mid and far infrared and reconfigurable computing chips. At the materials and systems level, the remarkable strengths of 2D FeFET in dimensional scaling and high area-efficient integration exceed that of traditional FeFET, but experimental verification on a chip level is still lacking. The successful controllable synthesis of wafer-scale MoS_2 in recent years will promote the development of massively integrated 2D FeFETs.

Going ahead, as new aspects of 2D ferroelectric materials and physics continue to be discovered and insights gained, we expect to see device concepts being developed that take advantage of the unique or enhanced properties of 2D vdW FeFET. Moreover, in this data-centric information age, the flourishing of FeFETs is rapidly affirming itself as one of the most promising technologies for neuromorphic computing, to create new opportunities for next-generation nanoelectronics and optoelectronics.

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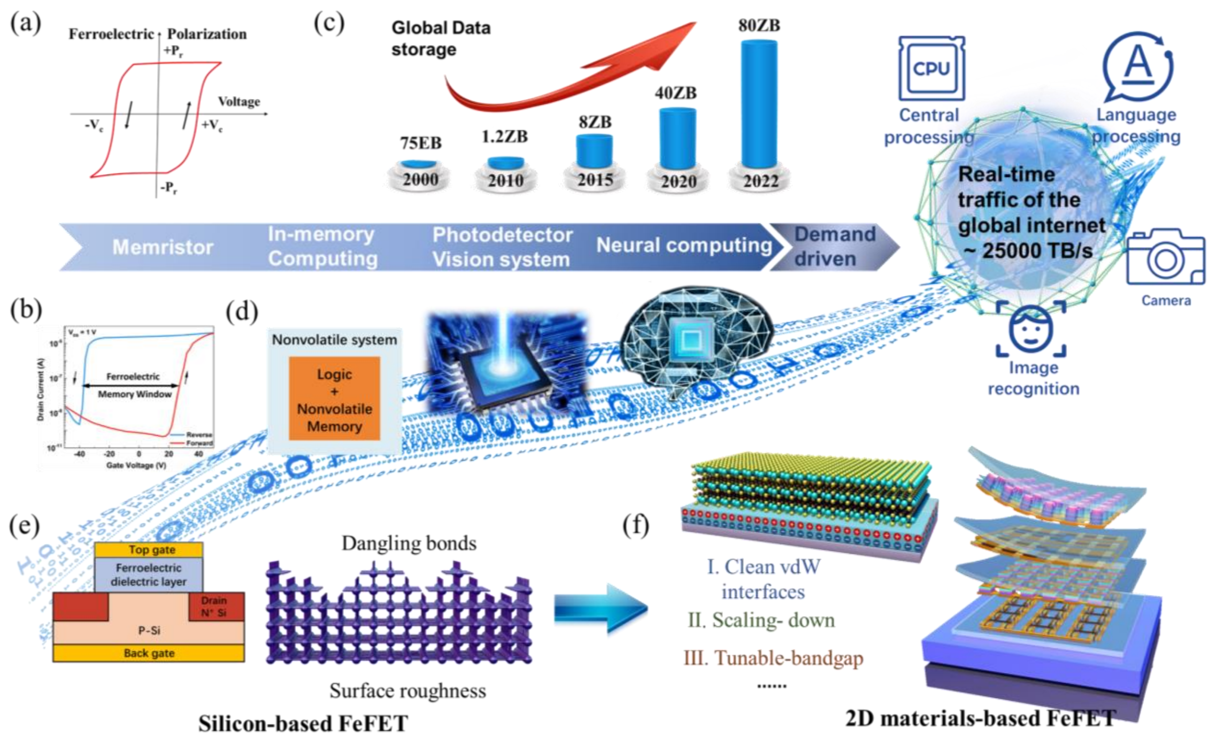

Figure 1. Schematic illustration of 2D FeFET. (a) Polarization-voltage hysteresis of a typical ferroelectric material. (b) Transfer characteristics of a representative 2D FeFET. Reproduced with permission.[5] Copyright 2021, American Chemical Society. (c) Global data storage from years of 2000 to 2022. (d) Emerging CIM with its computational paradigm and applications in image recognition, language processing etc., combined with nonvolatile system that combines logic modules and nonvolatile memory, find application in central processing. Additionally, emerging robotics technology, autonomous driving, and satellite remote sensing require highly sensitive, fast, broad-range vision systems, as well as photodetectors. (e) Conventional silicon-based FeFET. (f) 2D FeFET with vdW interaction.

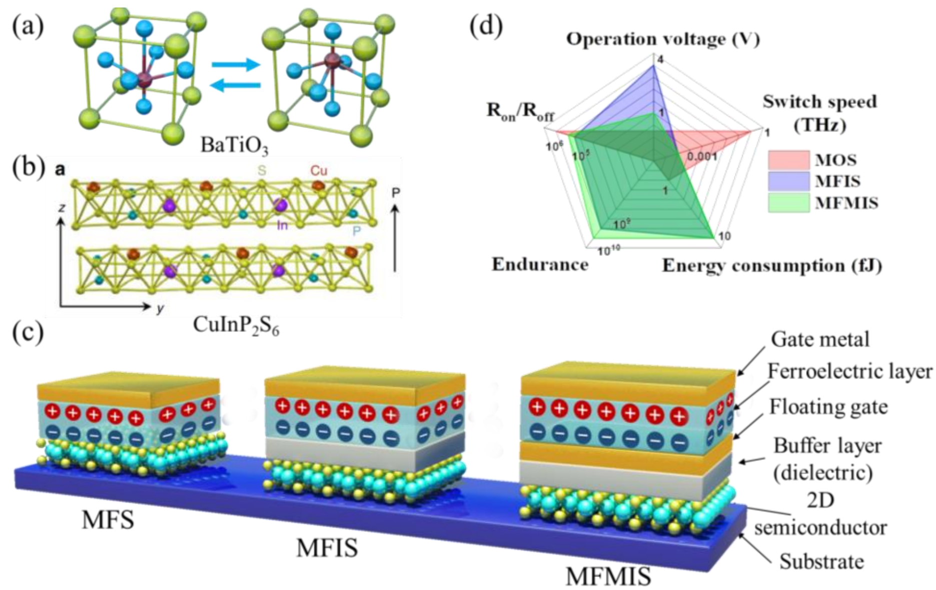

Figure 2. Combined 2D Semiconductor with Ferroelectric Dielectrics (a) Polarization switch in traditional ferroelectrics $BaTiO_3$. (b) Polarization switch in 2D vdW ferroelectrics CIPS. Reproduced with permission.[42] Copyright 2016, Springer Nature. (c) Structure evolution from MFS to MFIS to MFMIS which contains gate metal layer, ferroelectric layer, floating gate layer, dielectric buffer layer, 2D semiconductor layer and substrate. (d) Radar plot of key parameters comparison for 3 different device structures (MOS, MFIS, MFMIS).

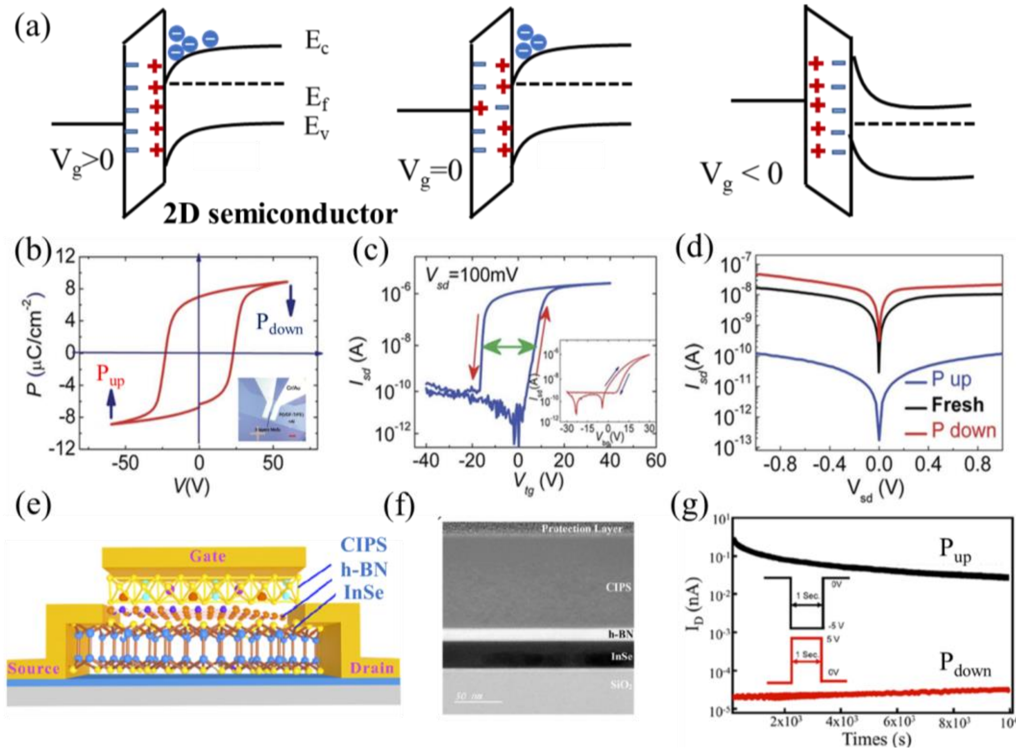

Figure 3. MF(I)S structure FeFET. (a) Schematic diagrams of energy band in positive, negative and zero-gate poling. (b) Polarization-voltage loop of 300nm PVDF film. (c) I_d-V_g transfer curve of MoS_2/PVDF heterojunction-based FeFET. The transfer characteristics of MoS_2 with SiO_2 back gate are shown in the inset. (d) I_d-V_d characteristics in fresh, P_{up} and P_{down} state. (e) Diagram of MFIS structure FeFET. Reproduced with permission.[25] Copyright 2015, WILEY - VCH Verlag GmbH & Co. KGaA, Weinheim. (f) Cross-section TEM image of CIPS/h-BN/InSe heterojunction layer stacking arrangement. (g) Source-drain current in P_{up} and P_{down} state with $\pm$ 5 V after 10^4 s circle. Reproduced with permission.[49] Copyright 2022, American Chemical Society.

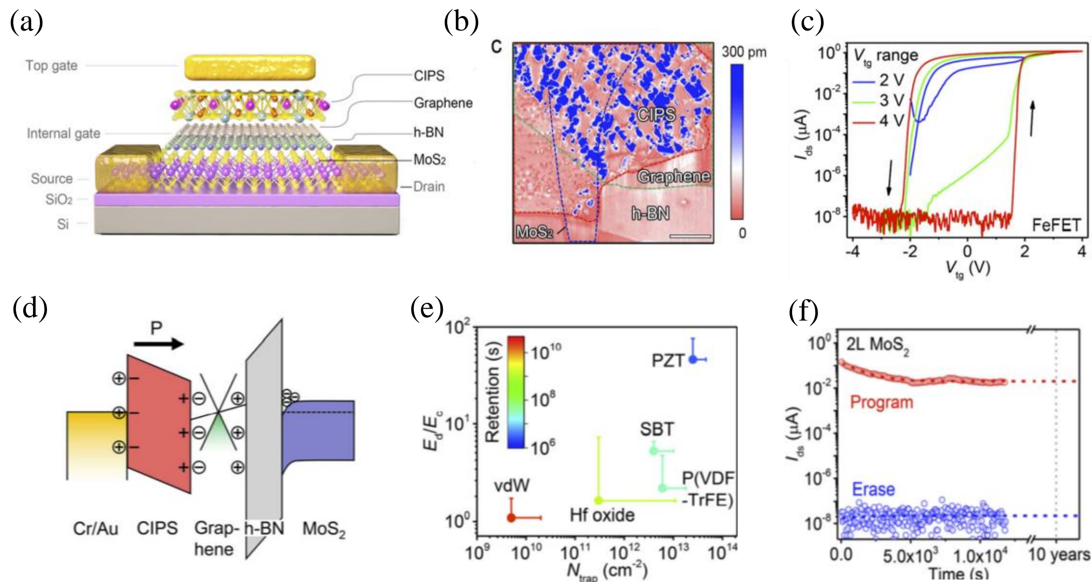

Figure 4. Two-dimensional vdW MFMIS structure FeFET. (a) Schematic diagram of CIPS/graphene/h-BN/MoS_2 vdW heterojunction FeFET. (b) PFM amplitude image of fabricated FeFET. (c) I_d-V_G transfer curve at various gate voltage range with V_d=0.5 V. (d) Band diagram and charge distribution of MFMIS structure FeFET with internal graphene floating gate. (e) Compared retention time vs E_d/E_c and N_{trap} concentration in vdW, Hf oxide, PTZ, P(VDF-TrFE). (f) Program and erase state after 10^4 s circle in 2L MoS_2 channel and extrapolated to 10 years memory retention time. Reproduced with permission.[23] Copyright 2021 Springer Nature.

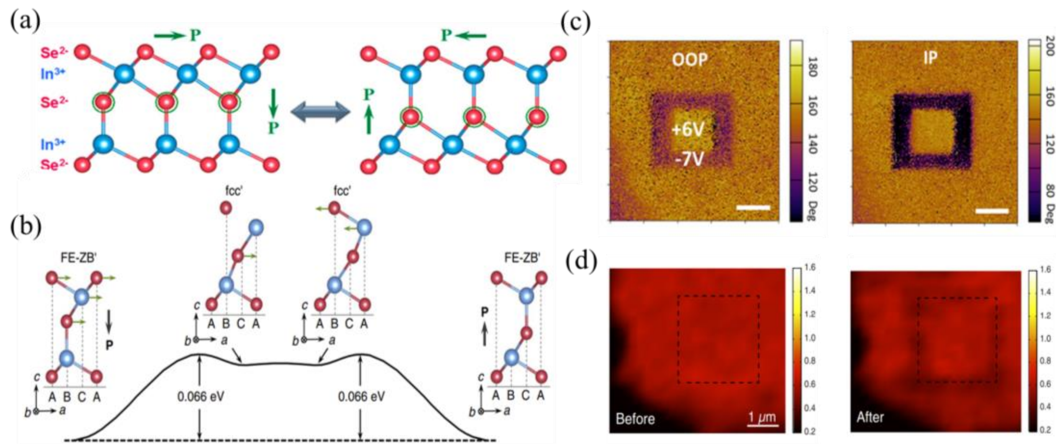

Figure 5. Ferroelectric polarization in 2D α-In_2Se_3. (a) schematic model of in-plane and out-of-plane switching coupling (b) Three-step kinetics pathways of polarization reversal processes in α-In_2Se_3. Reproduced with permission.[56] Copyright 2017 Springer Nature. (c) Out-of-plane and in-plane piezoelectric phase image of α-In_2Se_3. Reproduced with permission.[58] Copyright 2018, American Chemical Society (d) SHG intensity mapping of a trilayer α-In_2Se_3 before and after scanning with a negative biased AFM tip. The dashed line is the scanning area. Reproduced with permission.[31] Copyright 2018 American Physical Society.

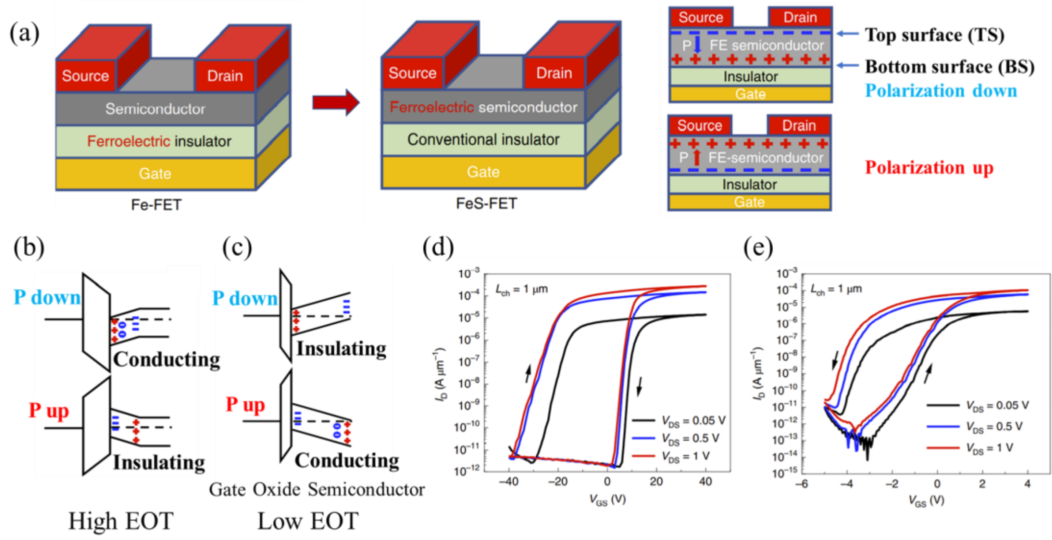

Figure 6. Ferroelectric semiconductor FET. (a) Schematic of Fe-FET and FeSm-FET. Polarization charge contribution in FeSm-FET in P_{up} state and P_{down} state. (b) Band diagram of FeSm-FET with high EOT in P_{up} state and P_{down} state. (c) Band diagram of FeSm-FET with low EOT in P_{up} state and P_{down} state. (d) Corresponding clockwise I_d-V_G transfer curve with high EOT. (e) Corresponding counterclockwise I_d-V_G transfer curve with low EOT. Reproduced with permission from.[34] Copyright 2019, Springer Nature.

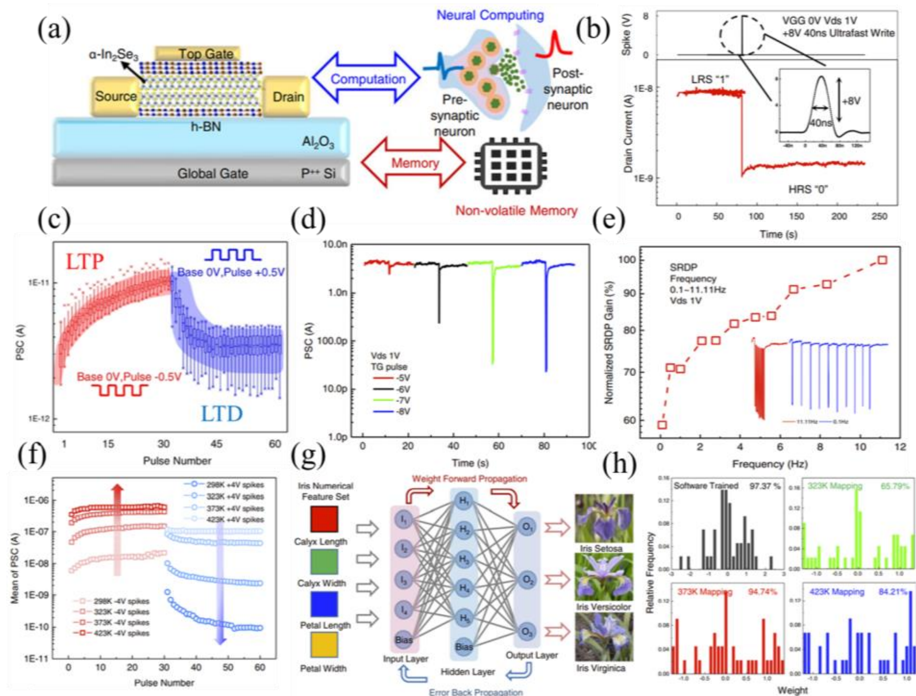

Figure 7. Neural computing based on 2D FeFET. (a) Fabricated α-In_2Se_3 based FeFET for neural computing and schematic diagram biological synapse. (b) Channel current switching from low-resistance-state to high-resistance-state under 40 ns spike writing and maintain stable for a long time. Confirms the ultrafast programmability of 2D FeFET. (c) LTP and LTD simulation in 2D FeFET with ± 0.5 voltage spike. (d) Incremental PSC amplitude under short negative spikes (-5V to -8V), corresponding to typical short-term plasticity simulation. (e) SRDP gains with different frequencies (0.1-11.11 HZ). (f) Temperature-dependent LTP and LTD simulation. (g) ANN for iris recognition and classification. (h) The weight and accuracy of simulated ANN contains software trained and thermal tuned. Reproduced with permission.[18] Copyright 2021, Springer Nature.

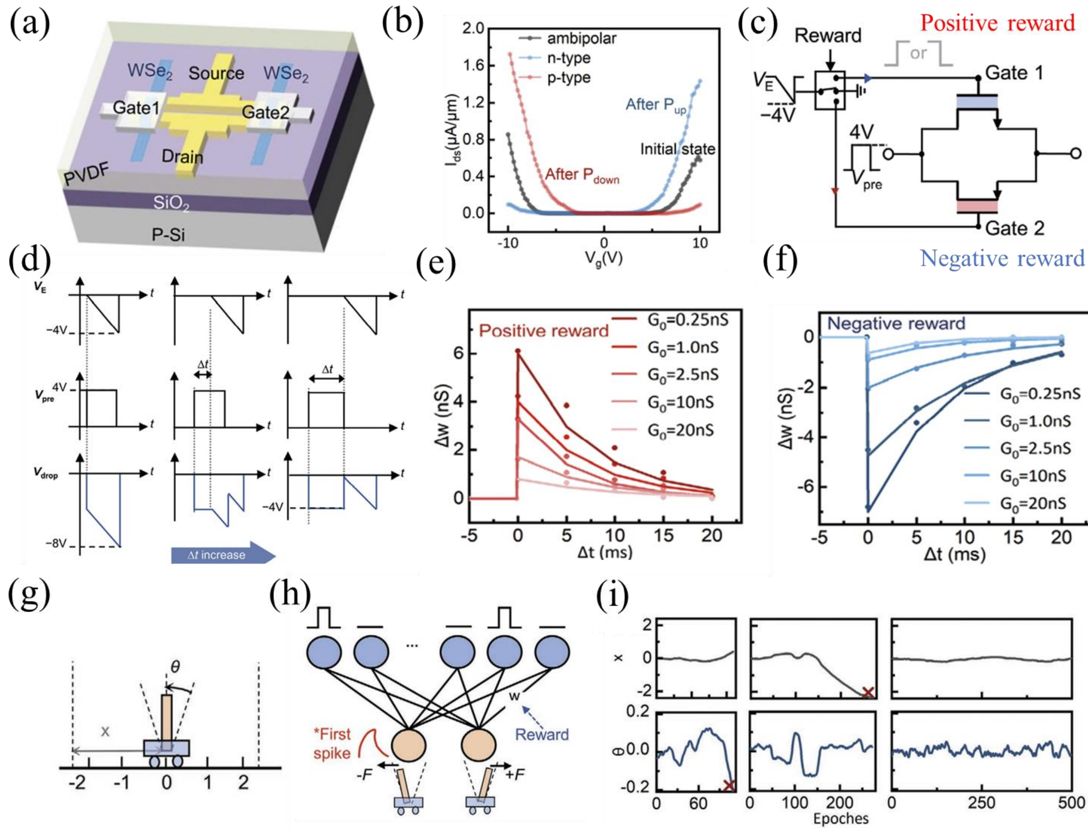

Figure 8. Machine learning based on SNN. (a) Schematic illustration of fabricated 2T synaptic cell structure based on bipolar WSe_2 FeFET. (b) I_d-V_g Transfer curve in different directions ferroelectric polarization. (c) Designed circuit diagram of 2T unit for realizing R-STDP. (d) Designed waveforms of preneuron signal V_{pre} and feedback signal V_e. (e, f) Measure weights in the coming positive reward and negative reward. Δt is the time difference of V_{pre} and V_e. (g) The standard control task: cart–pole problem. (h) Designed SNN to tackle the cart-pole problem including cart position, pole angle as input neurons and two forces (+F, -F) for balancing the cart as output neurons. (i) Time evolution of cart position and pole angle. The cart is successfully balanced after 500 rounds. Reproduced with permission.[20] Copyright 2022, WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

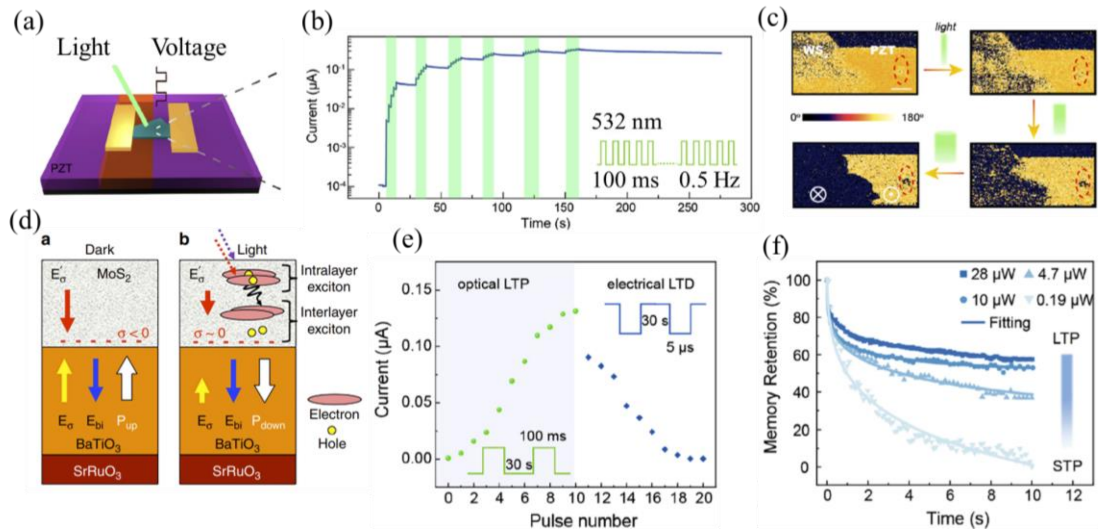

Figure 9. Artificial Optoelectronic Synapses. (a) WS_2/PZT heterojunction FeFET. (b) Channel conductance evolution after multi 532 nm light pulses. (c) PFM image of WS_2/PZT heterojunction and pure PZT with increasing light exposure time. (d) Mechanism of the photo-induced switching. Reproduced with permission.[78] Copyright 2018 Springer Nature. (e) Optical LTP and electric LTD in 2D FeFET. (f) Power-dependent memory retention proportion. High power light and low power light illumination are corresponding to LTP and short-term plasticity simulation respectively. Reprinted with permission.[24] Copyright 2019, American Chemical Society.

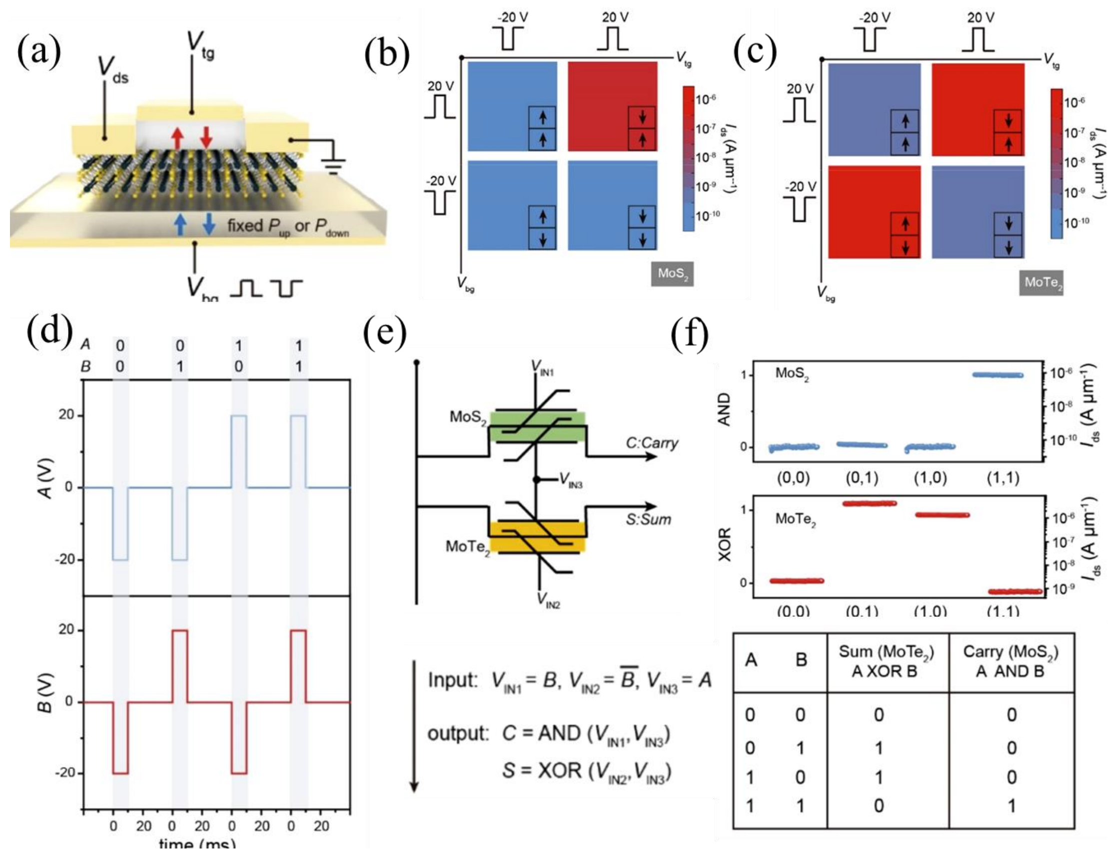

Figure 10. Non-volatile logic operation. (a) Schematic diagram Dual-gate FeFET for non-volatile logic operation. (b) Channel current of MoS_2 FeFET with different combinations of top and bottom polarization states. (c) Channel current of bipolar $MoTe_2$ FeFET with different combinations of top and bottom polarization states. (d) Input voltage waveforms. (e) Circuit diagram of half-adder based on $MoTe_2$ and MoS_2 FeFET. (f) Output states for AND, XNOR logic operations and truth-table for half-adder circuit. Reprinted with permission.[21] Copyright 2022 American Chemical Society.

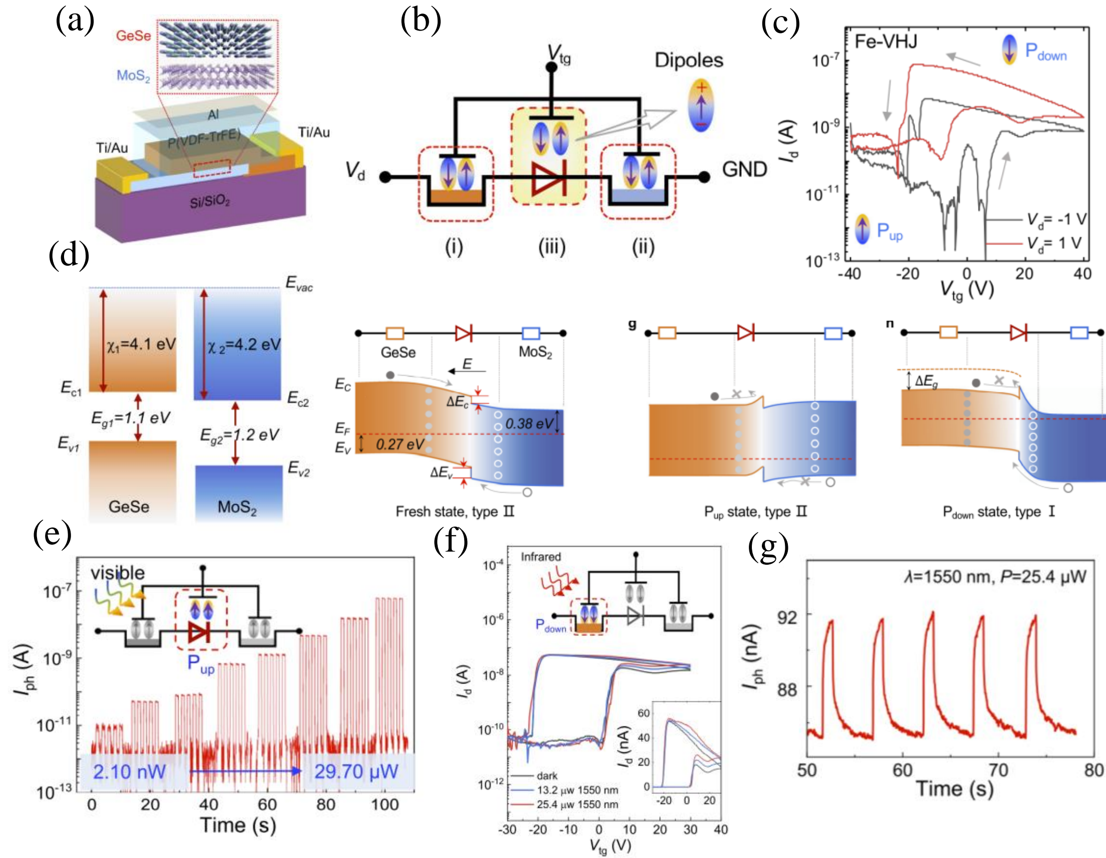

Figure 11. Ferroelectric band engineering. (a) Schematic diagram of GeSe/MoS_2/PVDF heterojunction FeFET. (b) Three parts electrical configuration of the device. (c) Counterclockwise I_d-V_g transfer curve of the heterojunction. (d) Energy band of GeSe and MoS_2 before contacted. The band structure of the heterojunction in the fresh state (type II), P_{up} state (type II) and P_{down} state (type I). (e) Photocurrent in P_{up} state under 520 nm illumination. (f) Transfer curve under the illumination of near-infrared light (1550nm). (g) Time-resolved photocurrent for 1550nm incident light. Reproduced with permission.[27] Copyright 2021 Springer Nature.

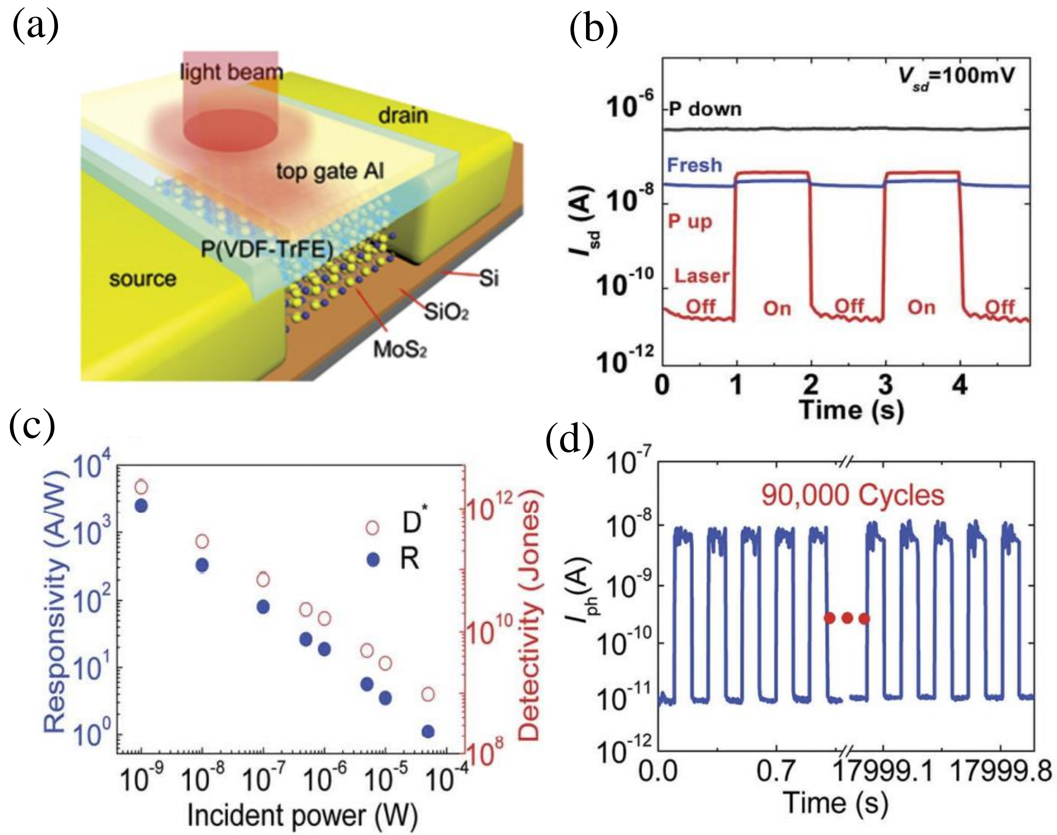

Figure 12. Ferroelectric driven high-sensitive photodetector. (a) Schematic diagram of MoS_2/PVDF heterojunctions FeFET. (b) Photo switch ON/OFF behaviors in P_{down}, P_{up}, fresh state. (c) Photo responsivity and detectivity as a function of incident power in Pup state. (d) Endurable photoresponse after 90000 cycles. Reproduced with permission.[25] Copyright 2015, WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

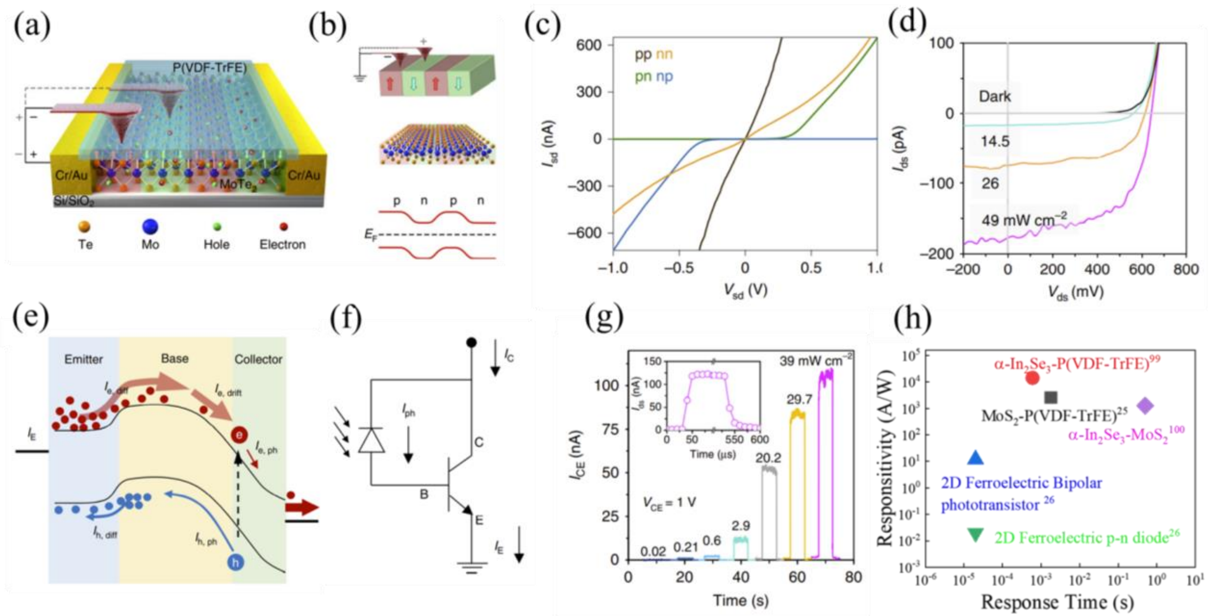

Figure 13. Ferroelectric reconfigurable 2D photodetector. (a) Schematic diagram ferroelectric patterned p-n-p-n junction probe-controlled ferroelectric domains in FeFET. Reproduced with permission.[94] Copyright 2020, Springer Nature. (b) Atomic arrangement and band diagram after ferroelectric patterning. (c) I_d-V_d for ferroelectric patterned p-p, n-n, p-n, n-p heterojunctions. (d) I_d-V_d of p-n junction under the illumination of 532nm laser. (e) Energy band diagram of the working mechanism of the n-p-n phototransistor. (f) Equivalent Circuit of the n-p-n phototransistor. (g) Photoresponse of the n-p-n transistor under various illumination power. (h) Benchmarks of 2D FeFET based photodetectors. Reproduced with permission.[105] Copyright 2019, Springer Nature.[26]

Tables

Standard logic/memory technology [1, 14, 37]	**Si-CMOS**	**SRAM**	**DRAM**	**Flash**	**2D FeFET** [14, 19, 35]
Operation voltage	0.7 V	0.7 V	0.45 V	< 12 V	1.5V
Subthreshold slope (mV/dec)	~62				< 60
Switch spead	0.4 THz	> 1 GHz	<100 MHz	> 10 MHz	0.1-1 GHz
Energy per switching	< 1 fJ	~ 1 fJ	~ 1 pJ	1fJ-100pJ	<10 fJ
Retention time		Volatile	Volatile	>10 years	> 10 years

Table1. Benchmarks of the standard logic/memory technology with 2D FeFET.

	Operation voltage	**Switch speed**	**Energy per switch**	**Endurance**
MFMIS-FeFET	1.5 V	0.1-1 GHz	1-10 fJ	> 10^{10}
Flash	< 12 V	> 10MHz	1fJ-100 pJ	~ 10^6

Table2. Benchmarks of MFMIS-FeFET and flash.

2D Ferroelectric Materials	**1T′-WTe_2**[3, 59]	**α-In_2Se_3**[3, 34, 60]	**$CuInP_2S_6$**[3, 42]
Band gap	~136 meV	~1.45 eV	~2.62 eV
Role in FeFET	Channel	Channel/Dielectric	Dielectric
Electrical properties	Metal/Semi-Metal	Semiconductor	Insulator
P (μCcm^{-2})	0.2	11.34	2.55
E_c(kVcm^{-1})	0.05	200	77
Sample synthesis	CVT/CVD/MBE	CVT/CVD/MBE	CVT
Structure in use	MFIS-FET	FeS-FET	MFIS/MFMIS-FET

Table 3. Benchmarks of 2D ferroelectric materials.

Structure	Ferroelectric	Channel	on/off	Endurance (cycles)	Retention time(s)	Switch speeds	Energy consumption (Joule)	Ref.
MFS	PVDF	$MoSe_2$	10^5	10^4	2000	50 us	-	[61]
MFIS	AlScN	MoS_2	10^6	10^4	10^5	<200 ns	-	[8]
MFIS	CIPS	In_2Se_3	10^4	1000	10^4	-	-	[49]
MFMIS	$H_{0.5}Z_{0.5}O_{2.0}$	MoS_2	10^5	$>10^{13}$	10 years	4.8 ns	22.7 fJ $bit^{-1}\mu m^{-2}$	[14]
MFMIS	CIPS	MoS_2	10^7	10^4	10 years	5 us	-	[23]
FeS	α-In_2Se_3		10^8	-	-	-	-	[34]
FeS	α-In_2Se_3		10^5	500	500	40 ns	234/40 fJ	[18]
FeS	α-In_2Se_3		-	-	-	-	3.6 fJ	[35]

Table 4. Summary of memory performance of 2D FeFET.

Structure	Neural network	Learning accuracy	Writing speed	Energy consumption	Reference
FeS-FET	ANN	94.74%	40 ns	234/40 fJ	[18]
FeS-FET	ANN	92.1%		~10 fJ	[35]
MFS	ANN	93.6		40 fJ	[72]
MFS	SNN		20 μs	32 pJ	[20]
MFIS	ANN	94.53%		<1 fJ	[71]
MFMIS	ANN	99.86	4.8 ns	22.7 fJ $bit^{-1}\mu m^{-2}$	[14]

Table 5. Benchmarks of neural computing based on 2D FeFET.

Structure	Neural network	Learning accuracy	Channel	Light Wavelength	Light pulse width	Energy consumption	Reference
MFIS	ANN	91%	MoS_2	450/532/650 nm	100 ms	1.8 pJ	[80]
MFIS	ANN	91%	ReS_2	405 nm	4 ms		[81]
MFMIS	ANN	~80%	Te	1550 nm	1 ms		[82]
FeS-FET	ANN	86.1%	α-In_2Se_3		200 ms		[83]

Table 6. Benchmarks of 2D FeFET-based optoelectronic Synapses.

Key parameters of 2D FeFET	Dimensional scaling	R_{on}/R_{off}	Maximum channel current	Retention Time	Endurance
	< 1 nm	> 10^8	>500 $\mu A \mu m^{-1}$	>10 years	> 10^{13}
Reference	14	34	34	14, 23	14
	Subthreshold swing	**Write voltage**	**Speed**	**Energy consumption**	**Linearity**
	< 60 mV dec^{-1}	<2 V	< 10 ns	<10 fJ	> 90%
Reference	19, 23	18, 19	14	35, 75	18, 35, 72

Table 7. Key parameters of 2D FeFET.

((**For Reviews and Perspectives,** please insert author biographies and photographs here for those authors who should be highlighted, max. 100 words each))

Author Photograph(s) ((40 mm broad, 50 mm high, color or grayscale))

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