Physical Verification for 3D Heterogeneous Integrated Electronic Photonic Integration designs using equation-based methods for Non-Manhattan structures

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Abstract

To effectively manage substantial data traffic in the data centre, the use of high-performance optical transceivers known as optical engines is essential. Optical engines are 3D integrated with Electronics and Photonics ICs employing advanced packaging will provide high performance in a compact form factor that can be fabricated at wafer-level. For such packages, there is an increasing demand to verify the process design rules in an automated way to prepare compliant mask layouts for reliable fabrication. More than 3X reduction on false violation is reduced by using Equation based rule methods on physical verification.

Introduction

Prominent software entities exert a significant influence and widespread usage across various public domains, such as social media, online shopping, and last-mile commute or delivery services. Software giants such as Facebook and Google require extensive data storage capacities to manage the vast volumes of information they handle. In 2011, the Open Compute Project Foundation [1] (OCP) was founded, aiming to leverage the advantages of open source and collaborative monolithic IC design development to drive innovation in networking equipment, general-purpose and GPU servers, storage devices, appliances, and scalable rack designs within and around data centers. The core elements responsible for managing data centre traffic include switches and optical couplers, which facilitate the conversion between optical and electrical data signals in both directions.

With each passing year, the intricacy and expenses associated with system-on-chip (SoC) designs continue to escalate. This trend has given rise to an expanding realm for 2.5D/3D System-in-Package (SiP) design. Although 2.5D/3D integration technology presents benefits for heterogeneous chiplet-driven systems, it concurrently introduces a more intricate design process, augmented by limited support from electronic design automation (EDA) tools. Chiplet based systems enable modularity, scalability and technology partitioning providing cost-effective solution. Unlike the traditional system-on-chip (SoC) design process, which has fully qualified design flow and verification methods embodied in the form of process design kits (PDKs) and automation scripts, chip design companies and assembly houses predominantly do not have heterogeneous integrated chiplet package co-design and sign-off verification process to help ensure that a heterogeneous chiplet based package will meet manufacturability and performance requirements. Recently advanced packaging technology such as Fan-out wafer level packaging (FOWLP) has been a choice for heterogeneous chiplets integration.

From 2018, for specific server application Open Domain Specific Accelerator (ODSA) [2] was initiated that works on Chiplets, phy interface and advanced packaging for Electronic Photonic Integration.

This study enables the physical validation of hybrid electronic-photonic packaging using Fan out wafer level packaging (FOWLP), a promising approach for developing a rapid Optical Engine (OE) compatible with High-Data-Volume Communications (HDC).

Architecture of Electronic Photonic Integration

For Co packaged Optical Engines [4] [5], apart from Photonic Integrated Chip (PIC), the package includes multiple Electronic Integrated chips (EICs) such as drivers for modulators and transimpedance amplifier that amplifies the signal. The package is specifically crafted to support the PIC, featuring optical edge couplers for seamless connection to external fibers through edge coupling.

FOWLP provides wafer-level heterogeneous integration of PIC and EIC in a compact form factor (Co-Packaged Optics) [6]. PICs are 2.5D integrated and embedded in Epoxy Molding Compound (EMC) with or without Laser diodes, while EICs are 3D integrated on top.

A Series of RDL layers establishes the connection between EIC and PIC. The PIC is linked via RDL and through the package via structure, extending through the mold to connect to the backside RDL and subsequently to C4 bumps that connect the package to the substrate.

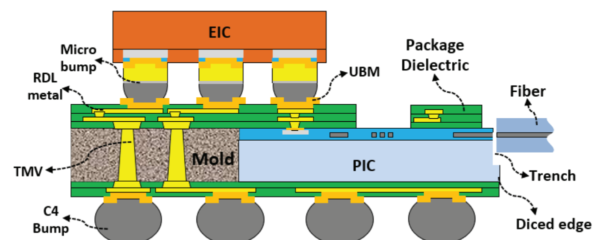

Fig. 1a. Schematic of a typical Electronic photonic integration using Fan out Wafer level Packaging (FOWLP)

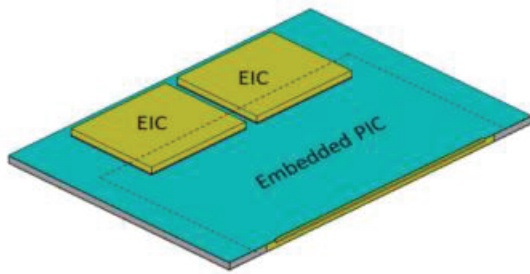

Fig. 1b. Floorplan of a typical Electronic Photonic package

Methodology

Electronic photonic heterogeneous integration presents chip-packaging level physical verification hurdles. The primary benefit of wafer-level packaging lies in its capacity to seamlessly integrate Optical Engine chiplets originating from various process nodes and diverse technologies, including but not limited to complementary metal-oxide-semiconductor (CMOS), silicon germanium (SiGe), and silicon on insulator (SOI).

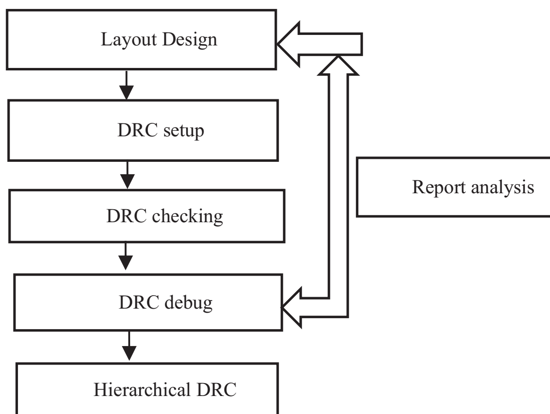

Fig. 2. Physical verification Design rule check flow

A. Design rule check method steps

As part of physical verification, Design rule check (DRC) involves area, density, width, spacing checks and so on. DRC checks are essential to ensure the design is compliant with certain rules before process fabrication.

In general DRC for advanced packaging (Figure 2) involves the steps below

• Design Setup: Understand system requirements for die placement and routing interconnect layers. Define package layers, substrate, components, and interconnections.

• DRC Setup: Design rule decks are prepared, defining the manufacturing constraints and guidelines from various process steps.

• Rules like Interconnect RDL internal dimensions and spacing between layers are defined for bump/pad placement, routing, via structures, etc...

• DRC Checking: The layout is subjected to DRC for vertical stacking and heterogeneous integration. Generate comprehensive reports detailing DRC results and violations using EDA tools.

• DRC Debugging: Designers' review and correct DRC violations by adjusting the layout, and iteratively refining the design until DRC errors are resolved.

B. Physical verification of packaging architecture

Design rules for this packaging architecture include but are not limited to

a) dimensions of these individual layers – Through package via, RDL on top, bottom side, EIC bump, package C4 bump, Deep trench related dimensions such as its width and length.
b) Layer-to-layer dimensions, such as spacing between through package vias and its spacing to adjacent package edge, spacing between bumps, spacing between adjacent ICs, distance between one layer edge to another etc.

In addition, there are also specific rules for positioning different components such as EICs, PICs, Laser diodes etc. and special structures such as cavities and deep trenches. Photonic IC is equipped with edge optical couplers or vertical optical couplers for optical IO that needs to follow certain definite design rules for its integration in this package platform and its proper functioning. DRC component of PDK coding helps in providing a report for designers to verify whether their physical layout design is in alignment with the process rules for fabrication.

Conventional designs exhibit structures that are rectangular, orthogonal, and adhere to the Manhattan layout style. Well-established advancements in one-dimensional design rule checking (DRC) have been tailored to scrutinize traditional integrated circuit designs resembling the Manhattan layout.

PICs packaging structure encompass geometries characterized by curvilinear, angular, and assorted non-Manhattan configurations. Upon converting designs from a continuous spatial representation to discrete layouts, significant instances of false errors emerge due to the gridding process applied to curvilinear geometries as shown in Figure 3.

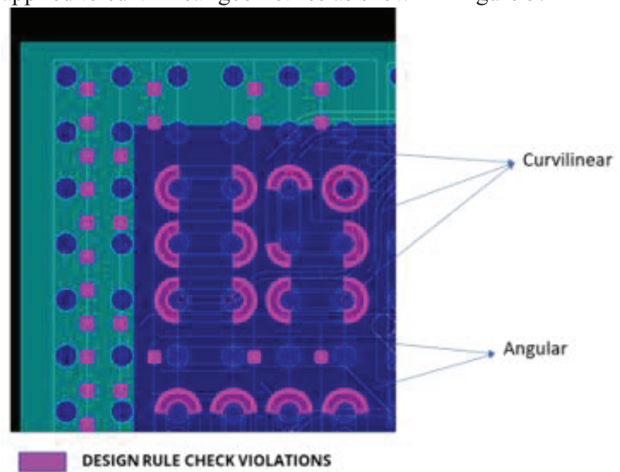

Fig. 3. Design rule violations for Non-Manhattan structures

Three prominent Electronic Design Automation tool providers, specifically Mentor Graphics, Cadence, and Synopsys, furnish options for conducting physical verification checks. Although most of these vendors supply conventional, monolithic integrated circuit-centric tools, a subset of their offerings encompasses tools centered around packaging and printed circuit board (PCB) design.

Tools oriented towards PCB or traditional packaging design conventionally rely on mil units, equivalent to one thousandth of an inch. When applied to expansive designs like the architecture detailed in this study, these tools encounter both hardware and software constraints.

C. Hierarchical chip level Physical verification

In advanced packaging, hierarchical DRC is performed when the design is partitioned into multiple levels, such as multiple dies on a single package. Electronic photonic heterogeneous Integration Packaging offers package frame and component frame. Component frame encloses Electronic or photonic IC.

Physical verification rules are available for layers like Waveguide RIB, Waveguide Grating Couplers, Waveguide Slab. Off grid, density, width of these layers and spacing of these set of layers and deep trench are the available rules. Rule validation shall be conducted on specific layers like Waveguide RIB, Waveguide Grating Couplers, Waveguide Slab for optical elements, as well as the implant layers of front-end devices. PICs are made of these layers and shall comprise distinct modules such as Modulators, Channel Waveguides, Grating Couplers, and Directional Couplers. The developed Hierarchical DRC can also be applied to chip level such as PIC as it involves non-Manhattan structures [3] in the design layout.

Results

When a Layout Design deviates from dimension rules, it results in violations being flagged during DRC checks. Narrow spacing between two shapes can lead to signal integrity problems, potential shorts, and undesirable performance characteristics. Grid-size denotes smallest incremental square unit from a central reference point in the horizontal and vertical space. Any measurement check between two lines should follow uniform multiples of grid-size in lateral and orthogonal space by DRC keywords. As shown in Figure 3,4 and 5, for curvilinear shapes, dimensions keep varying across the curve. Even for angular structures which are non-Manhattan, dimensions from lateral or orthogonal shapes keep on changing across the angular line. These variations on concentric arc, grating coupler like structures are unusual compared to the regular rectilinear or Manhattan structures. Traditionally physical verification constructs are keywords with reference to Manhattan or rectilinear type of structures. So, using these constructs on the curvilinear or angular non-Manhattan structures will induce higher number of false violations.

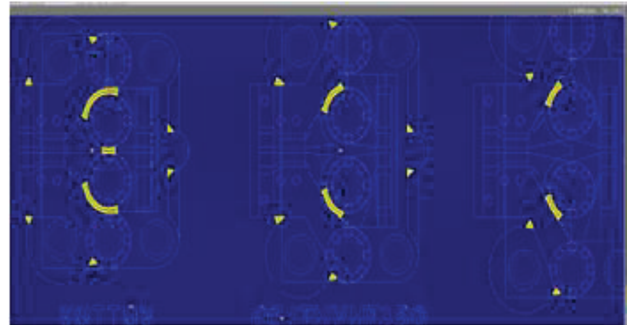

Fig. 4. Equation based method reduces false violations for curvilinear structures on packaging

Non-Manhattan, curvilinear shapes and skew edges are commonly encountered in Silicon Photonics design, even in traditional 2D fabrication. Equation-based Design Rules Checks are needed for non-Manhattan-based shapes. In addition, integration with special rules for Laser diode, Deep trench, and wire bonding on 2.5D shall induce additional false violations.

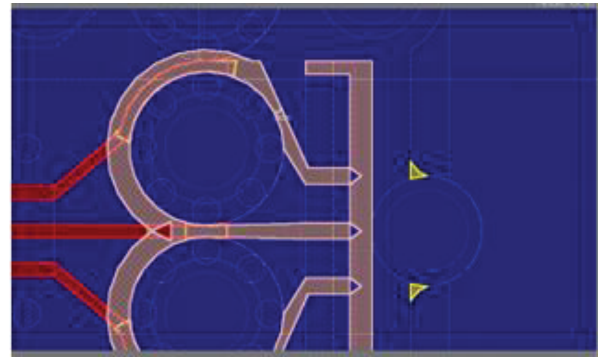

Fig. 5. Equation based method reduces false violations for region specific curvilinear and angular structures on packaging

The curvilinear spacing existing as a continuous arc between the two RDL lines has been partitioned into several smaller trapezoidal blocks, forming distinct segments. The spacing, measured in radians, is transformed into an angle representation based on (π) coordinates.

A minimum tolerance angle for RDL is established, and any violations occurring within this angle or spacing in radians are exempted.

By employing this approach, a significant number of erroneous linear violations that are angle-dependent are effectively disregarded.

In the case of a reference design, the count of curvilinear violations has been substantially diminished, decreasing from 264 to 63 which is more than 3x reduction shown in figure 7.

Polygon coordinates, width in linear dimensions and Count of the polygon are also reported part of results database.

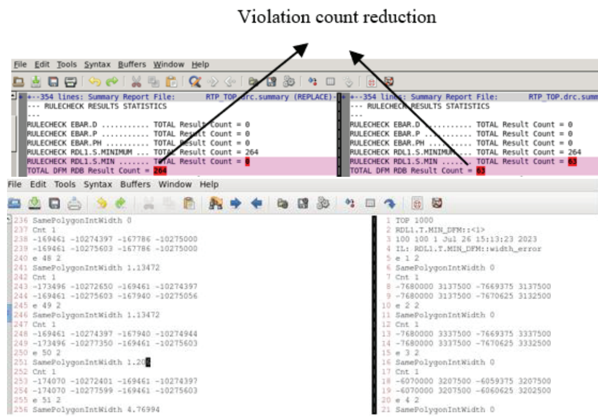

Fig. 6. Reduction of false violations for curvilinear structures on packaging using equation-based methods

Ensuring manufacturing process compatibility requires specific considerations when it comes to the layout of co packaged optics. The integration of 2.5D and 3D co-packaged optics necessitates the implementation of supplementary guidelines. Our methodology involves Equation based DRC and supplementary guidelines for 3D co packaged optics.

Designers are forced to manually waive an enormous number of false errors or non-checkable geometries, which is an error-prone process. Worse, the foundry can reject such designs for tapeout. Equation-based DRC shall capture or trace along the expected trajectory of the equation which shall be Non-Manhattan-like curvilinear or angular. Deviation from the expected trajectory will only flag false violations which will be a much-reduced count compared to using traditional DRC constructs.

Electronic photonic integration entails establishing guidelines and rules governing the positioning and arrangement of photonic elements, including lasers, photodiodes. These rules ensure precise positioning, alignment tolerances, and coupling efficiency to achieve optimal optical performance. DRC guidelines are necessary for designing and routing waveguides, which are essential for guiding and transmitting optical signals within the integrated package. These guidelines encompass waveguide width, bend radius, minimum feature sizes, and spacing requirements to maintain low-loss transmission and prevent signal degradation.

Hyper Lynx or 3D stacking technologies have been employed to validate the design within the PCB or packaging context. Traditionally, they have mil dimension units, a thousandth of an inch. For advanced packaging as FOWLP with micron feature size, IC level physical verification capability is required.

Conclusions

3D Integration of Electronic IC with Photonic IC offers cost advantages alongside compact form factor benefits over traditional 2D monolithic integration while providing good performance characteristics.

The utilization of design DRC coding using Electronic Design Automation tool enables designers to proactively validate the adherence of their physical layout design to process rules, significantly minimizing layout-related faults during reliability assessment and post-fabrication failure analysis.

In the case of monolithic designs, semiconductor foundries such as GlobalFoundries and AMF utilize equation-based design rule checks and Design for Manufacturability (DFM) keywords to automatically filter out false violations. However, in the realm of packaging, the practice of employing equation-based design rule checks is not as widespread.

In this work, 3X false violations are reduced using equation-based DRC methods for non-Manhattan structures with the layout of Co packaged optics.

Acknowledgments

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