Assembly process characterization of 3D Stacking of Heterogeneous Chiplets

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Abstract

The demands of advanced electronics products such as Automotive Radar and High functionality Smartphones have driven the growth of RF packaging market especially in radio frequency (RF) applications. Hence there is a need for RF devices with smaller form factors and higher speed operation. In this work, we have successfully demonstrated an assembly approach of CMOS and RF device chiplets stacked in a 3D configuration on a modified FOWLP platform. The chip-to-wafer bonding and different assembly processes will be discussed in the paper. The TSV measurement results and the daisy chain measurement results will also be updated.

Introduction

Radio frequency (RF) applications have driven the market for advanced electronics packaging over the past few years [1]. The RF packaging industry is anticipated to expand in products such as High-End Smartphones. Systems-in-Packages (SiPs), 3D through silicon vias (TSVs) and wafer-level packaging (WLP) are technologies where RF devices need to be compact and small at lower cost [2,3]. By the year 20251, the market for RF advanced packaging is expected to reach $34 billion. The use of 5G is expanding including telecom and automotive [4,5].

Many Front-End Modules (FEM) will be required to meet the growing demand for 5G wireless connectivity technology [6]. The limited space in the RF device must be used efficiently to allow for additional Front-End Modules (FEM) [7,8]. The 3D stacking of chiplets is an alternative approach to packaged chips [9]. However, the die pickup and transfer process for 50um thin small die 1.39x0.87mm to the bond head is a critical to achieve a robust chip to wafer attachment process and good assembly process yield. The selection of flux for chip to wafer attachment of the CMOS dies onto bottom RF device wafer also played an important role. In addition, void-free molding process is required to ensure the mold compound material has fully encapsulated the solder joint area under the die.

In this paper, we demonstrated a heterogeneous 3D stacked packaging of chiplets using FOWLP process with through silicon vias (TSVs). The die pickup and transfer process of the small thin die of 1.39x0.87x0.05mm is evaluated through different rubber tips, die pickup speed and die transfer speed to achieve no die breakage and good die transfer and no die tilt after bonding. In addition, a no-clean flux with long staging time and high tacky force is evaluated to understand the effect of staging time on the solder joint wettability and die tacking onto the RDL-wafer. The flux dipping process is also evaluated to ensure the solder bumps are dipped into sufficient flux with no flux bridging on the microbumps [6 to 9]. On the other hand, the effect of UBM dishing on the solder voids are also studied in the chip to wafer flip chip process for the small chiplet dies. Electrical measurements are done on the μ-bump chains and TSV via chains are designed in the package structure to allow for verification of the different connectivity and solder integrity at different layer. Molding is done on the assembled RDL-first wafer. CSAM is done to inspect the mold fill under the CMOS dies before the solderball attachment process. Finally, the wafer is singulated to a 1.56mm x 1.11mm package size and subjected to temperature cycle test and MSL L3 reliability test.

Test vehicle Description and Assembly Process Flow

There are 2 chiplets used in the test vehicle for this work. The first is a CMOS die (1.39mm x 0.87mm) and the other is a RF device die (1.56mm x 1.11mm). These chiplets are stacked in a 3D configuration as shown in Figure 1. The specifications of the chiplet package is shown in Table 1. The overall assembly process flow is shown in Figure 2. The RF device wafer front side has a single layer RDL layer with underbump metallization (UBM) for the C4 BGA ball connection. It is then bonded temporarily to a glass carrier face down using an adhesive material. The bottom side of the RF wafer is then backgrinded to specific thickness, followed by the TSV via last process. The TSV via etching is done on the silicon and followed by the low temperature liner oxide deposition. The oxide etching process is done on the bottom via to allow for connection to the Aluminium (Al) pad. The Ti-Cu seed layer is sputtered using the PVD process to ensure the TSV via sidewall and bottom is in contact with the Al pads. Electroplating process is carried out on the sidewall of the TSV to contact to the Aluminium pad and the RDL layer. A dielectric film is then laminated to fill up the remaining via space and via opening was built to connect bottom metal layers to top ubm structure. This sheet form of photosensitive dielectric layer was processed via series of lamination, lithography exposure and chemical developing. High temperature and pressure process conditions allowed to soften and squeeze the dielectric material to be filled up the TSV gap. Wafer will be sent for subsequent furnace high temperature curing process after via opening was developed. CuNiAu UBM layer was built at via opening to connect and bonded with solder ball. PVD Ti/Cu seed layer was deposited first, followed by photoresist patterning to create opening exposing Cu seed surface for UBM structure only. CuNiAu will be electro-plated on selected photoresist opening area to build UBM structure at desired height.

The attachment process of the CMOS dies onto the RDL-First wafer are done by flux dipping and followed by conveyor reflow process to form the solder interconnections. Then wafer

level molding process is carried out to encapsulate the CMOS dies at a mold thickness of 400um. The silicon carrier is then debonded from the device wafer and the molded wafer is then backgrind to ~180um thickness. Finally solderball attachment process is then done on the RF device front side using 200µm diameter SnAgCu SAC 305 solder balls.

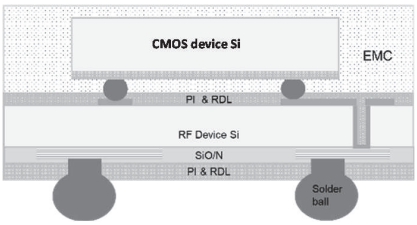


Fig 1: Schematic drawing of the 3D stacking of CMOS on RF device chiplets

Table 1: Specifications of 3D stacked chiplet package

Package specification	
Package size	1.56x1.11x0.28mm
Die size	1.39x0.87x0.05mm
Total number of IOs per package	6
BGA ball pitch	0.35mm

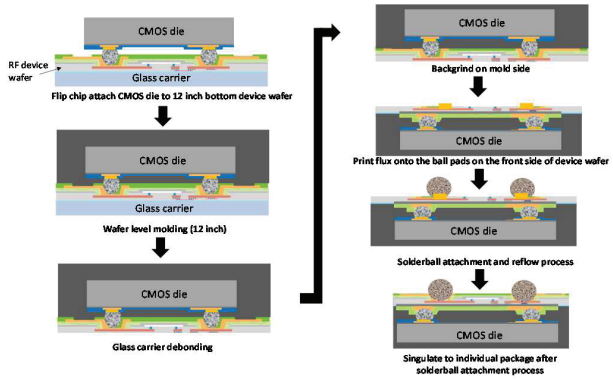


Fig 2: Overall assembly process flow

Evaluation approach

There are some considerations and evaluation approaches prior to the 3D stacked assembly of the small CMOS dies on the bottom RF device wafer. Flux and mold compound selection as well as UBM control dishing on RF wafer played a key role in the overall assembly process.

(a) UBM dishing on RF device wafer

The UBM structure is Cu/Ni/Au. Proper control and optimization on plating process minimizes the UBM dishing on the backside of the RF wafer is required to minimize solderjoint voids after the CMOS reflow attachment process.

(b) Flux selection

The flux selected is a long staging flux and more tacky flux taking into the consideration of the long processing time for the small CMOS dies onto the 12 inch wafer. No-clean flux is used compared water soluble type as the CMOS dies attached are very small and close to each other. The main advantage of using no-clean flux is to eliminate the need for post reflow flux residue cleaning process.

(c) CMOS assembly and reflow process

The study of the C2W bonding process for CMOS dies onto the RF device wafer is very critical to achieve good alignment bonding. Process evaluation on die pickup parameters and reflow process is important to ensure a robust and stable flip chip attachment process. There is also a need to have a high speed pick and place tool in a high volume manufacturing environment especially for higher throughput. This is due to the CMOS dies are very small and will require more time for a complete die placement on a 12 inch wafer. The assembly process yield is calculated terms of the number of dies tilt, number of missing dies and number of double dies for each wafer after the chip to wafer attachment and reflow process. The assembled wafer undergoes a lead-free reflow process to form the solder interconnection between the CMOS dies and the device wafer. Daisy chain measurements are measured to check the solder integrity and connection after reflow (Fig 3). Die shear is carried out to check the solder wetting of the CMOS die to the UBM on the bottom RF device wafer after the reflow process.

(d) Wafer level molding process

Wafer molding process is done on the device wafer to encapsulate the CMOS dies after flip chip attachment and reflow process. The selection of mold compound materials is crucial for the 3D stacked assembly process to ensure no mold voids is trapped between the CMOS die and the RF wafer during the wafer level molding process. The mold compound selected has a small filler size which allows for better mold flow during the molding process.

(e) Reliability test

The samples are attached with SnAgCu SAC305 solderballs and singulated to individual package before subjecting to MSL L3 and TC 500 cycles reliability test. Daisy chain measurements are taken at time zero and after the reliability tests.

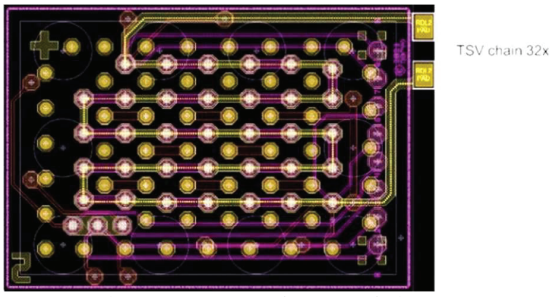


Fig 3a: Layout on the TSV chain structure

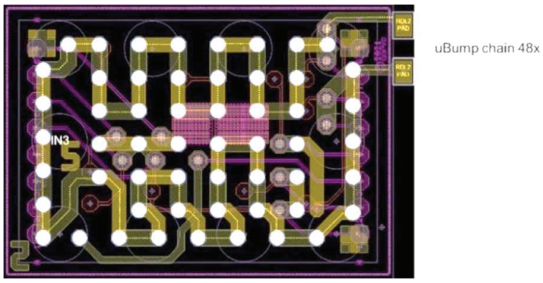
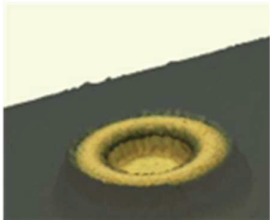


Fig 3b: Layout on the Micro-bump chain structure

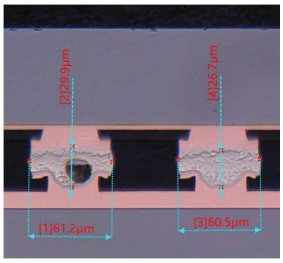
Results and Discussion

(a) UBM dishing on RF device wafer

The Cu layer thickness is increased using an electro-conformal plating from via contact on Al pad at the bottom of TSV to the sidewall of TSV and to the top surface on the bottom side of the RF device wafer.

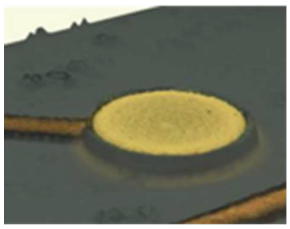


(a) UBM plating with more dishing

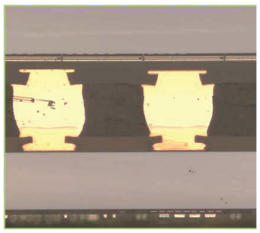


(b) Cross-section of CMOS die on bottom device wafer

Fig 4: Cross-section results on C2W bonding after reflow on UBM with higher dishing



(a) UBM plating with less dishing



(b) Cross-section of CMOS die on bottom device wafer

Fig 5: Cross-section results on C2W bonding after reflow on UBM with lower dishing

(b) Flux selection

Water-soluble fluxes have been used for a long time in flip-chip assembly and can be applied by dipping or spraying. However, the main disadvantage for using water-soluble flux is the need to remove the flux residues after post reflow process. In addition, its usage is slowly declining as the industry is slowly moving towards using no-clean flux. This is due to the industries moving to using Cu pillar microbumps instead of solder bumps. The solder bump pitch and solder standoff height are typically in the range of 40-60um for Cu pillar microbumps. The cleaning of the post reflow flux residues are extremely difficult at such low solder stand off height and fine pitch.

The flux selected in this work is a no-clean, long staging and more tacky flux from indium. This flux is a ultra-low flux residue type and has a staging time > 8hrs. The long staging time is required taking in the consideration for the long assembly duration time required for the small CMOS dies. A simple contact angle study is carried on this flux to understand the effects of different staging time on the contact angle and the solder spread wettability. Figure 6 shows the schematic diagram of the evaluation. The solderball used is SnAg which is the same as the microbump solder alloy in the CMOS die. The amount of flux dispensed is keep constant at ~ 0.4mm diameter (Figure 7). The sample is then subjected to Pb-free reflow profile in a conveyor reflow oven to melt the solderball with the flux. Contact angle measurement and the area of solder spread is measured after reflow. Figure 8 shows the optical image taken on the sample after reflow. Results showed that the contact angle ranging from 1 to 1.75° showing good solder wettability and minimum change in the contact angle and area of solder spread for staging time up to 14hrs (Figure 9).

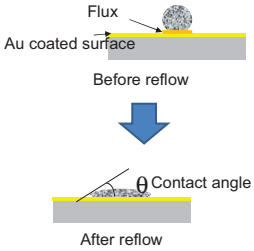


Fig 6: Schematic diagram on flux study evaluation

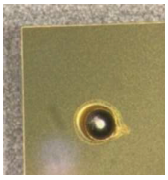


Fig 7: Optical image on sample with flux and solderball prepared before reflow

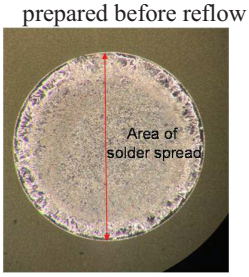
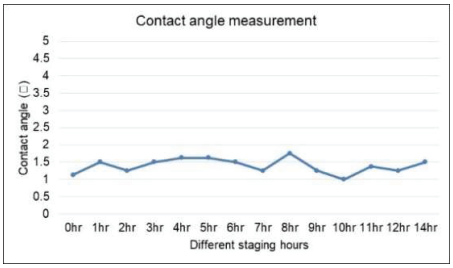
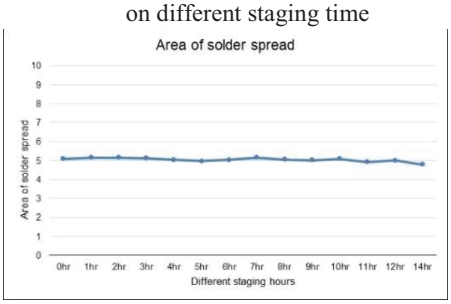


Fig 8: Optical image on sample after reflow



(a) Graph on contact angle measurement on different staging time



(b) Graph on area of spread on different staging time

Fig 9: Solder wettability study evaluation

(c) CMOS dies pickup and attachment process

The small CMOS dies pickup and attachment process involves the selection of a suitable rubber tip and different ejector pushup height. Two different ejector pushup height (i) 0.45mm and (ii) 0.65mm are used respectively to study the effect of ejector in the evaluation. Results showed that a rubber tip with sufficient vacuum slot and a lower ejector pushup height enables a more robust CMOS dies pickup and attachment process with > 90% assembly yield (Figure 10). The number of missing dies, die misaligned and double dies is greatly reduced as compared to using a higher ejector pushup height (Figure 11).

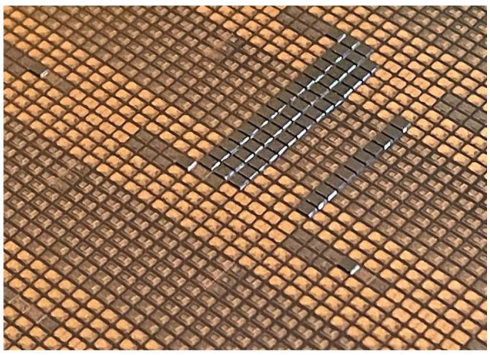


Fig 10: Good die attachment of the CMOS dies on the RF device wafer

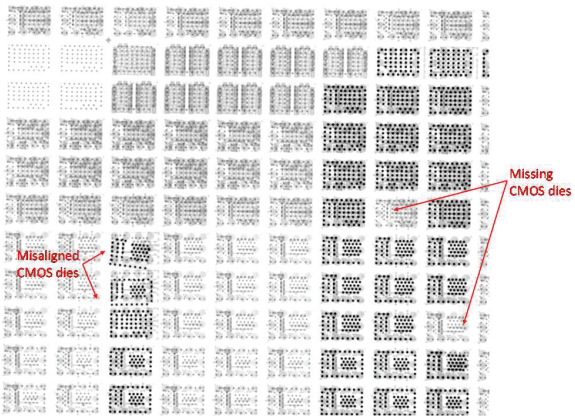


Fig 11: Xray images showing misaligned and missing CMOS dies after attachment

The flux dipping height is set at 10um flux height to ensure all the microbumps are coated with sufficient flux before attachment to the RF device wafer. The assembled wafer is then subjected to a lead-free reflow profile with peak temperature of ~ 255°C and dwell time above 221°C at about 55secs. Electrical connectivity measurement is used to check the continuity between the CMOS die and the bottom RF device wafer. There are 2 types of daisy chains structures designed in the 3D stacked chip structure. The structure includes the TSV daisy chains and the microbump daisy chains. Figure 12 shows the consistent electrical continuity results for both the TSV and microbump daisy chains. Die shear also showed good solder wetting of the CMOS die onto the bottom UBM of the RF device wafer with die shear failure mode at bulk solder (Figure 13).

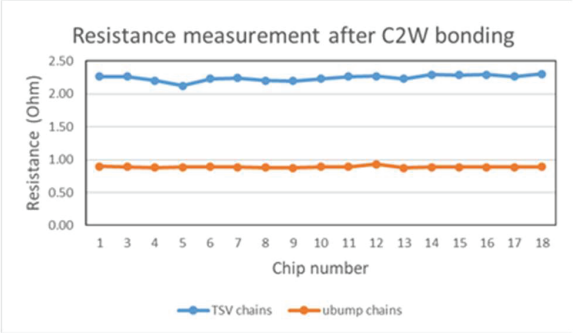


Fig 12: TSV chain and µ-bump chain resistance measurements after C2W and reflow

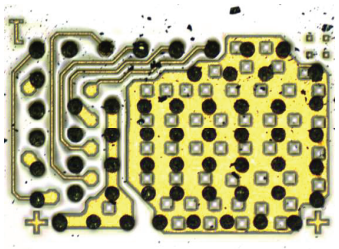


Fig 13: Optical image on die shear showing good solder wetting of the CMOS die to the bottom UBM on the device wafer

(d) Wafer level molding process

The wafer level molding is done using the compression molding process. During compression molding, the liquid or granular resin is put directly into the cavity. The wafer is loaded onto the top mold cavity followed by the mold closing with applied pressure and vacuum to remove any air or moisture from the mold compound. The mold compound will start to heat up and cure once the mold is fully closed. The selected liquid mold compound has an average filler size 8um and is suitable for the mold flow between the CMOS die and the bottom device wafer. Cross-section shows that good mold flow is observed with no mold voids between the CMOS die and the bottom of the RF device wafer (Figure 14)

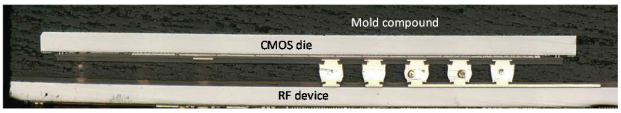


Fig 14: Cross-section showing no mold voids between CMOS die and RF device wafer

(e) Reliability Tests

The molded wafer subjected to backgrinding to thin down the wafer to ~ 180um before sending for laser debonding process to remove the glass carrier from the RF device wafer. SnAgCu SAC305 solderball attachment is done on the front side of the RF device wafer (Figure 15). The ball diameter used is 200um. A 2nd singulation is carried out on the diced reticle to dice the package to a size 1.56 x 1.11mm (Figure 16). CSAM and electrical measurements are done on the samples before and after MSL L3 and TC 500 cycles reliability tests to determine the connectivity of the TSV chains and the microbumps chains. Results showed that all samples passed the MSL L3 and TC 500

cycles test with no delamination and no electrical failures (Figure 17 and Figure 18).

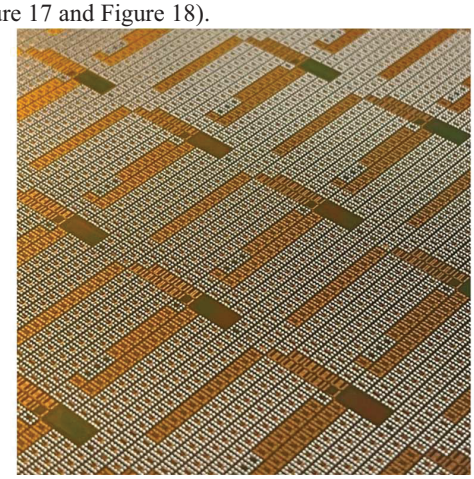


Fig 15: Optical image on the front side of the RF device wafer after solderball attachment process

Fig 16: Optical image on single sample after solderball attachment process

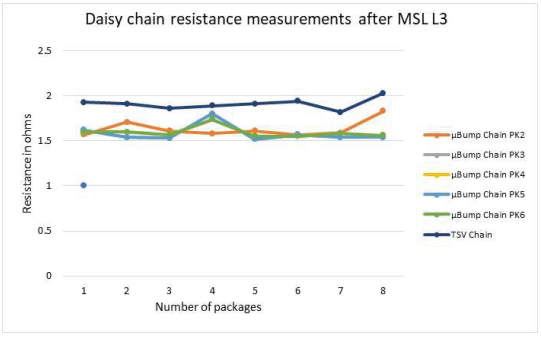


Fig 17: TSV and µ-bump chain resistance measurements after MSL L3 test

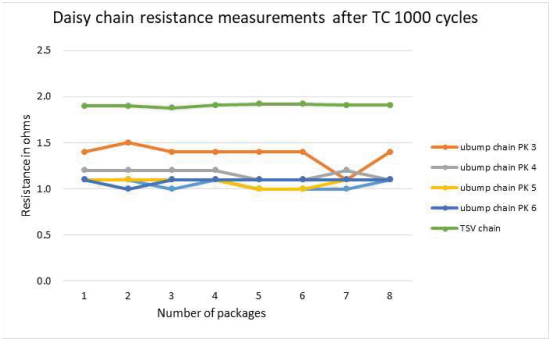


Fig 18: TSV and µ-bump chain resistance measurements after TC 1000 cycles test

Summary

This work demonstrated the feasibility of a 3D stacking of heterogenous (CMOS, RF device) chiplets assembly. Good solder interconnection is achieved with the Thru-Si RDL and solder bump on a modified FOWLP platform. Some of the findings are listed below:

A) Minimum solder voids are observed in the solder interconnections between the CMOS die and the RF device wafer with reduced UBM dishing.

B) The no-clean selected for chip to wafer attachment process showed good solder wettability and minimum change in the contact angle and area of solder spread for staging time up to 14hrs.

C) Good die bonding alignment of > 95% per wafer is also observed after attachment and reflow process.

D) Die shear after flip chip attach and reflow shows good solder wetting onto the bond pads of the bottom RDL wafer.

E) The mold wafer warpage is less than 2mm.

F) Good electrical connectivity is achieved on the µ-bump chains and TSV via chains. The packages also passed TC 1000 cycles and MSL L3 reflow reliability test.

This work will serve as a fundamental approach for FOWLP applications using small silicon CMOS, RF device chiplets assembly using Thru-Si RDl and solder bumps.

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