Ultrasonic Wavefront Computing Architecture on CMOS for Fourier Transform Computation

Y. S. Wang, K. T. C. Chai,
D. S. H. Chen, E. L. C. Wai, J. Sharma
*Institute of Microelectronics, Agency for Science, Technology and Research (A*STAR), Singapore*
wangys@ime.a-star.edu.sg

B. V. Phuong, C. E. Png
*Institute of High Performance Computing, Agency for Science, Technology and Research (A*STAR), Singapore*
A. Lal
Cornell University
NY, USA

***Abstract*—Fourier transform (FT) is an analytical algorithm that is ubiquitous with wide application uses from signal/image processing to solving differential equations. FT is most commonly computed using conventional computing resources which apply efficient variants like Cooley-Tukey's algorithm (FFT). Modern applications are demanding higher precision measurements, requiring heavier computation needs thus making conventional computing resources inept for the task. We are proposing a novel concept using wavefront computing based on the wave mechanics of acoustics to implement FT. Our proposed technique performs computation naturally via acoustic means in a "Fourier optics" like setup and is able to increase computation thru higher parallelism per area of hardware thus achieving higher computation speed. In this paper, we will present the design of our CMOS IC architecture for our ultrasonic wavefront computer which consists of transmitters and receivers for ultrasound in the GHz and signal processing.**

***Index Terms*—Acoustic lens, Piezoelectric, computing, wavefront, ultrasound, accelerator, digital phased-array**

I. Introduction

Fourier transform (FT) is a mathematical tool for the decomposition of functions into frequency components thus realizing essential functions in signal processing like filtering, modulation, and sampling of signal. FT is ubiquitous in applications that describe time (in communication systems, audio, and sensor signal processing) and space (real-time image classification [1]). Conventional hardware like multicore processors, GPU, FFT accelerators [2] and etc., employs architectures that are only achieving computation efficiencies of logarithmic linear, i.e. a 2D dataset of $N \times N$ needs $O(N^2 \log N)$ computations for decomposition. Alternative computing approaches based on wave mechanics in optical [3] and acoustic [4] domains can potentially achieve higher efficiencies with reduced complexity to $O(N_p)$ where N_p describes the propagation delays of N wavelengths of the carrier.

For a Fourier optical setup, the lack of a reliable phase modulation and retrieval method prevents a practical solution for the 2D FT problem, especially for space functions decomposition where complex values in the spatial domain are required for convolution operations in image enhancement, denoising, and feature extraction [5]. To overcome this issue, acoustic wave propagation can be used as both amplitude and phase modulation by using phase array implementation. In our proposal, we have implemented a digital ultrasonic phased-array on CMOS technology that can be operated at GHz frequencies thus allowing the wavefront computing module to be kept to $< 10cm^3$ volume. Based on our modeling work [6], we showed the potential impact of our ultrasonic wavefront computing engine being able to achieve magnitude improvement in speed and energy consumption for a large data set of more than 1k depth (i.e. N in $N \times N$, $> 1k$).

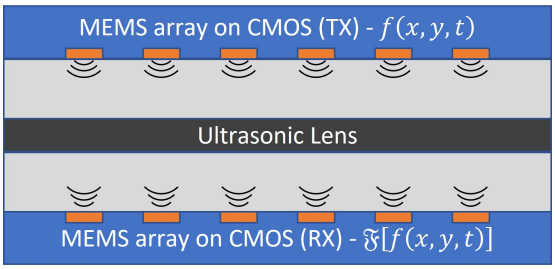


Fig. 1. Hardware architecture of Wavefront Computing Module.

In this paper, we are presenting the hardware architecture for implementing a GHz ultrasonic wavefront computing module on a conventional CMOS technology [7], [8]. Our computing module setup is similar to a Fourier optic system as illustrated in Fig. 1 using an ultrasound lens to focus an input-modulated ultrasound to the Fourier plane where the FT for the input data is derived naturally [9]. The ultrasound in our system is analogous to an RF carrier signal in a typical communication system hence, our CMOS IC resembles that of a radio IC with a transmitter (TX) and receiver (RX) chain. The key challenges for our system are: simultaneous, and synchronous GHz frequencies operation from an array, quadrature signal TX and RX, scalable pixel array, and fast signal acquisition.

We have built a pair of CMOS ICs (TX and RX) on a 0.18μm CMOS technology. The TX IC consists of a PLL, a digital controller, and an array 32×32 of synchronous digital phased array for generating quadrature-modulated ultrasound. The RX IC consists of a same-sized array of low-noise amplifiers with quadrature demodulation mixers, row-based baseband amplifiers anti-aliasing filters and ADCs, and digital controllers. Details of the architecture and components with sub-block measurements will be discussed in the following

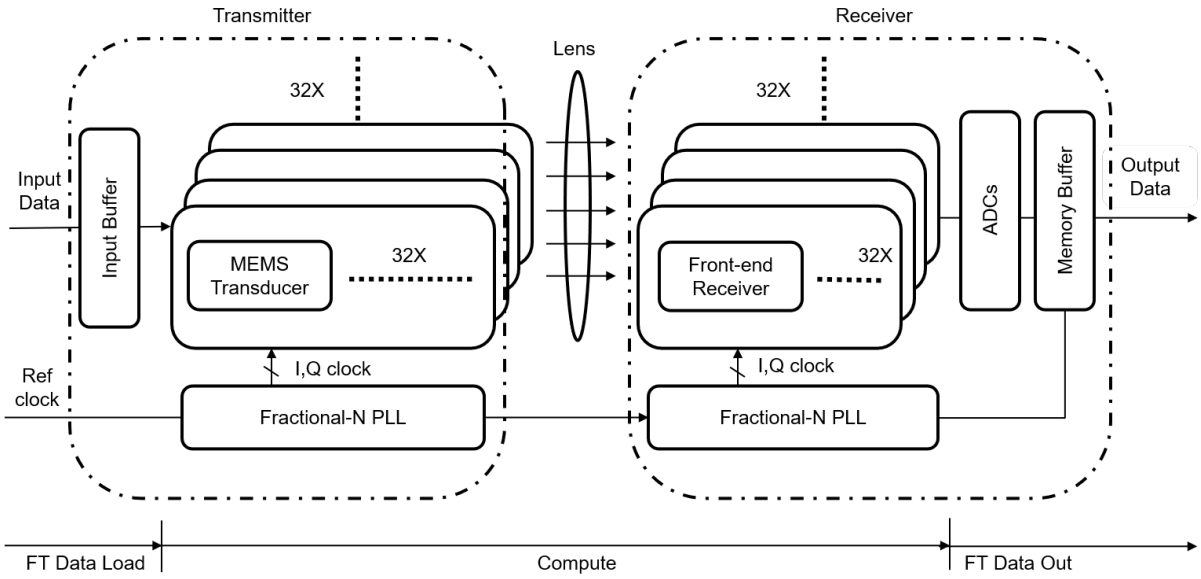


Fig. 2. CMOS IC architecture of our proposed ultrasonic wavefront computing module.

sections.

II. SYSTEM & CIRCUIT ARCHITECTURE

Fig. 2 shows the macro system of our CMOS IC. It is made up of two parts: the transmitter IC (TX) which performs input signal modulation and ultrasound driving; the receiver IC (RX) which receives that ultrasound and performs signal processing to recover the FT. A common reference clock source is provided to both TX and RX which has an internal Fractional-N PLL that generates the quadrature GHz clocks.

In TX, amplitude and phase modulation (quadrature) of the carrier signal in the GHz domain is implemented to allow complex-valued inputs. The process of quadrature modulation is quasi-digital using stored values and quadrature clocks to drive piezoelectric elements (ultrasound transducers) [10] as opposed to a fast digital stream modulating a quadrature clock. The advantage of such a driving scheme allows a fixed number of data path lines (determined by the depth of the data word of a single pixel) regardless of the size of the array. In essence, the quadrature modulation which enables complex words is achieved by both electrical driving and mechanical sizing [11].

In RX, the front-end (FE) receivers are arranged in an array that is configured to be size and pitch matched to the TX array. Ultrasound signals are sensed by piezoelectric elements which convert them to electrical signals. The FE receivers which are connected to the piezoelectric elements have a low-noise FE followed by a quadrature mixer for demodulation to recover the FT information. The RX chip employs a row-based baseband signal processing where each row of pixels shares a common baseband voltage gain amplifier (VGA), an anti-aliasing filter buffer, and an analog-to-digital converter (ADC). Data from the ADC is stored in a memory buffer for stream out.

A. Quadrature Clock & Fractional-N PLL

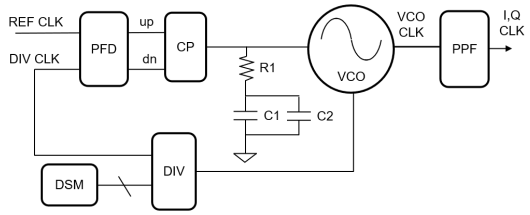


Fig. 3. Architecture of the quadrature clock generation with fractional-N PLL and polyphase filter.

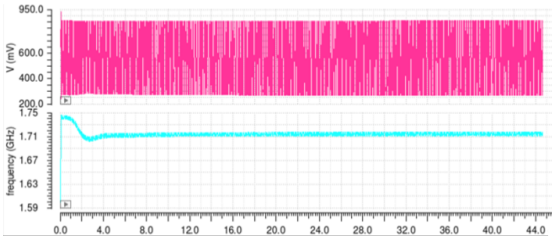


Fig. 4. Transient simulation result of the PLL showing the output clock (top) and the frequency (bottom) against time.

The timing source is critical for the accuracy of the system as it affects the resolution achievable for quadrature modulation/demodulation, the digital conversion of the data, and the strength of signal propagation as the efficiency of the piezoelectric transducer is dependent on its resonant frequency. We have implemented a Fractional-N architecture for our clock generation. Fractional-N can generate a fractional value from the reference clock thus, is suited for our system needs. Fig. 3 shows the fractional-N phase locked loop (PLL) architecture which consists of a voltage-controlled oscillator (VCO), a

phase-frequency detector (PFD), a charge pump (CP), a divider (DIV), a delta-sigma modulator (DSM), a loop filter, and a polyphase filter (PPF). The external reference is a 25MHz crystal for low noise and high stability. The local oscillator is an LC-tuned VCO with programmable varactors that allows frequency tuning across a wide range 1-2GHz at a resolution down to 50Hz. The high fractional frequency divisions are achieved with the high bit-orders DSM which generates an accumulated word that controls the fractional division factor in DIV. This allows the VCO output to be set to the desired output frequency at fine resolution spacings. The polyphase filter takes the VCO output and generates the quadrature phases of the output clock. To limit the quantization noise in the system, the loop bandwidth was set to $100kHz$ and the equation for the loop bandwidth, f_{LBW} can be derived as follows:

$$2\pi f_{LBW} = I_{cp} R_1 K_{VCO} \frac{C_1}{C_1 + C_2} \times \frac{1}{N} \quad (1)$$

where I_{CP} is the charge pump current, K_{VCO} is the VCO gain that represents the frequency sensitivity to voltage control, R_1, C_1, and C_2 are the parameters of the loop filter, and N is the fractional division of VCO frequency with respect to the reference clock frequency. The passives R_1, C_1, and C_2 are fixed in our system hence, we designed our charge pump current to be variable to account for process variations in order to maintain f_{LBW} within specification.

Fig.4 shows the simulation of the transient result. For our design, we used an external 25MHz reference and a 21-bit DSM word, and the PLL output frequency becomes $25 \times 10^6 \times (N + \frac{DSM_{in}}{2^21})$, where DSM_{in} is an input digital word and N is an integer division factor. The PLL takes about $40\mu s$ to lock to the desired frequency.

B. RX front-end receiver

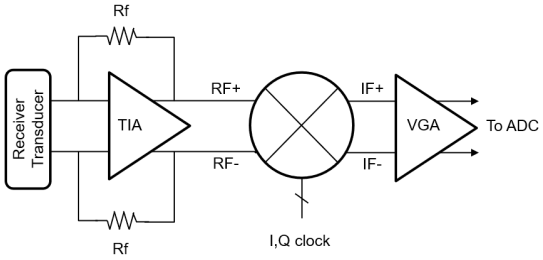


Fig. 5. RX front-end receiver.

Fig.5 shows the RX front-end receiver consists of a piezoelectric MEMS, a transimpedance amplifier (TIA), a quadrature active mixer, and a variable gain amplifier (VGA). The piezoelectric MEMS senses the ultrasound and converts it into an electrical signal which is received by the TIA. The TIA presents a low-impedance interface to the piezoelectric MEMS, isolating it from the input to the quadrature mixer. The TIA is also a low-noise interface with a transimpedance conversion gain that is defined by Rf which converts the input current to a voltage output.

The TIA output contains the analog and phase information from the Fourier transformation and recovery is achieved by demodulation using the quadrature active mixer. The mixer is a three-port system with RF input at F_{rf} frequency, quadrature IQ clock at F_{clock} frequency, and IF output at F_{if} frequency. The resultant F_{if} is demodulated to baseband $F_{if} = |F_{rf} - F_{clock}|$. To improve the signal quality, the VGA provides additional gains and filtering to remove high-frequency noise (tones from the mixer) before the signal is digitalized by the row-based ADC in the next stage.

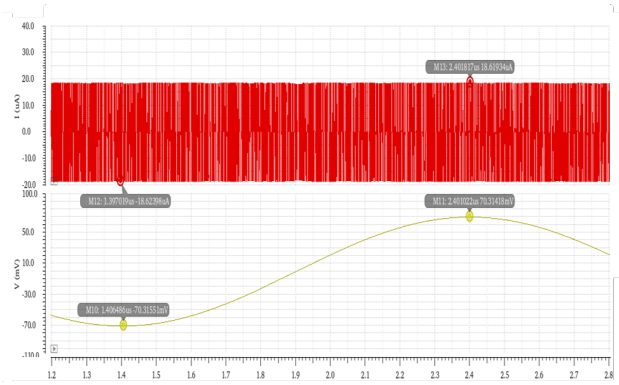


Fig. 6. Simulated results of the RX front-end showing a differential input current of $117.3\mu A$ V_{PP} (top) and the corresponding differential output voltage of $445.2mV$ V_{PP} at the output of the RX chain.

In Fig. 6, the quadrature mixer demodulates the input 1.252GHz RF signal to a 500KHz IF signal (baseband) for the VGA. The overall gain from TIA to VGA is set at 71.5dB as shown in Fig. 6.

C. Analog-to-Digital Converter(ADC)

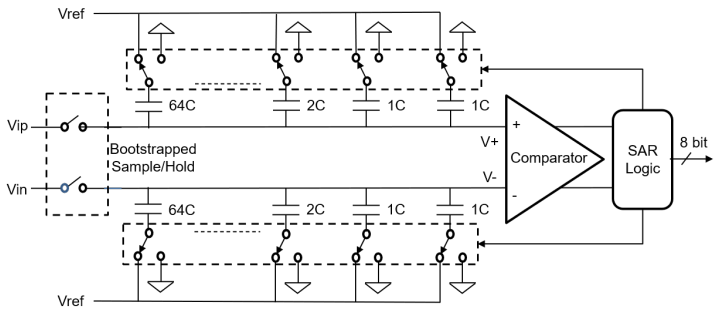


Fig. 7. Differential SAR ADC architecture.

The RX chip used row-based ADC for digital conversions and each ADC is based on a differential SAR ADC architecture as shown in Fig.7. The fully differential architecture suppresses substrate and supply noises and provides good common-mode noise rejection. Our SAR ADC uses a binary-weighted capacitor array and consists of a comparator, bootstrapped sample-and-hold (S/H) circuits, and successive approximation registers. The SAR logic is asynchronous hence

only a lower frequency (sample rate) clock is needed for digital conversion.

III. Measurement Results

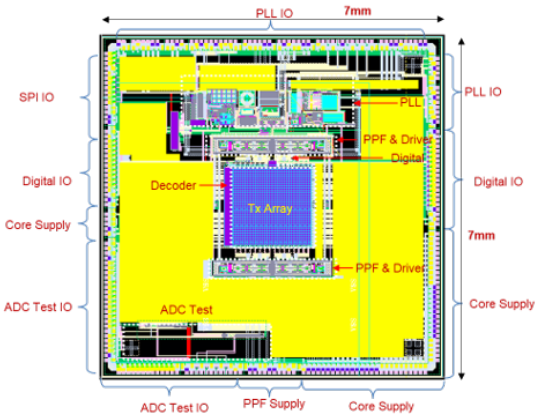


Fig. 8. Micrograph of the TX CMOS IC.

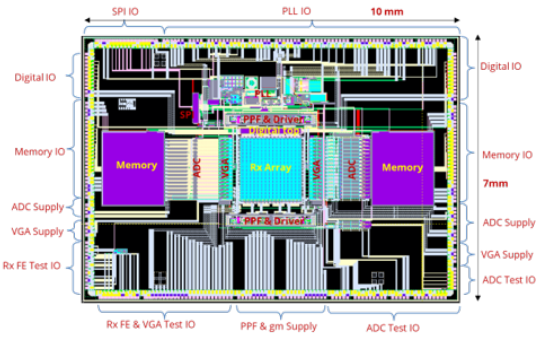


Fig. 9. Micrograph of the RX CMOS IC.

A pair of CMOS ICs (TX and RX) was fabricated on a 0.18μm CMOS technology. Fig. 8 and Fig. 9 show the TX and RX CMOS IC micrographs respectively. The electrical characterization of the PLL, the RX front-end, and the SAR ADC was performed and the results are shown as follows.

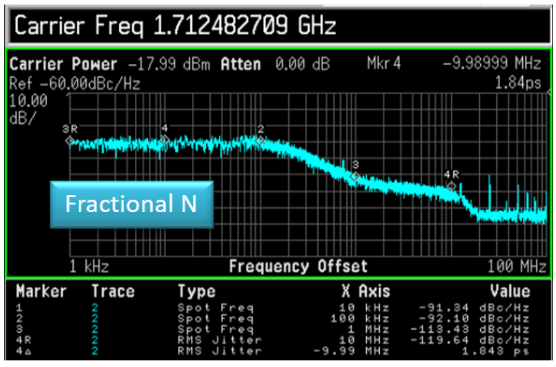
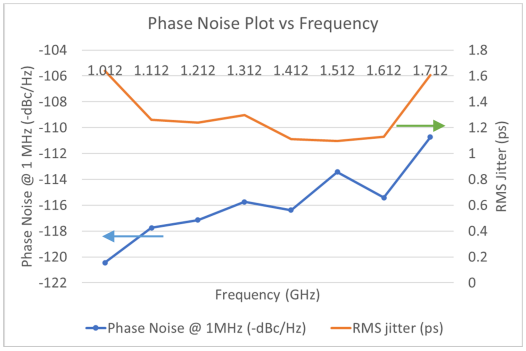


Fig. 10. Phase noise measurement of the Fractional-N PLL.

Fig. 10 shows the measured phase noise of the fractional-N PLL. The phase noise measured at 1MHz offset is -113dBc/Hz for fractional-N and this number improves for the interger-N setting (-126dBc/Hz) due to the additional noise contribution from the fractional-N division. Fig.11 shows the PLL's output set at values that range from $1012MHz$ to $1712MHz$. The rms jitter is <0.2ps and the phase noise is ≈10dB across this range. The tuning resolution measured is ≈50Hz using the 3 LSBs input from the DSM output control word. The PLL consumes 7.67mW from a 1.8V measured at an output of 1.712GHz.



Spot phase noise @ 1 MHz varies 10dB between (1-1.7GHz) less than 0.2ps variation on jitter

Fig. 11. The measured result of PLL: output frequency tuning range.

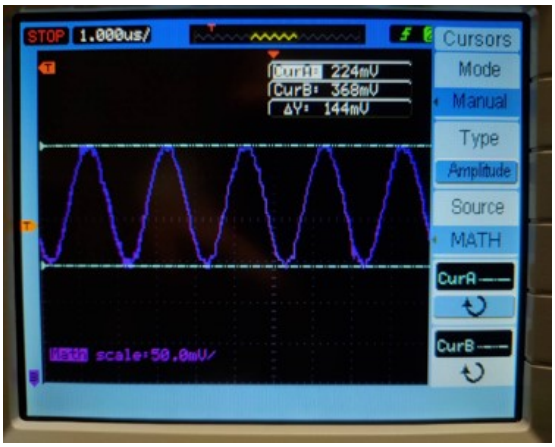


Fig. 12. Measurement of the RX front-end showing the differential output waveform from a 117.3μA differential input current.

Fig. 12 shows the measured result of the RX front-end chain without a MEMS transducer. From Fig. 12, the measured conversion gain is only 61.7dB (144mV output, 117.3μA input) as opposed to the designed 71dB. The RX front-end input is to be connected directly to the MEMS transducer and was not designed to be 50Ω matching hence the electrical testing incurred attenuation.

Measurement of the SAR ADC is shown in Fig. 13. For measuring the ADC, a differential input transient of $1.6V_{ppk}$ @ 195kHz was used. The SAR ADC was sampled using a 25MHz clock at 25% duty-cycle with 25% for sampling and 75% for holding (comparison). The output spectrum of ADC

is shown in Fig. 13. The measured SNR, SINAD, SFDR, and ENOB are 31.42dB, 30.2dB, 37dB, and 4.7 respectively. The lower-than-expected ENOB is suspected to be caused by the low bandwidth voltage reference used in our test setup. The measured DNL (Average cycles) is $\leq$1LSBs shown in Fig.14. and the measured INL (Average cycles) is $\leq$2LSBs across limited code 10–255. The higher errors for INL are caused by sampling switches in our design.

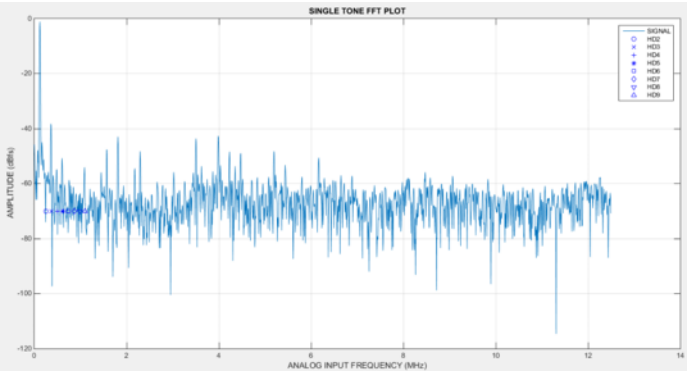


Fig. 13. Output spectrum from the SAR ADC measurements.

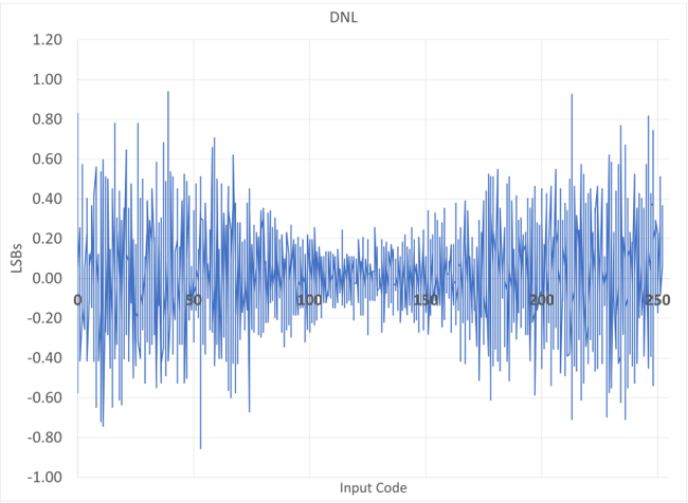


Fig. 14. Measured DNL (Average cycles) of the ADC to $\leq$ 1LSBs.

IV. Summary

We have proposed a hardware architecture for implementing a GHz ultrasonic wavefront computing (WFC) module on a conventional CMOS technology. The ultrasonic WFC module was designed to compute Fourier transform using the principles of wave mechanics and would be able to achieve speed limited to only the speed of wave propagation. A prototype module consisting of a pair of transmission and receiver CMOS ICs has been fabricated on a 0.18μm technology and measurements have been conducted at the sub-blocks PLL, RX front-end, and ADC. The PLL has a tunable range of 1-2GHz and has a phase noise of -113dBc/Hz at 1MHz offset with an RMS jitter of 0.2ps and a tunable resolution of 50Hz.

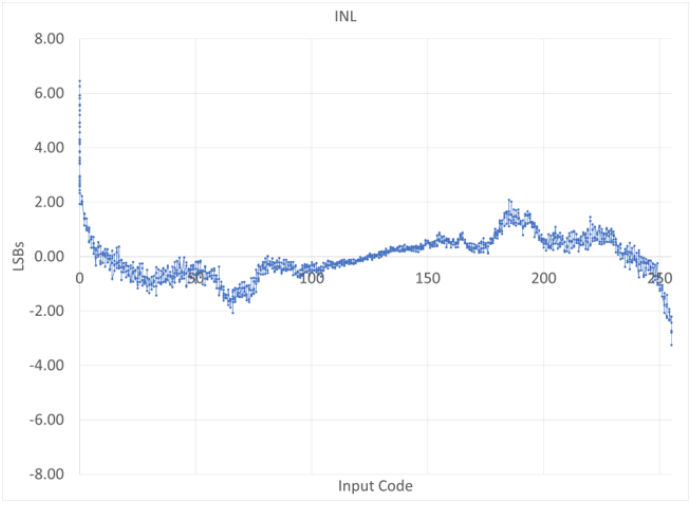


Fig. 15. Measured INL (Average cycles) of the ADC to $\leq$ 2LSBs across limited code 10–255.

The RX front-end with an LNA, a quadrature mixer, and a baseband VGA has achieved a measured gain of 61.7dB when tested with a 1.25GHz input-modulated carrier. The ADC was measured at 25MS/s with an SNR of 31.42dB. The next stage of the testing will be conducted with the CMOS ICs integrated as a single module with MEMS transducers to perform the Fourier transform computation.

Acknowledgements

This research was supported by A*STAR under RIE2020 grant (Grant No. A19E8b0102).

References

[1] L. Jiao and J. Zhao, "A survey on the new generation of deep learning in image processing," IEEE Access, vol. 7, pp. 172231-172263, 2019.
[2] J. Chen and et. al., "Hardware Efficient Mixed Radix-25/16/9 FFT for LTE Systems," IEEE Trans. on VLSI syst., vol. 23, pp. 221-229, Feb. 2015.
[3] S. Perrin and P. Montgomery, "Fourier optics: basic concepts," arXiv:1802.07161 [physics.gen-ph], 2018.
[4] Y. Liu and et. al., "Optical Measurement of Ultrasonic Fourier Transforms," IEEE International Ultrasonics Symposium (IUS), 2018.
[5] L. Yu and et. al., "Complex-Valued Full Convolutional Neural Network for SAR Target Classification," IEEE Geosci. Remote Sens. Lett., vol. 17, pp. 1752 - 1756, Oct. 2020.
[6] D. A. Patel and et. al., "SonicFFT: A system architecture for ultrasonic-based FFT acceleration," ASP-DAC 2022: 345-351
[7] K. H. Teng and et. al., "An On-Chip 2-D DFT Accelerator Ultrasonic Wavefront for Convolutional Neural Networks," 2021 IEEE (APS/URSI), 2021
[8] D. S. H. Chen and et. al., "A Study of Bonding Materials for GHz Ultrasonic Wavefront Computing," IEEE IUS, 2022
[9] Z. F. Yang and et. al., "Wavefront Computing in Solids: The Design Parameters and the Ideal Lens," 2021 IEEE (APS/URSI), 2021
[10] Z. F. Yang and et. al., "Effect of Tapered Angle on BAW Transducer Performance for Ultrasonic Wavefront Computing," IEEE IUS 2022
[11] M. Abdelmejeed and et. al., "GHz Ultrasonic Digital to Analog Converter for Wavefront Signal Processing," IEEE IUS 2018