Thermal Characterization of Both Bare Die and Overmolded 2.5-D Packages on Through Silicon Interposers

Heng Yun Zhang, Xiao Wu Zhang, B. L. Lau, Sharon Lim, Liang Ding, and M. B. Yu

***Abstract*— The next generation of heterogeneous integration requires 2.5-D packages on through silicon interposer (TSI) as enabling technology for less signal delay, faster speed, and more functionality. In the meantime, the introduction of multiple chips on interposer tends to increase the heat density with added interconnect complexity, which requires systematic thermal analysis and characterization. In this paper, thermal characterization of 2.5-D packages on TSI is reported in both bare-die package and overmolded package formats. The test vehicle consists of two dummy chips and thermal test die assembled on the same interposer of 18 mm × 18 mm × 0.1 mm through the flip chip bumping and joining process. A thermal test chip of 5.08 mm × 5.08 mm is built in with heaters and diodes for thermal characterization. Thermal measurements are conducted for thermal resistances from junction to the ambient, from junction to the board, and from junction to top casing. Measurement accuracy is improved through distributed through silicon via network, multidie temperature monitoring and uncertainty analysis and minimization. It is found that the overmolded package has lower thermal resistances than the bare die package. In addition, the thermal resistance from the junction to the casing is also characterized with a liquid-cooled minichannel cold plate as heat sink, indicating the vast difference between bare die package and molded package. Besides experimental measurements, thermal simulation models under different boundary conditions are established, respectively, to compare with the measurements. Good agreements are generally achieved between simulation and measurements. Further simulation is also conducted to examine the effects of overmold thickness and power dissipation from the multichips module on the interposer.**

***Index Terms*— 2.5-D package, distributed through silicon via (TSV) network, measurement, overmolding, power dissipation, thermal characterization, thermal resistance, thermal simulation, through silicon interposer (TSI).**

I. Introduction

NEXT generation of heterogeneous integration demands for 2.5-D and 3-D chips in one package for less delay and faster speed, more functionality and less system-level power consumption. Because of the difficulty in realizing a real 3-D vertical architecture, 2.5-D package on through silicon interposer (TSI) has been envisioned as the most viable way in heterogeneous integration. In a typical 2.5-D package, dissimilar chips such as logic, memory, and ASIC chips can be assembled on an interposer, commonly made of silicon, to fulfill a quasi-3-D integration. Wafer-level packaging facilitates the manufacturability of the interconnection of multiple chips on TSI. On the other hand, the integration of multichips in one package on TSI tends to generate higher heat density, which is yet to be addressed in 2.5-D or 3-D package design [1]–[3]. In literature, the through silicon via (TSV) fabrication process and thermal characteristics due to the TSI are being studied [4]–[9]. Nonetheless, most of the work is focused on the process characteristics, or particularly relies on certain thermal simulation tools without experimental validation. Standardized thermal measurements are not well reported for 2.5-D and 3-D packages. A few thermal characterizations of 2.5-D and 3-D packages through thermal measurement in comparison with simulation are available in [10] and [11]. Oprins *et al.* [10] studied the effect of TSVs on hot spot temperature for two stacked IC on cold plate. In comparison with the case without TSV, the 11 × 11 TSV array built underneath the hot spots reduced the peak temperature in line with thermal simulation prediction, whereas the 7 × 7 TSV array increased the peak temperature, which nonetheless reversed from the simulation results. Recently, Khan *et al.* [11] reported the measurement for two stacked chips on silicon carriers cooled by microchannel heat sinks fabricated in the carriers. A heat flux of 100 W/cm^2 could be dissipated from each chip stack through a dual-port fluidic design. The measured thermal resistance was found to be 0.577 K/W for 10 mm × 10 mm chips, which was 44.3% higher than the simulation results. The common deviations between simulation and measurements could be due to factors such as process misalignment/delamination with additional interlayers and interconnections in 2.5-D/3-D packages, limited thermal and fluidic design optimization with TSVs and fluidic ports, and or lack of in-depth measurement uncertainty analysis.

In this paper, detailed thermal characterization and comparison with simulation for the 2.5-D package on TSI are described. Efforts have been made to achieve accurate measurements and characterization, including distributed TSV network to minimize interposer power loss, multiple point measurement on the chip for alignment, multiple package tests under same test conditions to minimize system error, and examination of overmolding effect. Two silicon chips simulating the logic and memory are fabricated and assembled on the interposer wafer through microbump and underfill

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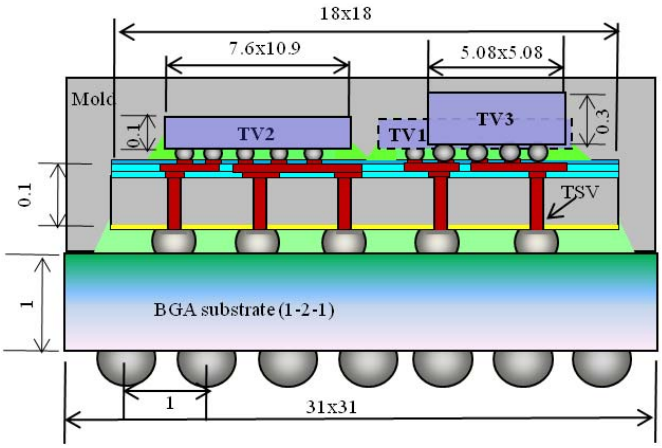

Fig. 1. Schematic of the multichip module on TSI, with TV1 behind TV3. Unit: mm.

processes. The interposer wafer has gone through the TSV process to fabricate micro vias of 10 μm in diameter and 100 μm in depth. For purpose of thermal metrics determination, the commercially off-the-shelf thermal test die is used. The test setup has been established, including data acquisition, current sourcing, cold plate, and accessory thermal and hydraulic connections. Both the bare die package and overmolded packages are examined experimentally. The thermal metrics including thermal resistances from junction to the ambient, from junction to the board and from junction to top casing, namely, Theta JA, Theta JB, and Theta JC are measured. Accurate measurements are achieved through techniques such as distributed TSV network, package electrical resistance minimization, and multiple locations die temperature monitoring and statistical data reduction.

The thermal simulation models are constructed under the corresponding boundary conditions to predict the thermal performance of the 2.5-D package with multichips on TSI. The equivalent thermal conductivities for the microbump, TSV and solder ball layer have been developed to account for the effects of various packaging elements across the package. Thermal performance metrics are derived and compared with thermal measurements. Further simulation is conducted to examine the effects of the molding thickness and maximum power dissipation from the present 2.5-D package.

II. Description of Test Packages

A. Packaging and Assembly of the 2.5-D Package

The concept of the package structure is shown in Fig. 1 and the actual packages, both molded and bare die types, are shown in Fig. 2. The molded package on board is also shown in Fig. 2. The thermal test die with a size of 5.08 mm $\times$ 5.08 mm is laid out on the silicon interposer, together with two dummy dies with sizes of 7.6 mm $\times$ 10.9 mm, 8 mm $\times$ 8 mm. All the dies are fabricated and assembled on the same interposer wafer through microbumps and underfill processes. The two dummy dies represent the logic and memory chips in a typical TSI integration. The interposer wafer has been built through TSV, copper filling, and top-side redistribution layer processes on 12 inch wafer to form micro straight vias of 10 μm in diameter and 100 μm in depth. The interposer

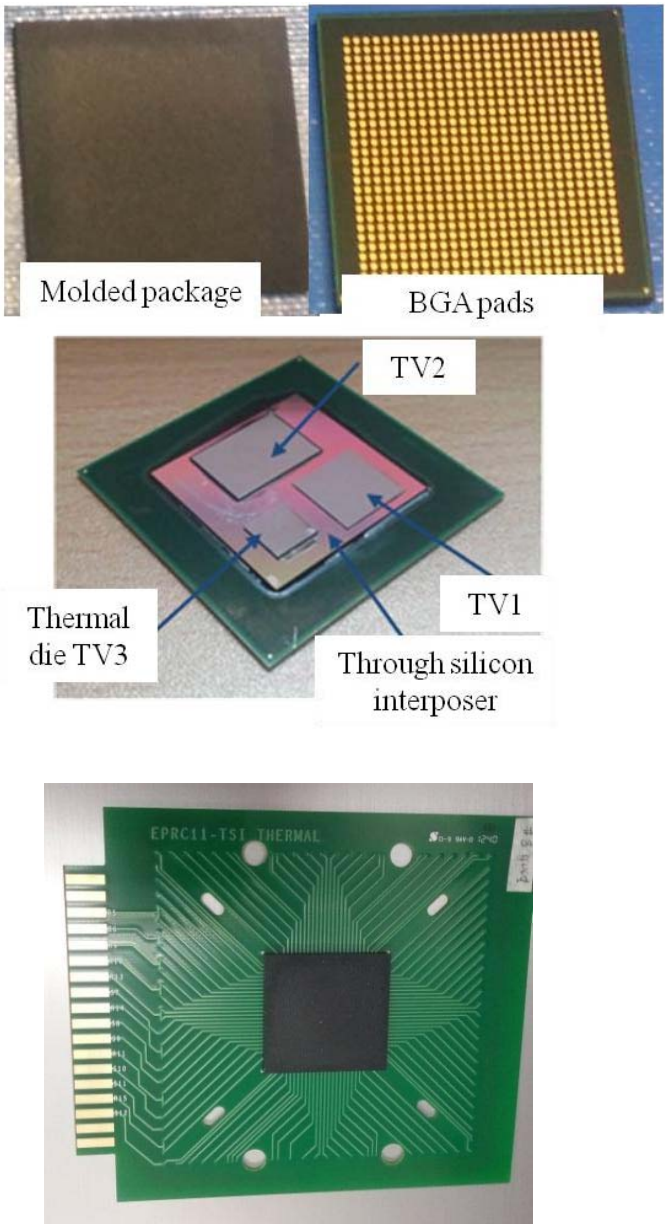

Fig. 2. Molded and bare die TSI package in 26 $\times$ 26 full array BGA format and the board assembly.

of 18 mm $\times$ 18 mm $\times$ 0.1 mm in size was then assembled onto the organic substrate of 31 mm $\times$ 31 mm $\times$ 1 mm. For the molded packages, additional molding process is conducted on the wafer level to form the epoxy molded encapsulation on the chip package. The molding layer helps protect the die from damage such as mechanical shock. The wafer is then diced into the package size. After the BGA solder ball attach process, the package is assembled on the thermal test board for electrical connections. Fig. 2 also shows the assembled thermal test board (1s0p) with molded package.

B. Thermal Test Chip Layout and Diode Calibration

The thermal test chip has been assembled on the same TSI to facilitate the thermal characterization. The thermal test chip consists of four heating unit cells of same size, covering over

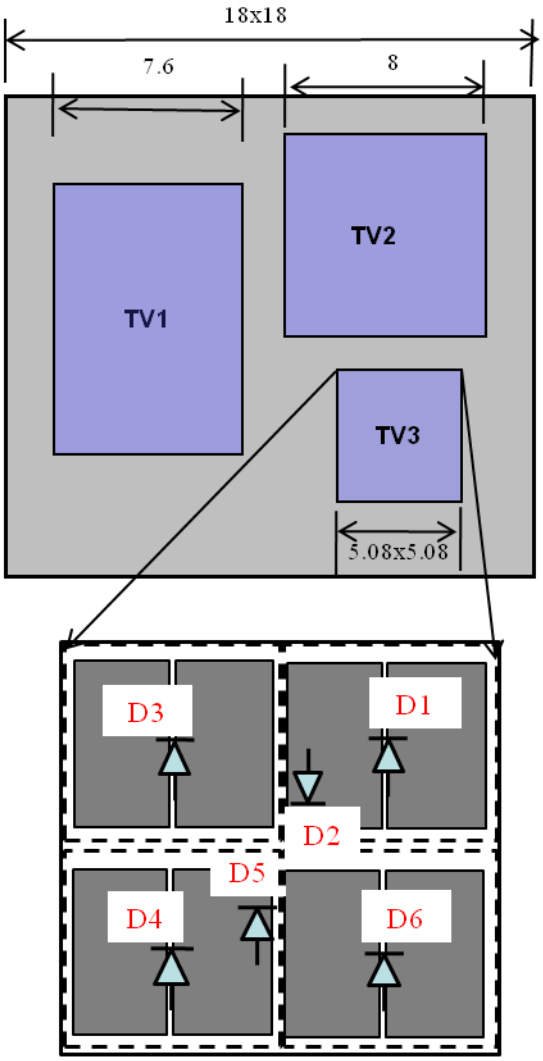

Fig. 3. Thermal test chip location on the TSI and corresponding heating cells (dashed line) and diode locations. Note that the two shadowed areas in each heating cell represent the resistors. Six diodes are routed for temperature measurements, with D1, D3, D4, and D6 at the center of each corner, and D2 and D5 near the chip center.

85% of the chip area to provide uniform heating, and six diodes for die temperature sensing. Each heating unit cell, consisting of two identical resistors connected in parallel, has equivalent dc resistance ∼3.5 Ω, with two pairs of pads at each end for electrical resistance verification, as well as equal distribution of heating current. Four diodes (D1, D3, D4, and D6) located in the four cell centers are recorded, in addition to the two diodes D2 and D5 located near the center of the chip. The locations of the resistors and diodes are shown in Fig. 3. The multiple diode locations could monitor the on-chip temperature variation and also help detect the heat sink misalignment during the testing. A D-type edge connector was used to connect the thermal test chip to the power supply and diodes for thermal testing.

The thermal diodes are calibrated in the air-convection oven with data taken at room temperature, 60 °C, 100 °C, and 140 °C to get the proportionality factor, so called K factor in semiconductor thermal management. It is found that the six diodes on the thermal test chip have excellent linearity with R-squared value ≥ 0.9999, with almost identical K factor of 517 K/V with standard deviation of 1.2 K/V based on four calibrated packages on board. Therefore, the deviation of K factor with locations is negligible in calculation of the junction temperatures. Thermal diodes are recalibrated after thermal testing, which shows an average diode K factor of 514 K/V, with a standard deviation less than 1 K/V across different diodes on the chip. Less than 1 K/V difference is identified on the average K factor difference across four packages. Overall, the contribution of diode deviation on chip temperature would be less than 1% and can be neglected in the thermal characterization. It should be noted that thermal equilibrium should be reached to get diode voltage reading, for which the variation in diode voltage is within 0.4 mV in 5 min. Occasionally, transient fluctuation could be in the range of 1–2 mV, which causes temperature variation of 0.5–1 °C. In the experiments, at least two rounds of readings are required during thermal equilibrium to avoid undesirable diode fluctuation and incorrect reading.

III. Distributed TSV Network

In high-power chips, the current flowing through fine TSV and interconnects could produce significant ohmic heat and thus generate hot spots, which may affect the operation and reliability of the package. Assuming 20 W power dissipation on the present test chip, the power dissipation on each unit cell is 5 W, which leads to a current of 0.3 A on each bump interconnection. If a single TSV with 10 μm in diameter is connected to the bump, the carrying current density and resulting heat density would be 3.8×10^5A/cm^2 and 3.9×10^5 W/cm^3, respectively, which is among the high level as indicated in literature such as [12] and [13]. In this paper, a distributed TSV network is adopted to minimize electrical resistance and Joule heating along the interposer. The corresponding die connections to the TSVs are shown in Fig. 4, with each heater cell is connected to 5×8 TSVs at one end and 6×7 TSVs at the other end. Though the diode connections are not sensitive to the wire resistance, each electrode is connected to eight TSVs as redundancy design. The cross-sectional view of thermal test chip and interconnections are also shown in Fig. 4, indicating there is no process defect on the interposer assembly. The electrical resistances across the printed circuits board (PCB) and connector, package and die are measured with a Microtech probe station and the results are shown in Table I. The test setup for the package resistance measurement is shown in Fig. 5. The die resistance is close to the system resistance, indicating workability of the TSV network and minimal power loss along the wires and packages.

IV. Thermal Measurements: Theta JA, Theta JB, and Theta JC

A. Thermal Measurement Methods

During the test, a power supply from Xantrex (XHR 150-7) is used to supply electrical power to the thermal chip, whereas the temperature reading was attained by activating the diodes with 1 mA current from the Keithley

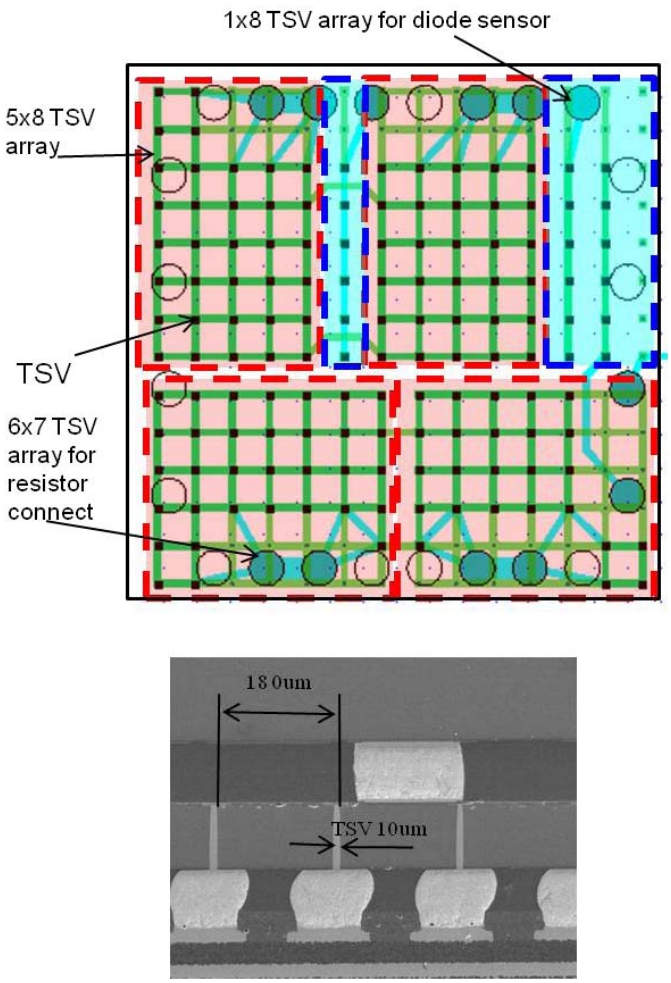

Fig. 4. Corresponding interposer top layout for the thermal chip, with one end of each heating resistor connected to 5×8 TSVs, the other end connected to 6×7 TSVs, and each diode end linked to 8 TSVs. The SEM image of the TSV underneath the thermal chip bump is also shown.

TABLE I
MEASURED ELECTRICAL RESISTANCE FROM EXTERNAL ROUTING TO DIE

Die resistance (Ohm)	3.518
Package to TSV & die resistance (Ohm)	3.52
PCB to TSV &die resistance (Ohm)	3.61
PSU to TSV & die resistance (Ohm)	3.62

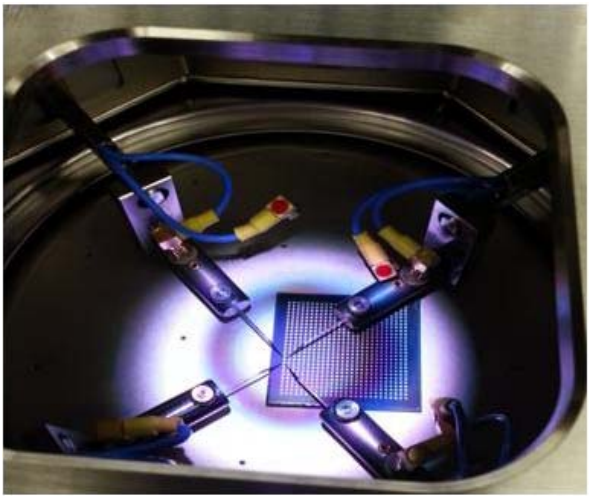

Fig. 5. Probe station test of the TSI package electrical resistance.

2400 sourcemeter. The Theta JA test configuration is shown in Fig. 6, where the test section is installed in a transparent chamber made of Perspex. For Theta JA test, the test board is arranged in the one feet cubic chamber conforming with the JEDEC standard [14]. The package is placed in still air for 10–15 min without power input and then the diode readings (V_0) and the ambient temperature ($T_{a,0}$) are recorded as initial readings. A J-type thermocouple with factory calibration is used to measure the ambient temperature. The thermocouple is inserted in a support tube, which has been fixed 25 mm below the PCB in the vertical direction and 25 mm away from the side wall in the horizontal direction. The power input is then applied, and the corresponding junction temperatures and ambient temperature are recorded at thermal equilibrium. The corresponding junction temperature T_J and thermal resistance R_{JA} are calculated as follows:

$$T_J = \Delta V \cdot K + T_{a,0} \tag{1}$$

$$R_{JA} = \frac{T_J - T_{a,t}}{P} \tag{2}$$

where $T_{a,0}$ is the ambient temperature before the power is input, $T_{a,t}$ the ambient temperature when the thermal equilibrium is reached at time t at given power input P, ΔV the average of the diode voltage difference before the power input and at time t when the thermal equilibrium is reached at a power input P, normally taking 30–45 min upon the power input. It is noted that, due to chip heating, $T_{a,t}$ is usually 1–2 °C higher than $T_{a,0}$, which should be considered for accurate calculation of R_{JA}.

For the Theta JB and Theta JC characterization, a liquid cooling loop is established, which includes the micropump (Monarch pump), heat exchanger (Lytron LL510), temperature-controlled chiller (Huber K6S-NR), together with the piping and fittings. The double-ring cold plate for Theta JB and minichannel heat sink for Theta JC is shown in Figs. 7 and 8, respectively. The coolant water temperature is set to 24 °C, which is within 1 °C variation from the ambient temperature. The exact inlet temperature is measured with a J-type thermocouple mounted at fluid inport. The flowrate is fixed to be 0.4 mL/min throughout the experiments.

The Theta JB measurement basically follows JESD 51-8 as outlined in [15]. The double-ring test jig is shown in Fig. 7, which is to cool the package from the top and bottom sides of the PCB. A T-type thermocouple of 36 gauge is soldered onto the board for board temperature measurement. In the

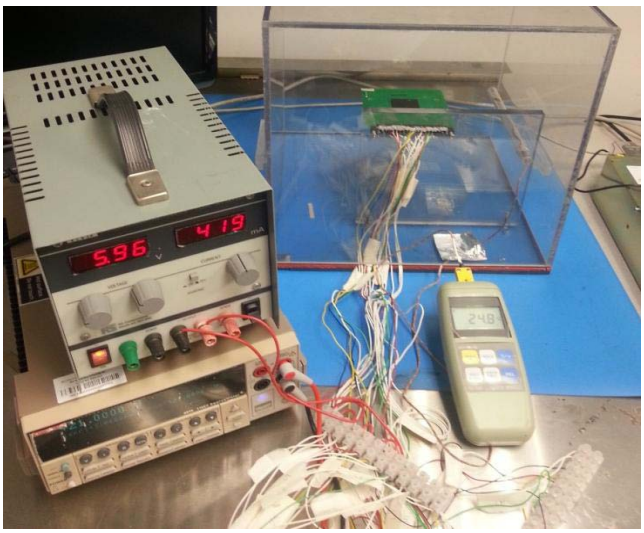

Fig. 6. Test configuration for Theta JA test jig under natural convection.

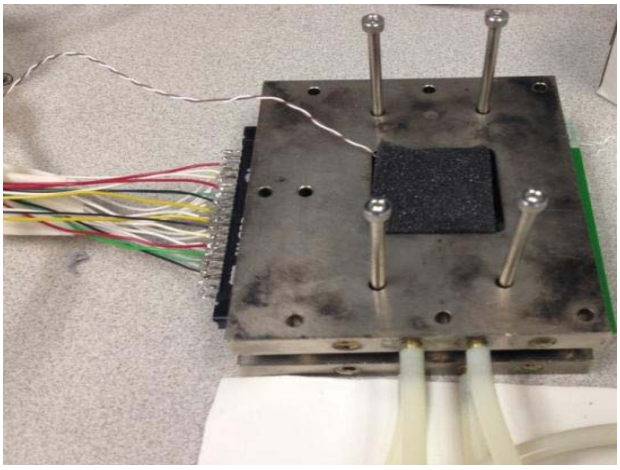

Fig. 7. Test configuration for Theta JB with double-ring cold plate.

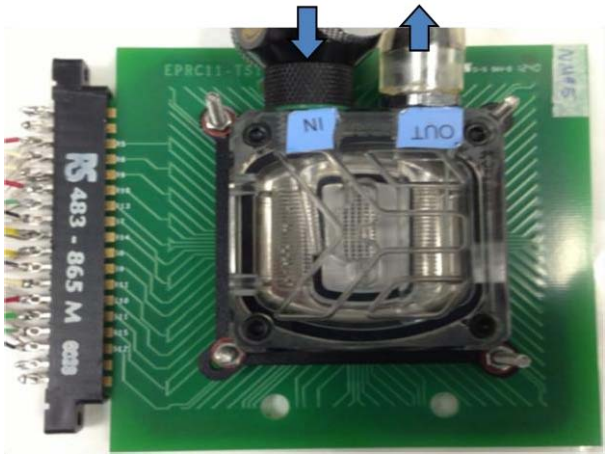

Fig. 8. Theta JC test jig with the heat sink mounted on top.

experiment, the soldering of thermocouple on the dummy traces of the PCB is acceptable. Nonetheless, the distance from the solder bead to the package edge is difficult to control to be exactly 1 mm. The actual distance from the solder center to the package edge is measured 2 mm in the present case. A foam insulation is installed on top of the package to minimize heat flow directly from the top to the ambient. Theta JB is calculated in the similar way as the Theta JA, with the board temperature $T_{B,t}$ in place of the ambient temperature at thermal equilibrium with the power input P

$$R_{JB} = \frac{(T_J - T_{B,t})}{P}. \tag{3}$$

In the Theta JC measurement, the most difficult part is to measure the maximum casing temperature accurately, especially in real cases such as nonuniform chip heating, off-center heating and multiple chip heating. There is also no JEDEC standard available at this stage due to the measurement difficulty [16]–[18]. Instead of direct measurement of the casing temperature, a minichannel heat sink made of copper plated with nickel, with 0.5 mm channel and fin widths, was mounted on the top of the package to remove heat. Thermal grease with a thermal conductivity of 3.2 W/mK is used as the thermal interface material because of its minimum interfacial thermal resistance. Other solid or soft thermal interface materials such as thermal pads are not recommended due to their large contact thermal resistance, which adds to the Theta JC value in spite of the claimed high thermal conductivity of 5 W/mK. The present method conforms with the standard MIL-STD 883-method 1012.1 [17], though there is no JEDEC standard. Fig. 8 shows the test configuration for Theta JC. To avoid heat conduction from interposer to the heat sink base, a plastic film ~0.1 mm is applied on top of the interposer beside from the thermal test chip to insulate the heat sink contact with the interposer directly. It should be noted that the present Theta JC measurement method is applicable for cases where Theta JC is much larger than the heat sink thermal resistance.

Similar to the Theta JA and Theta JB measurements, the ambient temperature and diode readings for the chip under nonheating condition have been recorded in advance. The heating power is then applied to the chip. The temperature difference between inlet water and ambient is controlled within around 1 °C during the test. The temperatures and heating power are recorded when thermal equilibrium is reached, which usually takes 20 min. Alignment of heat sink with the die surface is required to make sure good thermal contact. The temperature difference between the junction and the inlet fluid is used for calculating Theta JC, namely

$$R_{JC} = \frac{(T_J - T_{w,t})}{P} \tag{4}$$

where the inlet water temperature $T_{w,t}$ at thermal equilibrium time t is used for calculated R_{JC}.

B. Uncertainty Analysis

The measurement uncertainty is estimated as follows. Each TSV has a resistance around 20 mΩ and the TSV network has a smaller resistance, which can be neglected in the overall power supply calculation. The wire connections from the power supply to the die has average electrical resistance of 0.1 Ω, which is much smaller than the die resistance of

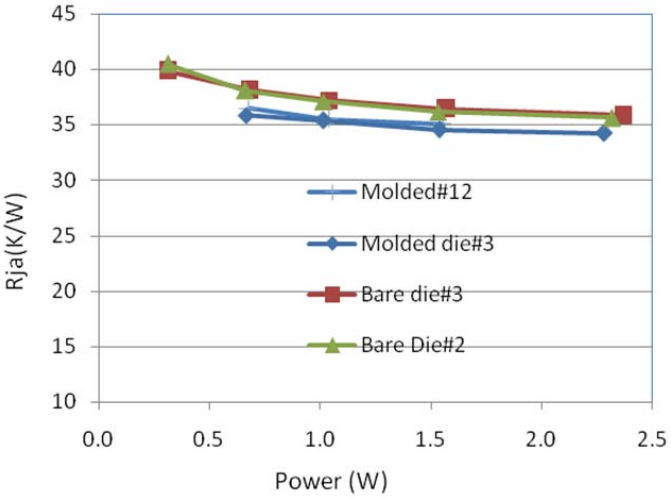

Fig. 9. Measured Theta JA under natural convection condition for both molded and bare die package.

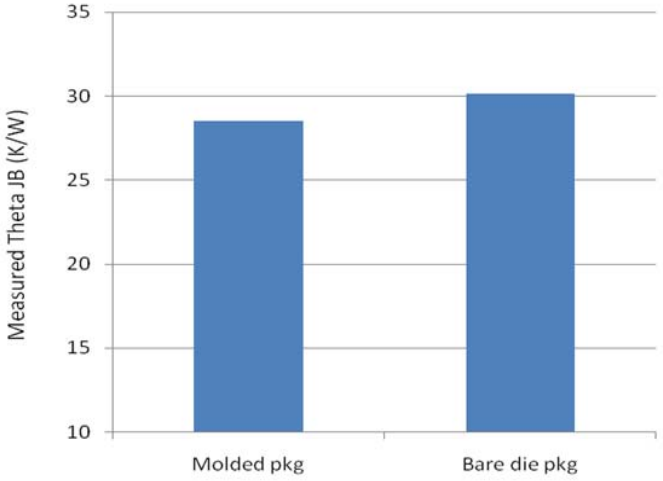

Fig. 10. Measured Theta JB under 1 W power input for both molded and bare die package.

3.5 Ω. The wire resistances from the die to the external power supply may accounts for 2.8% of electrical power, which nonetheless is not excluded from the calculation of the present thermal resistance. The product of the current and voltage of the dc power supply is used as the power to the test chip with uncertainty within 1% from the displayed readings. The temperature sensing deviation is estimated to be 0.2 °C for a minimum junction temperature rise of 7–8 °C, or maximum 2.5% for the overall test range up to 100 °C. Thus the uncertainty for the thermal resistances is estimated to be around 5%. In general, repeated tests under the same test conditions give a variation around 1% since the measurement system error is minimized. As such, the small difference in the thermal performances for molded packages from the bare die packages could be detected.

C. Measurement Results

The measured thermal resistances for Theta JA are shown in Fig. 9 for both the molded packages and bare die packages under power input 0.3–2.45 W. Two packages in the same package type have been tested and shown in the same figure. Theta JB under 1W power input are shown in Fig. 10. According to Theta JA and Theta JB measurements and corresponding thermal simulation in the later section, the molded packages are found to give consistently lower thermal resistances than the bare die packages. This can be partially attributed to the enhanced thermal radiation effect due to the molding compound with the surface emissivity ∼0.9, larger than that of silicon surfaces in the range of 0.1 for the bare die package. The emissivity value can be confirmed by matching the infrared camera reading with the diode temperature reading. Molding on the BGA substrate also assists the heat conduction from die to substrate and thus would reduce the thermal resistance.

Table II shows Theta JC results for both bare die and over-molded packages. It is identified that the Theta JC for the bare die package is one order of magnitude smaller than the molded package. The molding layer, with a thermal conductivity of 0.7 W/mK, greatly adds to this thermal resistance. For the accurate measurement of Theta JC for the bare die package, larger power inputs (8-20 W) are supplied to achieve a junction temperature rise ∼7 °C or higher to minimize junction temperature reading error in the Theta JC measurement case. A common problem in Theta JC measurement for the bare die package is the misalignment of the heat sink base with the top of the test die. Misalignment would generate additional interfacial thermal resistance and abnormally high on-chip temperature variation. Table III shows the on-chip temperature variations for misaligned in the first run (Run 1) and well-aligned heat sink (Run 2) for the bare die package. In comparison, the Run 1 has abnormally large temperature variation on the chip due to tilting heat sink, which leads to large Theta JC of 1.2 K/W and temperature variation of 9.7 °C as the difference of maximum and minimum diode temperatures in spite of uniform heating. Such a thermal assembly is attributed to the interfacial misalignment resulting unacceptably large die temperature variation and should be reassembled and tested. Run 2 is considered good alignment due to small on-chip temperature variation under uniform heating condition, and can be viewed as proper thermal characterization with a low thermal resistance of 0.83 K/W for the bare die package. In real application, alignment mechanism should be established to minimize interfacial thermal resistance for high performance cooling of the bare die package on TSI.

TABLE II
MEASURED THETA JC: MOLDED AND BARE DIE PACKAGES

Molded package power(W)	R_{JC} (K/W)	Bare die package power(W)	R_{JC} (K/W)
1	10.9	8	0.85
2	10.9	14	0.84
4	10.8	20	0.83

TABLE III
MEASURED JUNCTION TEMPERATURE FOR BARE DIE PACKAGE R_{JC} TESTING. UNIT: °C

Rjc test	Run1 at 20W	Run2 at 20W
$T_{w,t}$	25.0	25.1
D1	54.8	44.7
D2	45.7	41.0
D3	50.8	43.0
D4	48.3	41.7
D5	46.2	41.0
D6	45.1	41.9
Average T_J	48.5	42.2
Standard deviation	3.7	1.4
Max temperature variation	9.7	3.7
Remark	Heat sink not well aligned	Good heat sink alignment

V. THERMAL SIMULATION

A. Thermal Model Validation

The thermal models for the three test conditions are constructed, respectively, with commercial software Flotherm. As shown in previous studies [4], [5], the various TSV structure can be lumped as a compact interposer model without detailed modeling of individual TSV structure. The silicon interposer has been modeled as anisotropic thermal conductor by considering the contribution from the TSVs. In the present case, due to the large pitch between TSVs, there is no much increase in the thermal conductivity across the TSI. The flip chip bumping with underfills are modeled as simplified solid blocks with equivalent thermal conductivity. The thermal conductivity for each package layer is shown in Table IV. Note that the different layers of copper traces on the substrate are modeled as uniform blocks with equivalent thermal conductivity. Since the copper trace fan-outs underneath different dies are not interconnected on layer 1 (L1), the heat spreading from thermal test chip to the rest of the layer is limited by the bulk substrate material. Strips with thermal conductivity of 0.2 W/mK are applied on the L1 layer to separate the different trace fan-outs on the substrate and to avoid unrealistic heat spreading in L1 lumped with copper plane. Thus, the accuracy of the computed junction temperature would be improved by a few percent for the Theta JA and Theta JB cases. Moreover, thermal radiation effect is considered in the Theta JA thermal simulation. Neglect of thermal radiation would overestimate Theta JA by 27% at 2 W power input, which is not acceptable as standardized thermal performance characterization.

TABLE IV
THERMAL CONDUCTIVITY DATA FOR THE TSI PACKAGE

Package materials	Thermal conductivity (W/mK)
Silicon die	100
TSI interposer	K//=100, K⊥=101
Microbump and underfill layer under TV1/TV2	K//=1.3, K⊥=6.2
Microbump and underfill layer under TV3	K//=1.0, K⊥=5.0 for peripheral bumps, 0.5 for center area
TSI bump and underfill layer under	K//=0.4, K⊥=6.88
BT Substrate with vias	K//=0.2, K⊥=0.5
Substrate copper Layers: L1, L2, L3, L4 (L1 with separate strip corresponding to die footprint)	128, 160, 155, 103
Solder ball layer	K//=0.04, K⊥=8.1
PCB FR-4	K//=0.8, K⊥=0.3
PCB copper layer L1	20
Molding compound	0.7

A grid independence study is also conducted. The mesh system for the package is around 341 K under natural convection condition, 600 K under double-ring cold plate condition, and 990 K under heat sink cooling condition, with denser grid cells in the packages. The numerical meshes for the packages are maintained in the same level for all the three test conditions. We investigate the grid independence under natural convection. The mesh density is increased to 580 K by increasing the mesh of the package by 50%, including the thermal die, interposer, substrate, and PCB. The deviation in T_j is found within 1%. Therefore the present mesh sizes are considered sufficient and used for all the simulation in the ensuing part of this paper.

Fig. 11 shows the thermal simulation model for the TSI package based on the present test board (1s0p) together with the temperature and air flow profiles in the A-A cross section under the Theta JA test condition. Fig. 12 shows the comparison of simulation results versus averaged thermal resistances for both the bare die and overmolded packages.

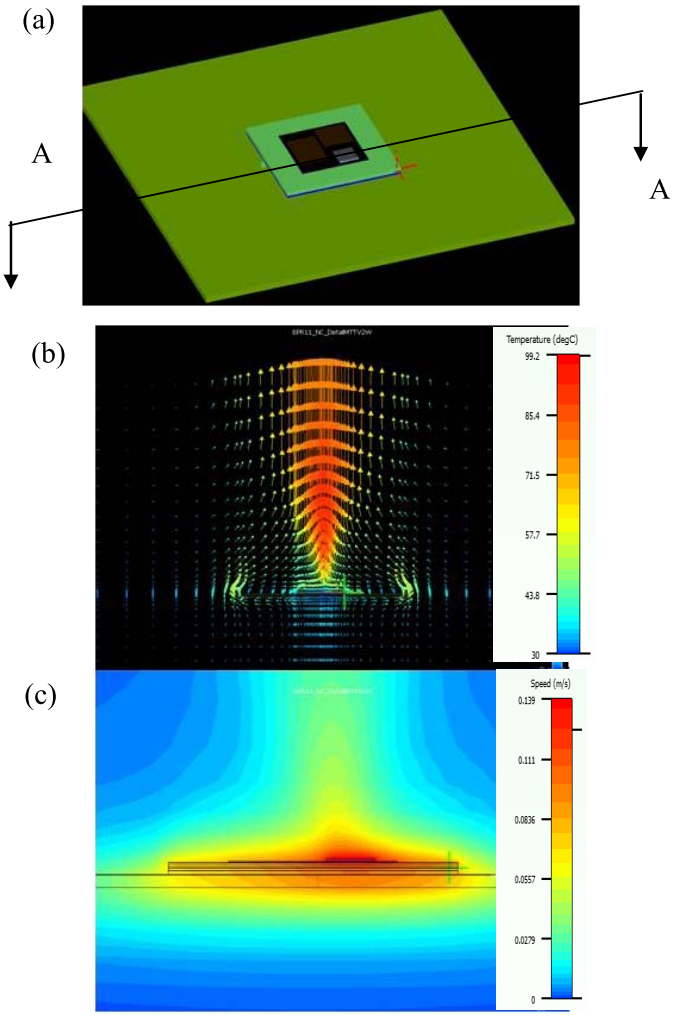

Fig. 11. Thermal simulation model for (a) TSI package and simulation results at the A-A cross section cutting through the thermal test die, (b) air flow, and (c) temperature profile.

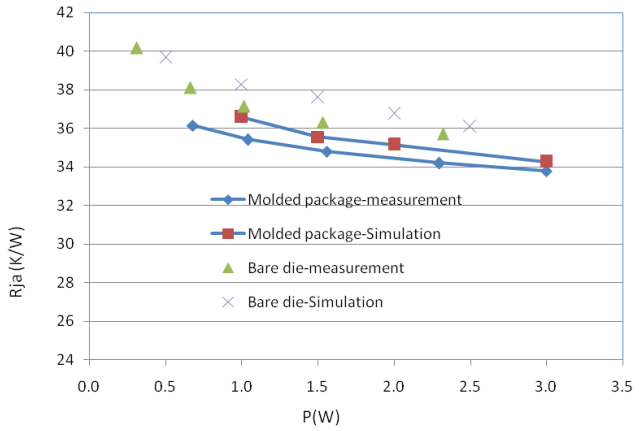

Fig. 12. Comparison of simulation results versus measurements.

Note that the thermal resistance for each package type has been averaged and fitted based on the measurements displayed in Fig. 9. Good agreement is found between characterization and simulation at different power inputs. For Theta JB test, the double-ring cold plates are modeled. The thermal resistance obtained from thermal simulation is shown in comparison with the measurement in Fig. 13.

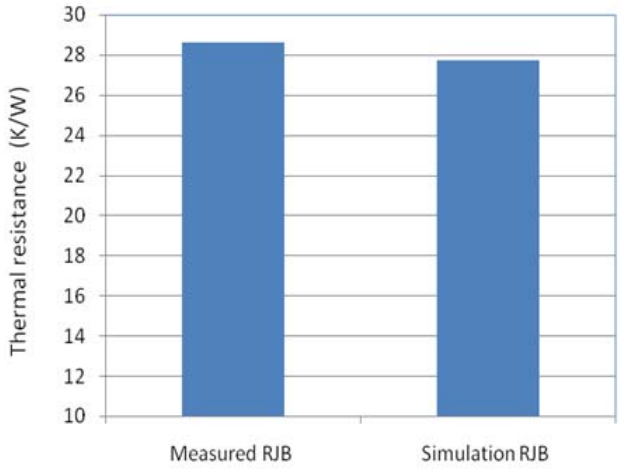

Fig. 13. Comparison of simulation versus measurement for R_{JB}.

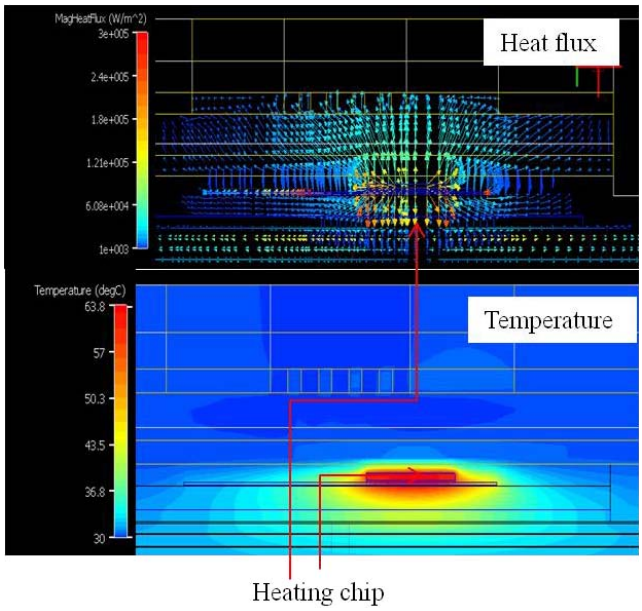

Fig. 14. Heat flux and temperature profiles for the molded package in the A-A plane under heat sink cooling for determining Theta JC.

The corresponding heat flux and temperature profiles based on thermal simulation for the molded package are shown in Fig. 14. As the thermal performance of the minichannel heat sink is not known, the detailed fin/channel structure is modeled together with the inlet and outlet to extract the thermal performance. Table V shows the comparison of Theta JC. In the thermal simulation, the nominal interfacial resistance of 0.098 K cm^2/W from supplier's datasheet for the thermal grease has been incorporated in the simulation model. Good agreement is found for the bare die package. For the molded package, a relatively obvious discrepancy of 10.4% is found. The molded package is cross sectioned and the microscopic view shows a surface roughness approximately 15–20 μm as shown in Fig. 15. The presence of roughness is beneficial to the mold release process but it may cause additional interfacial thermal resistance. Surface warpage could also contribute to the deviation of simulation from measurement.

TABLE V
MEASURED AND SIMULATION RESULTS FOR THETA JC

Package types	Power input (W)	Measured R_{JC} (K/W)	Simulation (K/W)	Difference from measurements
Molded package	2	10.9	9.76	-10.4%
Bare die package	14	0.84	0.82	-2.4%

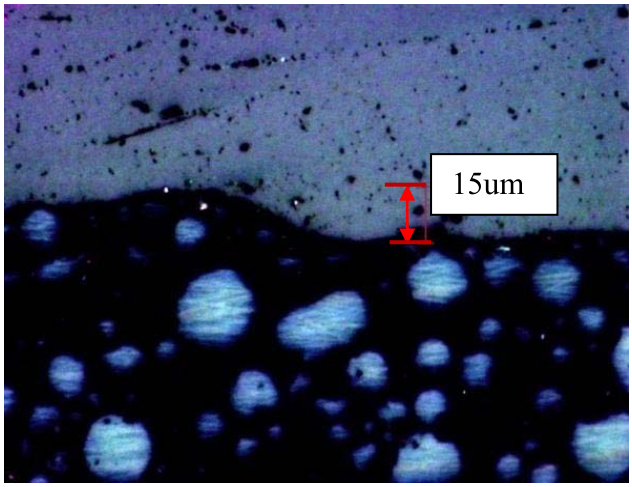

Fig. 15. Cross section of the molding compound.

It is feasible to examine the heat sink performance through simulation even if TV3 is located off the package center (Fig. 3). Here are two methods to calculate the heat sink resistances. The first method is a conventional method based on the heat sink base center corresponding to the center of the package, which leads to heat sink thermal resistance of 0.076 K/W for the bare die package and 0.085 K/W for the molded package. The other method is based on the heat sink base corresponding to the heating chip TV3, which results in a nontrivial thermal resistance 0.31 K/W for the bare die package and 0.22 K/W for the molded package. Because the current focus is to determine R_{JC}, we may not take much space to discuss which heat sink thermal resistance is more representative in this paper.

B. Effect of Overmolding Thickness

With the validated thermal model, it is feasible to conduct thermal simulation on the parameter effects. One of the key package parameter is the thickness of overmolding for the 2.5-D package. The molding layer helps protect the silicon dies from being damaged but has a large impact on Theta JC, though its effect on Theta JA is favorable. Fig. 16 shows the Theta JC versus the molding thickness based on simulation study. It is seen that, with the increase in overmolding thickness from 0 to 0.6 mm, the thermal resistance increases drastically from 0.82 to 11.76 K/W, mainly due to the thermal conduction resistance across the overmolding layer. If additional thermal solution such as heat sink is applied at

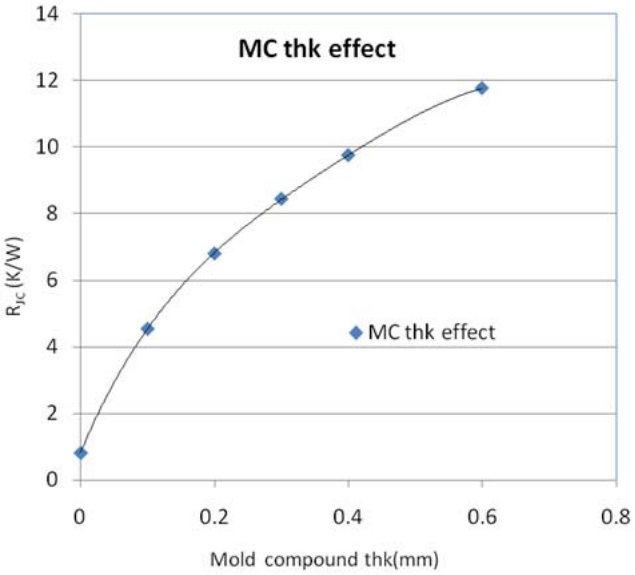

Fig. 16. Effect of molding compound thickness on the R_{JC}.

the top of the package, a thin overmolding thickness ~0.1 mm or even bare die package is suggested to minimize the overall thermal resistance.

C. Maximum Package Power Dissipation

The validated thermal model can also be used to predict the maximum power dissipation from the simultaneous heating of TV1 and TV2 dies under passive cooling condition. This can be achieved by assigning power dissipations of 1 and 2 W on the two dies while keeping the thermal die power to be zero. The interaction of the multichip heating on the 1s0p thermal board under natural convection condition can be expressed in the linear superposition form, namely

$$\begin{bmatrix}\Delta T_{j1}\\ \Delta T_{j2}\end{bmatrix}=\begin{bmatrix}A11 & A12\\ A21 & A22\end{bmatrix}\begin{bmatrix}P1\\ P2\end{bmatrix}=\begin{bmatrix}33.0 & 19.0\\ 22.2 & 28.9\end{bmatrix}\begin{bmatrix}P1\\ P2\end{bmatrix} \quad (5)$$

where ΔT_{j1}, ΔT_{j2} are the junction temperature rises in °C, A_{11}, A_{12}, A_{21}, A_{22} are the influence factors in °C /W due to the power dissipations P1 and P2 in Watts for TV1 and TV2, respectively. Given a temperature rise, we can estimate the allowable electrical design power with (5). For example, the present package format could dissipate 2.3 W at the temperature rise of ΔT_{j1}, $\Delta T_{j2} \sim 60$ °C. To improve the power dissipation without heat sink on top, an immediate method is to use a thermally enhanced four-layer PCB (2s2p). The computed power dissipation from a 4L PCB is correlated with the linear superposition approach through thermal simulation. The power dissipation with the two chips on TSI package can go up to 3.5 W with the same temperature window of 60 °C.

VI. CONCLUSION

Thermal characterization and analysis for 2.5-D package with multichips mounting on the TSI is presented. Two dummy dies and a thermal die are assembled onto the TSI, with TSVs of 10 μm in diameter and 100 μm in depth, to form

BGA package. The embedded thermal test die facilitates the thermal characterization with accurate measurements under different test conditions. The thermal performances for the TSI packages, either in bare die or molded types, are measured under different conditions to obtain Theta JA, Theta JB, and Theta JC, respectively. To identify and minimize the measurement error, efforts have been made such as distributed TSV network design, package resistance measurement, multiple die location temperature monitoring, heat sink alignment verification, multiple package tests under same test conditions, and package cross-sectional analysis.

Favorable thermal advantages of the molded package over the bare die package are identified in Theta JA and Theta JB due to the mold compound over the substrate. For Theta JC, a drastic performance difference is identified for the bare die package and the molded package. A low thermal resistance of 0.82 K/W is achieved for the 5.08 mm $\times$ 5.08 mm bare chip on TSI. This is equivalent to a specific thermal resistance of 0.21 K cm^2/W, which is the lowest among the thermal resistances as reported in literature [4]–[6] and [11]. Because of the dominant overmolding thermal resistance layer, the Theta JC for the overmold package has high thermal resistance of 10.9 K/W. A thinner overmolding layer such as 0.1 mm is suggested to minimize Theta JC for top cooling scenario. In addition, the thermal simulation models are constructed in line with the experimental conditions. The simulation results are in good agreements with measurements, validating the thermal models. Further simulation is conducted to study the effect of the overmolding thickness. The module power dissipation under natural convection is also estimated with the present simulation model. With a 4L thermally enhanced PCB, the power dissipation is increased to 3.5 W at a temperature rise of 60 °C.

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