# Polymer Based Dual Damascene Process for Fine Pitch RDL Advanced Packaging

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**Abstract**

In this paper, a trench-first dual damascene process is used to demonstrate 1 µm L/S meander trenches and 1 µm CD and space vias. A non-phototype polymer material is selected as the dielectric layer and two layers of 1 µm dielectric are spin-coated. The issues and costs associated with the chemical mechanical planarization (CMP) process are eliminated. In the lithography process, a 1.5 µm thick photoresist was spin-coated using optimized exposure energy patterns of 1 µm L/S trench and 1 µm CD and space vias, respectively. Finally, dry etch parameters were fine-tuned to complete etching of 1 µm L/S meander trenches and 1 µm CD and space vias.

## INTRODUCTION

As we enter the high-speed computing and artificial intelligence era, the integrated circuit industry needs to meet Moore's law and reduce manufacturing costs. When the 2-nm node technology matures, advanced packaging technologies must be utilized to maximize performance [1]. Therefore, how to provide high-density and high-speed interconnection links to minimize high-frequency electrical transmission loss has become a vital issue in advanced packaging technology [2]. Among the advanced packaging technologies in recent years, the fine pitch redistribution layer (RDL) connection technology is mainly used in the Fan-out wafer-level package (FOWLP). The reason is that the process cost of FOWLP is lower, and the RDL provides more layer stacking and wider winding distribution. FOWLP fabricates high-density redistribution layers using a semi-additive process (SAP) [3]. However, SAP had some difficulties to overcome [4]. 1. Copper oxidation in reliability high-temperature test. 2. After multi-layer RDL stacking, it will cause a copper undulation phenomenon. 3. Due to the over-etching of Ti during the seed layer etching process, the adhesion of RDL is not better in the thinner line width. To overcome some shortcomings of SAP fabricated RDL, this research uses photolithography and dry etching process to fabricate polymer-based dual damascene RDL for application in future advanced packaging technology with 1µm line and space (L/S)

### Test Vehicle Description

Fabricated polymer-based Cu dual damascene RDLs with vias on 300 mm wafer using 2 layers polymers. To design vias ranging with a minimum CD is 0.7µm and maximum CD is 5µm and Cu trench with L/S from 0.7µm to 5µm. The design test vehicle is shown in Fig. 1.

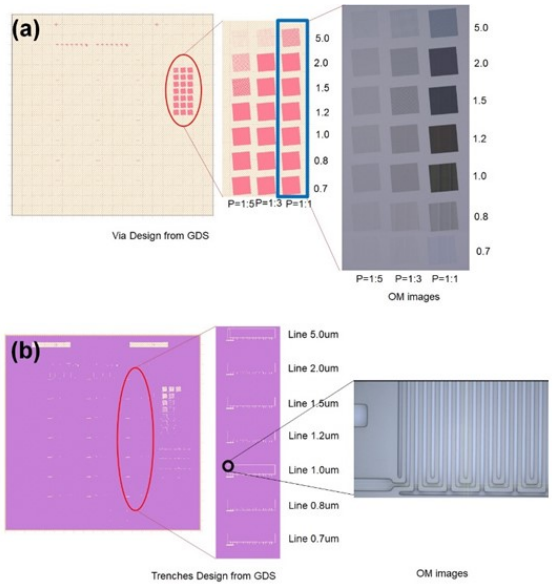


Fig. 1. Design for 1 µm L/S polymer-based Cu damascene RDLs (a) vias and (b) Trenches

## 2. METHODOLOGY

We demonstrated the capability to fabricate an advanced 1µm L/S polymer-based Cu dual damascene RDL using the trench first process.

1. To coat a layer of 1-2 µm polymer on the silicon wafer with TEOS and Aluminum and perform soft baking and curing. To use SFX 200 to measure the thickness of the polymer. A dry etching stop layer is grown on the polymer to make the endpoint of dry etching for the polymer trench. To coat the secondary layer of the polymer as the thread patterns. The exact process goes through soft baking, curing, and thickness measuring.

2. To prepare for the dry etching process by coating one layer of the hard mask to use dry etching to make the patterns of the trenches. After the dry etching of the trenches, remove the hard mask, and then coat another layer of hard mask via patterns of etching. Finally, remove the hard mask.

3. The third stage is Cu metal filling and planarization. It mainly uses electroplating and chemical mechanical planarization (CMP) processes to fill the entire trench and planarize the polymer based RDLs. Finally, some electrical measurements with leakage current and Rc will be performed.

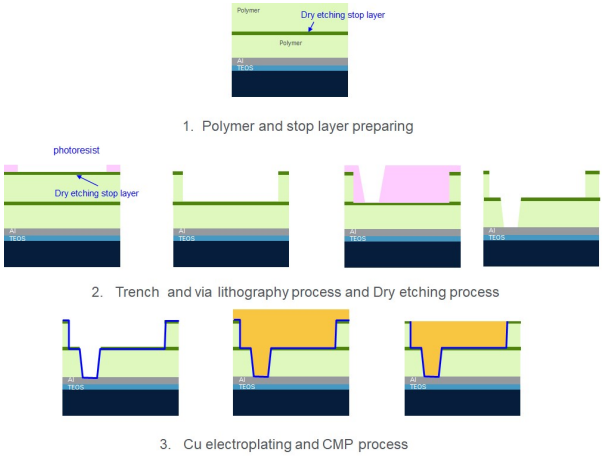


Fig. 2. Process flow for polymer-based Cu dual damascene RDL fabrication

**Polymer materials decision for Dual Damascene RDL**

For this experiment, it is necessary to decide on a suitable polymer material. The requirements for a suitable polymer are as follows: Firstly, it must be able to reach a thickness of 1 um after curing. Secondly, the polymer must be able to withstand the high temperature dry etching process without delamination. Thirdly, the polymer must be able to withstand the CMP process after copper plating without polymer delamination. Three different polymer materials are therefore used as dielectric materials. Polymer A is a negative tone polymer, polymer B is a positive tone polymer and polymer C is a non-photo type polymer.

Polymers A and B are commonly used as dielectric polymer layers in RDL. However, the thinnest thickness can reach 5 μm and 7 μm after the polymer curing process. Therefore, to reduce the thickness of the polymer to 1 μm, it is necessary to use the CMP process. The results of the CMP process for polymer A and polymer B are shown in Fig. 3(a)-(d). After the CMP process, only the center of the polymer remains, and polymer A is completely stripped. Polymer B can withstand the CMP process, but after the thickness is less than 2 μm, it can be seen that the polymer peeling phenomenon starts to occur.

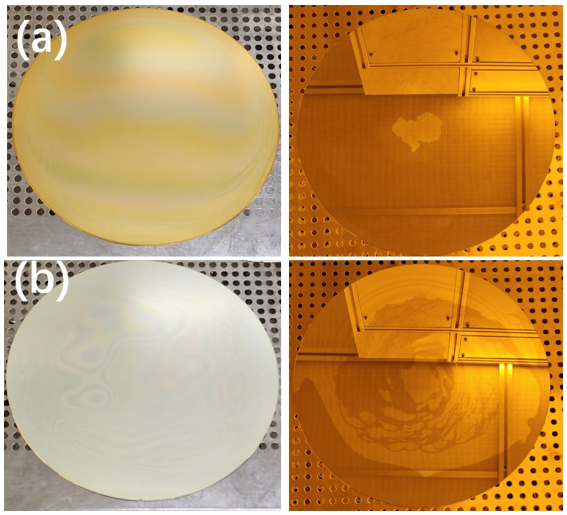


Fig. 3. The results of (a) polymer A and (b) polymer B before and after CMP process

Therefore, we chose polymer C as the polymer dielectric for this experiment. Because it can be coated directly to the silicon wafer after appropriate dilution, after curing at 350°C, the polymer dielectric layer of 1 μm thickness can be achieved without the CMP process. The result is shown in Fig. 4(a)-(c).

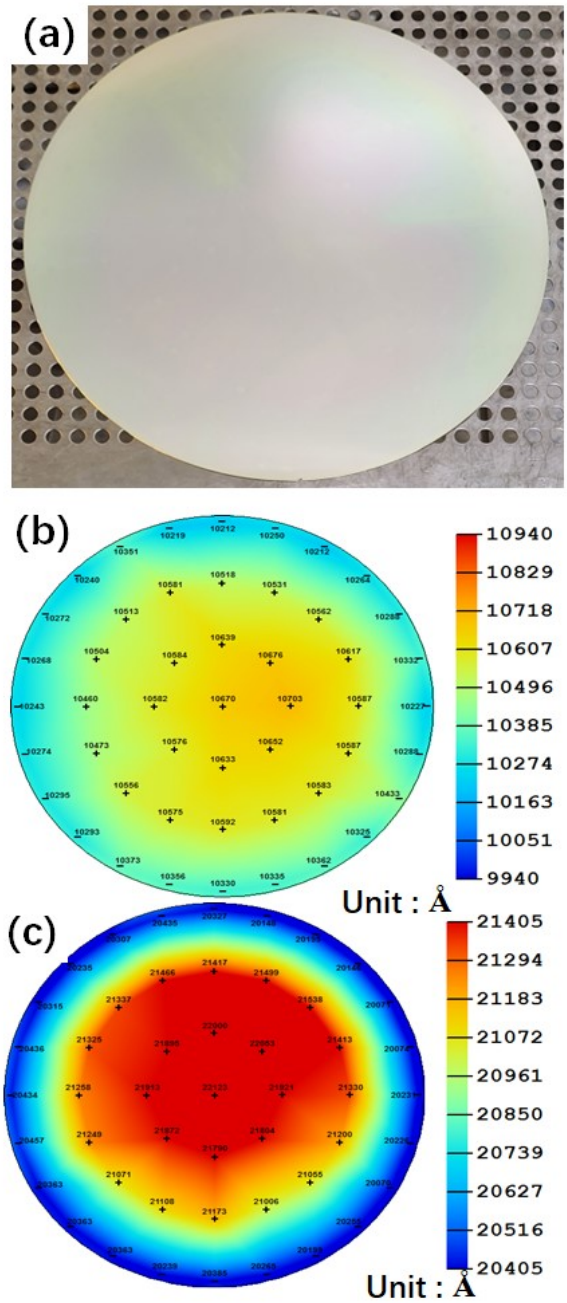


Fig. 4. The results of polymer C (a) after curing process, (b) map of polymer C thickness on a Si wafer for 1st layer and (c) for 2nd layer coating

**Lithography process evaluation for Dual Damascene RDL**

The lithography process plays an essential role in the subsequent dry etching process. It affects whether or not the dry etching performance can be achieved. If the photoresist is properly developed, the dry etching will be able to be complete; conversely, if the CD and L/S are too large after the lithography process, the desired dimensions will not be achieved. Therefore, the evaluation of the lithography process is necessary.

Two types of photoresists are used for evaluation in the experiment. Photoresist A can reach a minimum thickness of 3 μm, and photoresist B can reach a minimum thickness of 1.5 μm.

The thickness of the photoresist will affect the result of the subsequent process. After the lithography process, the photoresist will have good coverage, which can minimize the result of over-etching. However, if the photoresist is too thick, the resolution will be too low to achieve 1 μm CD and L/S. In addition, too much photoresist will be left over, requiring more cleaning operations to remove the remaining resist.

On the contrary, if it used thinner photoresist, it will be easier to achieve 1 μm CD and L/S. The photoresist residue is less, and the cleaning is more straightforward. However, the photoresist is less effective in preventing etching.

The results of photoresist A after lithography process are shown in the Fig. 5(a) and (b), in terms of photoresist coating, the thinnest thickness of photoresist A can be minimum to 2.5 μm. In the Focus Exposure Matrix (FEM) for process windows of photoresist A, the exposure energy is from 80 mJ/cm$^2$ to 350 mJ/cm$^2$, and other parameters are kept fixed. At lower exposure energy, the photoresist is under develop. When the exposure energy increases to optimized exposure energy, it is observed that the bottom of the vias pattern can be current develop. For trench patterns, the bottom of the trench is correct develop when used optimized exposure energy. However, for vias patterns, the top CD is about 2 μm and the bottom CD is about 1.6 μm, which exceeds the required CD. For trench patterns, the top CD is about 2.0 μm and the bottom CD is about 1.5 μm, which also exceeds the target CD. This result is for a L/S more than 2 μm. When the L/S is 1 μm or less than 1 μm, we can observe from the microscope images that all the photoresist has disappeared after developed (Fig. 5(c)). Therefore, the dimensions of the trench and vias patterns of photoresist A are larger than 1 μm, and the patterns cannot be patterned for 2 μm L/S.

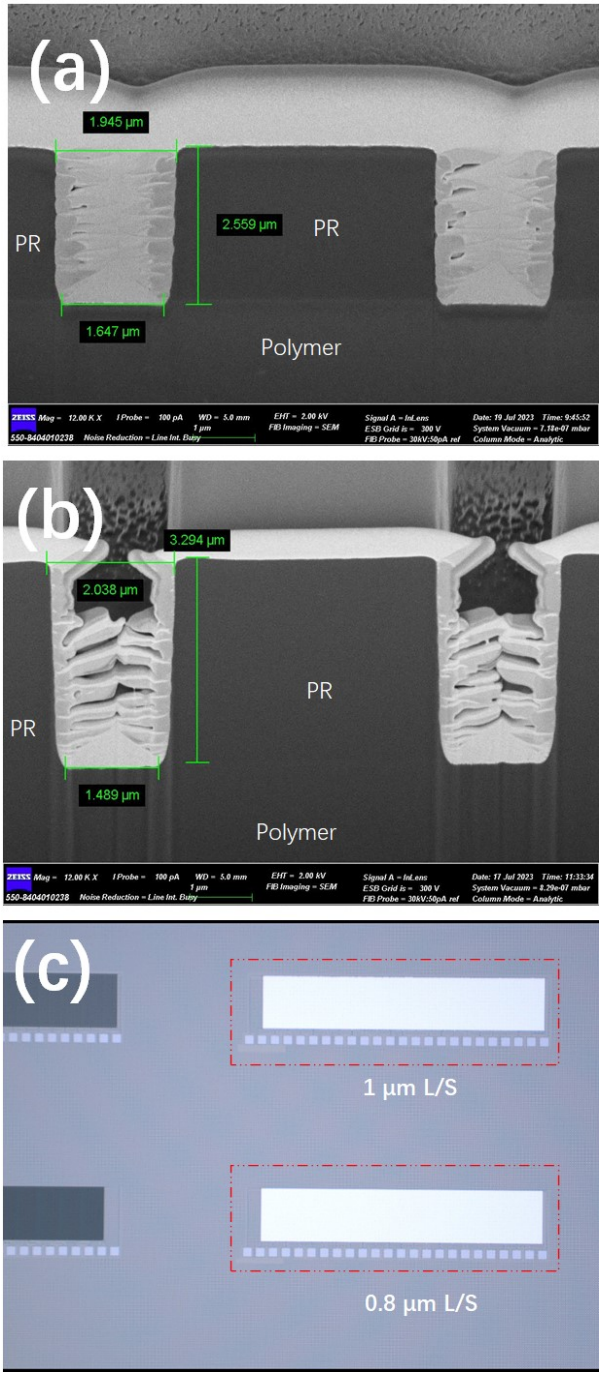


Fig. 5. The results of photoresist A after lithography process (a) cross-sectional view of vias, (b) cross-sectional view of trench, (c) OM image of less than 1 μm L/S trenches

Photoresist B can be spin coated to a thickness of less than 2 µm. Therefore, it is more suitable for patterning line width and line spacing less than 1 µm, and 1 µm vias.

To spin-coat 1.5 µm of photoresist B, an optimized exposure energy was used, and 1 µm L/S trenches successful pattern was observed. The results is shown in Fig. 6(c) and (d). On the contrary, for 1µm CD and space vias, the vias in the same layer as the trench can be patterned, but the vias inside the trench cannot be patterned. Since the vias inside the trench are 1 µm deeper than the trench and the CD is small, the exposure energy required must be higher than trenches. Therefore, the exposure energy was increased to optimized exposure energy, and from the SEM results are shown in Fig. 6(a) and (b), it was observed that the vias inside the trench had been developed. Furthermore, the CD of the bottom via is 1 µm.

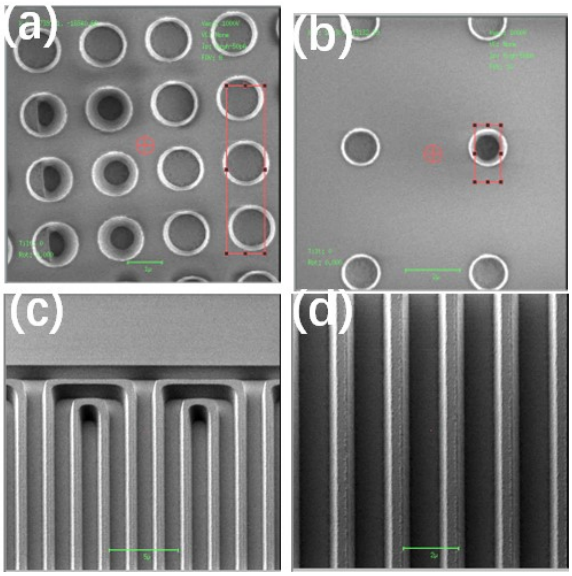


Fig. 6. The SEM images of photoresist B (a) vias inside trench, (b) via in kelvin test structure, (c) top of meander trench and (d) middle of meander trench

**Dry etching process results**

After evaluation the lithography process, a good pattern can be obtained for the subsequent dry etching process. In this experiment, the dry etching equipment is used to etch the polymer dielectric layer. The experimental results are shown in Fig. 7-10.

In the 1st batch for dry etching process, 3 µm photoresist A was utilized for the dry etching process.

From the experimental results shown in Fig. 7(a)-(d), it was found that the trench and vias with 2 µm L/S could be successfully etched. From the cross-section SEM, the top CD of vias is about 1.7 µm and bottom CD of vias is about 1.5 µm. For trench patterns, the top CD is about 2.3 µm and the bottom CD is about 2.1 µm. On the contrary, for the 1 µm L/S trench and 1 µm vias shown in Fig. 8 (a)-(d), it is observed that the etching process stops at the SIN layer, and the polymer underneath has not started etching. The results show that when the photoresist is under-developed or there is some residue, it will block the dry etching effect.

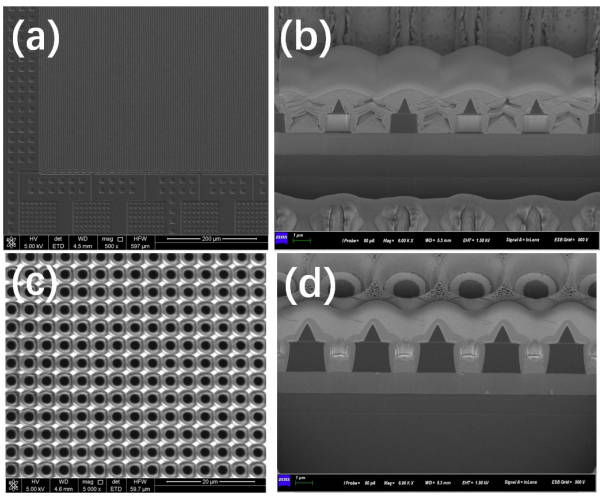


Fig. 7. The SEM images after dry etching process used photoresist A (a) plan view of 2 µm trenches, (b) cross-section view of 1µm trenched, (c) plan view of 1 µm vias and (d) the cross-section view of 2 µm vias

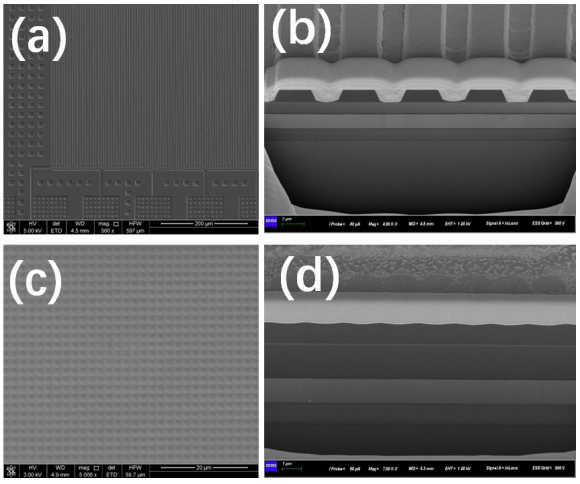


Fig. 8. The SEM images after dry etching process used photoresist A (a) plan view of 1 µm trenches, (b) cross-section view of 1 µm trenched, (c) plan view of 1 µm vias and (d) the cross-section view of 1 µm vias

When using 1.5 µm photoresist B for the dry etching process, it can be observed that 1µm L/S and 1µm vias can be successfully etched. The results are shown in the Fig. 9-10. For the 1 µm L/S trench, the CD obtained is about 1.4 µm, and for the 1 µm vias, the CD obtained is about 1 µm.

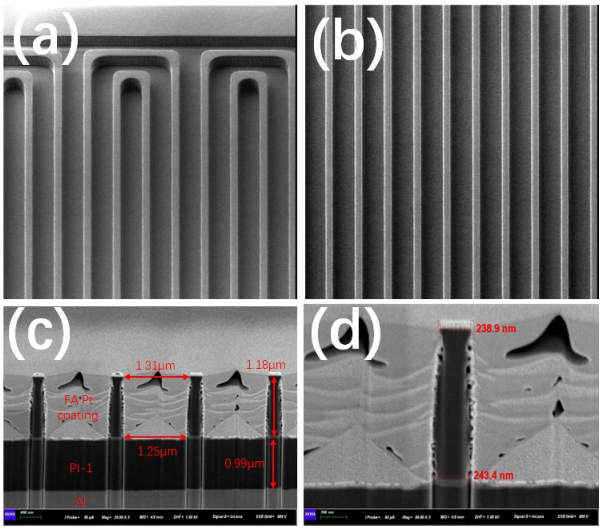


Fig. 9. The SEM images after dry etching process used photoresist B (a) plan view of 1 µm top of meander trench, (b) plan view of 1 µm middle of meander trench, (c) the cross-section view of 1 µm trenches and (d) zoom in the cross-section view of 1 µm trenches

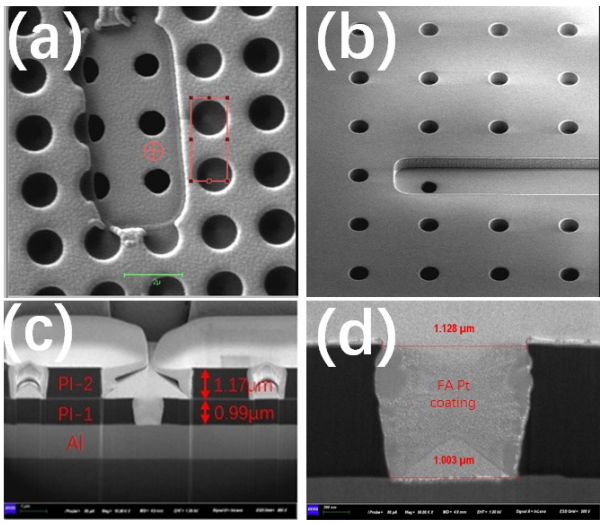


Fig. 10. Plan view (a)-(b) and cross-section view (c)-(d) of 1 µm CD vias

## Conclusions

We have successfully demonstrated the dry etching of 1 µm L/S trench and 1 µm vias CD on two layers of polymer dielectric material with 1.5 µm photoresist using dual damascene process. In addition, the results of RDL of plating and some electrical measurements will be shown at the conference.


## Acknowledgments

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