# A Compact Wafer-Level Heterogeneously Integrated Scalable Optical Transceiver for Data Centers

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***Abstract*— We present a compact heterogeneously integrated optical transceiver package with very low interconnect loss for hyper-scale data center applications realized through 300mm wafer-level packaging. It facilitates the integration of various electronic and photonic components, each independently optimized through diverse technologies, within a unified package platform.**

***Keywords- Optical Transceivers, Hyperscale Data Centers, High-performance computing, Silicon photonics, Heterogeneous Integration, 2.5D, 3D packaging, , Optical Engine, Fan-out wafer-level packaging, Electronic Photonic Package.***

## I. INTRODUCTION

As data-intensive applications grow, there's a consistent rise in data center traffic pushing the need for greater data rates and bandwidth [1, 2]. The primary elements managing data center traffic include switches and optical transceivers, which facilitate the conversion of optical data to electrical data (and vice versa). Contrary to switch capacity, the scalability of optical transceivers does not correspond with semiconductor process technology. Consequently, a gap exists between the two, necessitating enhancements in power efficiency, performance, form factor, and cost for optical transceivers to bridge this disparity. The existing optical interconnect solutions, Optical Pluggable Modules that assemble different discrete transceiver components on PCB board, lack the capacity to scale to support future data rate demands. This necessitates the development of advanced packaging for Silicon Photonics to form co-packaged optics systems [3-5].

To support higher data rates per channel and increased number of high-speed channels, innovative scalable electrical and optical integration strategies that effectively manage signal integrity are required. For high-performance optical transceivers, it's crucial to utilize heterogeneous integration that allows for closer positioning of electronic and photonic components, reducing interconnect loss at high frequencies.

In this work, an electronic-photonic heterogeneously integrated transceiver module or Optical Engine (OE) that is realized by advanced Fan-out wafer-level packaging (FOWLP). In contrast to a monolithic integration that incorporates electrical and optical components utilizing a common foundry process, the proposed method cost-effectively integrates individually optimized discrete components such as silicon photonics IC (PIC), electronic ICs (EICs) and III-V semiconductor material laser source. This work focuses on the design and fabrication of an OE.

## II. CHARACTERISTICS OF THE OE

The fully-integrated, compact module, measuring 8.3mm x 13mm, incorporates a PIC and several EICs. The PIC is embedded within the epoxy mold compound (EMC), together with pre-designed and fabricated through mold interconnects using a 300mm wafer reconstitution molding process. These vias, standing at 300 µm tall, bridge the front and back redistribution layers (RDL) and these RDL layers facilitate connectivity between the PIC and EICs as well as to the substrate or PCB. The package comprises two frontside RDL metal layers and one backside RDL metal layer. This package utilizes 6µm thick metal with a line/space of 30µm/30µm, and our facility is capable of achieving a fine-pitch RDL with a line/space of 1µm/1µm in FOWLP. The embedded PIC features optical elements including Mach Zehnder modulators, waveguides for light signal transmission, high-speed photodetectors and spot size converters for coupling the light to external optical I/O through edge coupling. There are two driver ICs and two Transimpedance amplifier ICs (TIA), supporting 4 channels each to drive the modulators and amplify the signals from photodetectors in the PIC. In addition, there are four DFB laser diodes as light sources and their corresponding driver ICs. The TIA and Driver ICs are flipchip assembled onto the surface of the frontside RDL through a microbump solder joint while the laser diodes are bonded inside cavities provided on the PIC. The wafer-level integration strategy ensures the preservation of vital PIC sections, like the laser diode cavity and edge coupler optical I/O trench. A tailored silicon buffer structure is utilized to safeguard the optical coupling structures of the PIC from contamination and damage during molding process for chip reconstitution. Figures 1a and 1b depict the floor plan and cross-sectional schematic, respectively, of the OE package.

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## III. Package Design Optimizations

In order to optimize the high-frequency electrical performance of interconnects between the components and to the PCB substrate, simulation studies are conducted. Package interconnects are designed such that a shortest path is formed with minimal transitions between EIC and PIC to reduce the frequency-dependent insertion loss. During the design phase, modelling is also conducted to predict the mechanical characteristics of the package to ensure they meet the specified criteria.

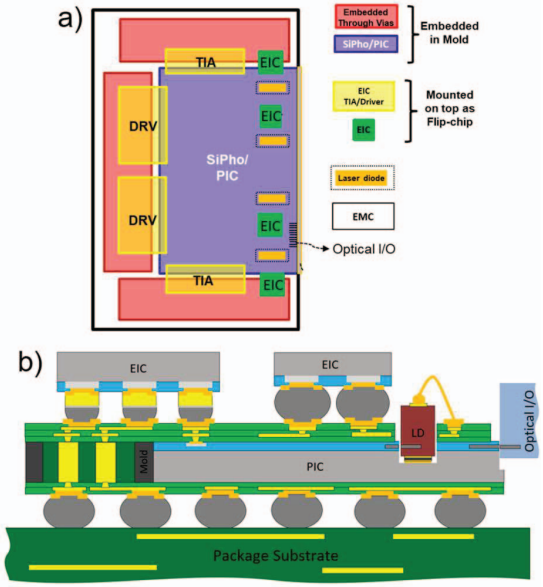


Fig. 1. a) The layout floor plan design of the optical engine package. b) The cross-sectional schematic diagram of the optical engine.

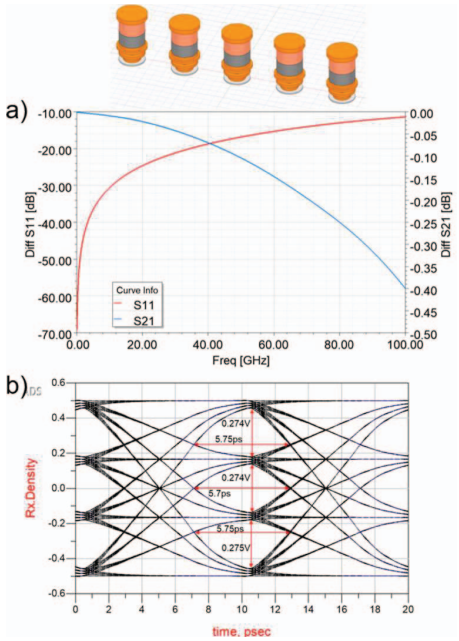


Fig. 2. a) Frequency response of the interconnections linking the EIC to the PIC b) and its 200Gbps PAM4 Eye diagram.

The RF signals are routed from the front side to the backside of package through RDL metal layers and through mold interconnects. Engineered with minimal propagation loss, the high-speed signal interconnects between the EIC and PIC enable high data rates. The EIC and PIC are connected in such a manner that the shortest path is established by aligning the micro bumps of the EICs directly over the modulator or PD pads on the PIC. Simulations were done in ANSYS HFSS and the Fig. 2. shows the 3D model, frequency response and 200Gbps PAM4 Eye diagram of the interconnects between EIC and PIC. The input/output pads of both EIC and PIC chips are in GSGSG configuration with a pad pitch of 125 µm. With the EIC flip-chip attached on top of PIC, direct vertical connections between EIC and PIC are achieved through uBump, UBM, two layers of RDL, and micro-vias. The RDL metal has a thickness of 6 µm while vias have a thickness of 10 µm. A good return loss of more than 10dB is simulated from DC to 100GHz. Additionally, insertion losses of -0.04dB and -0.13dB are simulated at 28GHz and 56GHz, respectively.

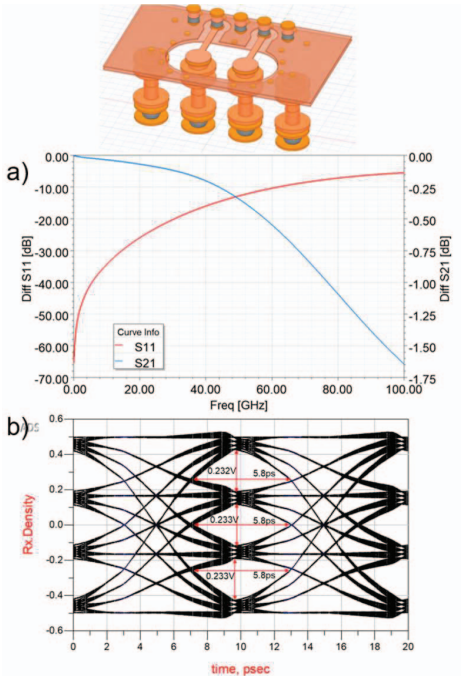


Fig. 3. a) Frequency response of the interconnections from EIC to package substrate and b) 200Gbps PAM4 Eye diagram.

Figure. 3. shows the interconnects for the input/output of OE routing from EIC to package substrate through uBump, frontside RDL, through mold interconnects, and C4 bumps. The uBumps have a GSGSG configuration with a pitch of 125 µm following EIC chip pads. Through mold interconnects and C4 bumps are in GSSG configuration with a pitch of 250 µm. Frontside RDL layers are ground planes with antipads and gaps etched out for the signal routing. Two ground layers are connected through micro-vias. Signal lines with a width of 32 µm and length of 300 µm on top RDL are to connect uBump and through mold interconnects. Figure. 3a. shows the differential S-parameters simulated from DC to 100GHz.

Return loss of better than 10dB is maintained from DC to 60GHz. Simulated insertion losses of -0.11dB and -0.46dB are observed at 28GHz and 56GHz, respectively.

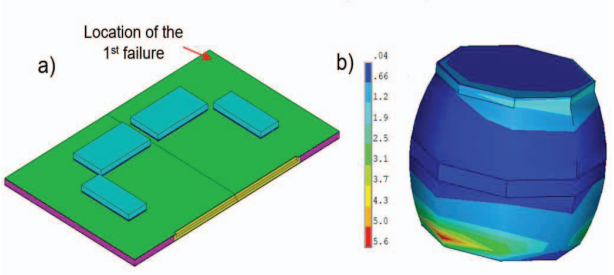


Fig. 4. a) Schematic showing the location of the 1st failure c4 bump underneath the package. b) Strain energy Density (MPa) Plot in solder bump.

A thermo-mechanical Finite Element Analysis (FEA) model is developed for the package to predict mechanical characteristics. The anticipated warpage of the OE package is under 25 µm. The reliability of the C4 solder joint between the OE package and the substrate is assessed via the model (Fig. 4). After subjecting the assembly to temperature cycling tests ranging from -40ºC to 125ºC, with a cycle duration of 1 hour, the predicted solder joint fatigue life is 4471 cycles.

## IV. Packaging and Assembly

A chip-first FOWLP process flow is utilized for the integration of the OE package. The main stages in the package processing are illustrated in Fig. 5. It commences with the reconstitution of the molded wafer using discrete silicon photonics chiplets and pre-fabricated through-mold vias. Initially, both the PICs and through-mold via interconnects based on build-up substrates are positioned with its face down on the mold plate with thermal release tape, followed by compression molding for encapsulation. A segment of the molded wafer is shown in Fig. 6a. Following the molding process, the measured warpage of the wafers is less than 400 µm (refer to Fig. 7). Process optimizations, such as the assessment of a molding tape with lower adhesive strength, were conducted to attain contamination-free cavities on PIC surface.

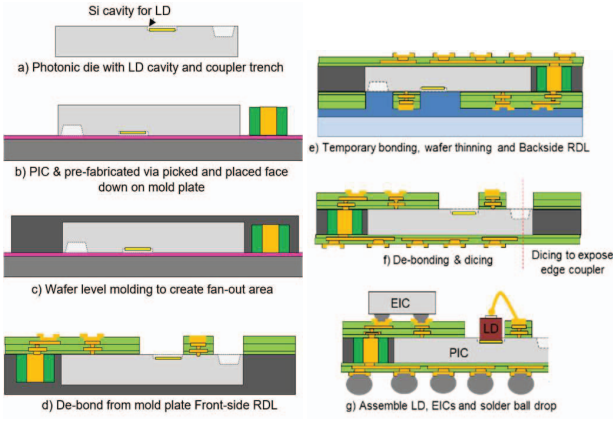


Fig. 5. The steps for integrating the optical engine package.

Once reconstituted, the wafers are detached from the mold plate and proceed to undergo processing for front-side RDL metal, Under Bump Metallization (UBM), and dielectric layers (Fig 6c). The front side features two metal layers for routing, along with a UBM layer containing exposed bond pads used for bonding the EICs. Because of the complex topology of photonic ICs, achieving a conformal dielectric layer and preventing material ingress into PIC cavities pose challenges in using liquid-based dielectric and photoresist materials. Therefore, dry film-based dielectric and photoresist material lamination process is optimized during front-side dielectric, RDL, and UBM formation. This approach ensures the creation of a uniform dielectric layer in the mold area, particularly within narrow gaps between PIC and adjacent embedded structures, enabling continuous RDL formation without breaks.

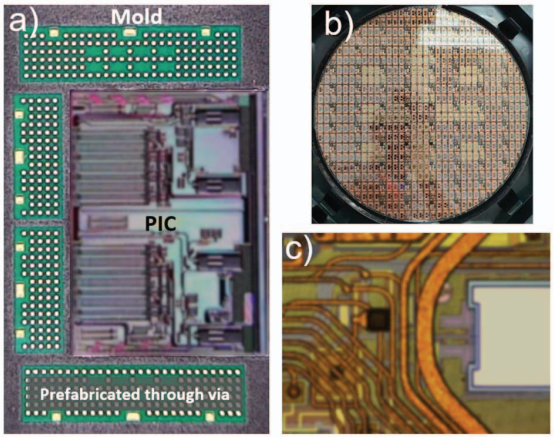


Fig. 6. a) Reconstituted wafer post-molding, with the PIC and pre-fabricated through-mold interconnects encapsulated within the mold compound. b) A fully processed reconstituted 300mm wafer. c) A section of the package's front side showcasing the formed multiple metal RDL traces.

Following the front-side RDL processing, the wafer thickness is decreased to 300 µm via a back grinding process before advancing to back-side RDL processing (Fig. 8a). To facilitate this, the wafer is bonded to a temporary carrier wafer. The backside RDL comprises one metal layer for routing and UBM pads for dropping c4 solder balls. Following this, the wafer is diced along the deep trenches to expose the edge optical I/Os prior to assembly with laser diodes, EICs and solder balls (Fig. 8c). Cross-sectional views of the package and its components are visible in Fig. 9.

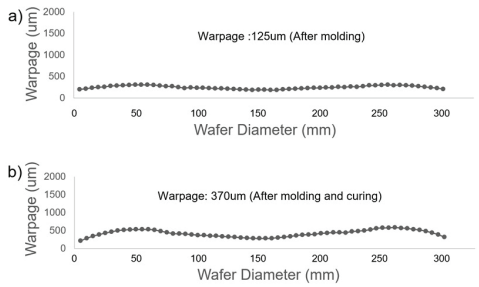


Fig. 7. Wafer warpage plot following the molding processes a) after reconstitution and molding b) after curing.

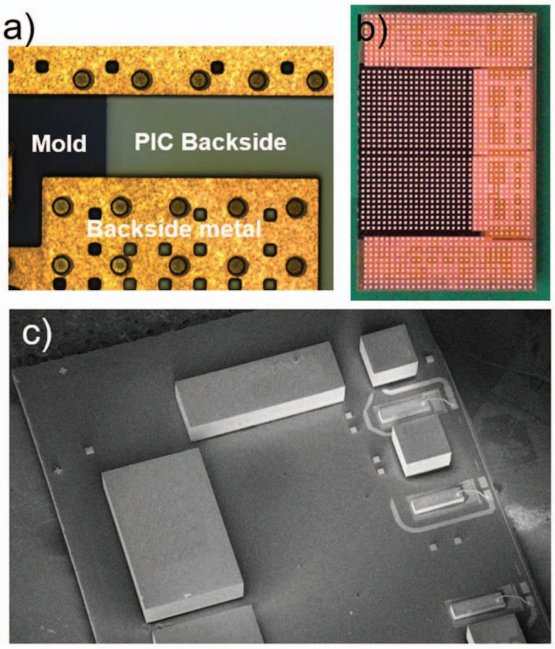


Fig. 8. a) Package backside RDL on thinned down interposer. b) OE package backside after c4 ball drop. c) Image showing Laser Diodes inside cavity with wire bond.

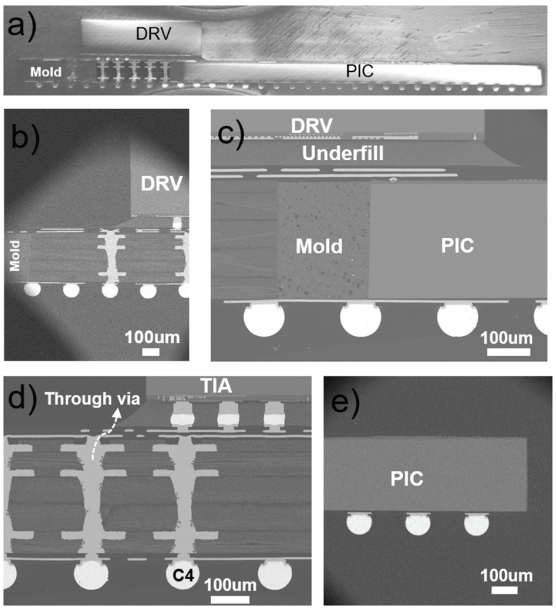


Fig. 9. Cross-sections of the OE package a) An overview cross-section displaying the embedded PIC and through-mold interconnects within the mold, with the driver electronic IC flip-chipped on the surface. b, c, d, e) Magnified cross-sectional images showing different package components and their interfaces.

The finalized OE packages (Fig. 10a) are subsequently assembled onto the substrate (Fig. 10b) along with additional components such as DSPs and PLCs before undergoing functional testing. In previous works [6-8], we have demonstrated similar process integration platforms to enable electronic-photonic integration.

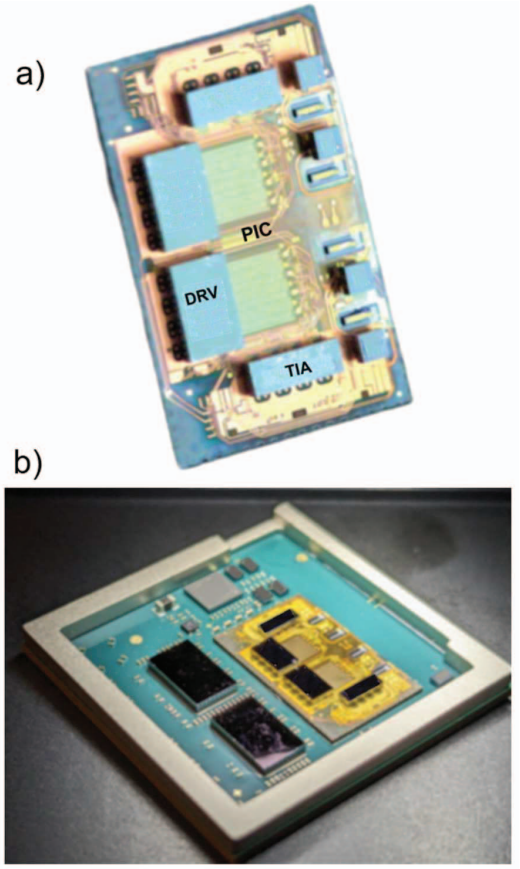


Fig. 10. a) Fully integrated Optical Engine package, b) Optical Engine assembled on substrate with DSP and other components.

## V. Testing

To facilitate the measurement of the performance of the high-speed carrying interconnects, separate test structures were designed and fabricated without PIC or EIC silicon chips. As the electromagnetic (EM) fields are tightly confined within the vertical interconnects and RDL structures, the presence of these chips is insignificant. Figure 11 shows the 3D model of through mold interconnects connecting to top frontside metal layers through stacked vias in GSSG configuration. The structure was measured using double-side probing with FormFactor GSGSG ACP probes with a probe pitch of 150 µm. Figure. 11a. compares the measured and simulated differential return loss and insertion loss where dotted lines are the measured results while solid lines are the simulation results. A good return loss of more than 20dB was measured from DC to 40GHz. At 28GHz, differential insertion loss of -0.12dB was measured. The eye diagram for 100Gbps PAM4 signals is shown in Fig. 11b. The diagrams are generated in Keysight ADS channel simulator with the measured 4-port S-parameters imported. There is no pre-emphasis or equalization added at Tx or Rx.

The rise/fall time at Tx was set to 5ps and the load impedance at Rx was set to 100Ohm. As shown in the figure, clear eye openings can be observed for the interconnects.

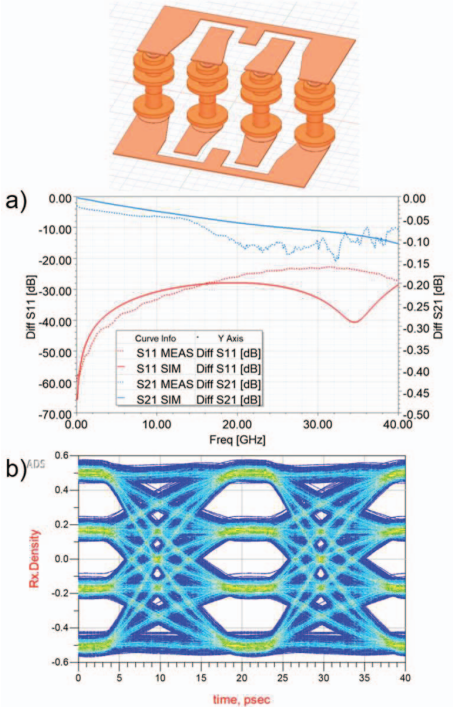


Fig. 11. a) simulated and measured results of through mold interconnects and RDL and b) corresponding 100Gbps PAM4 eye diagram.

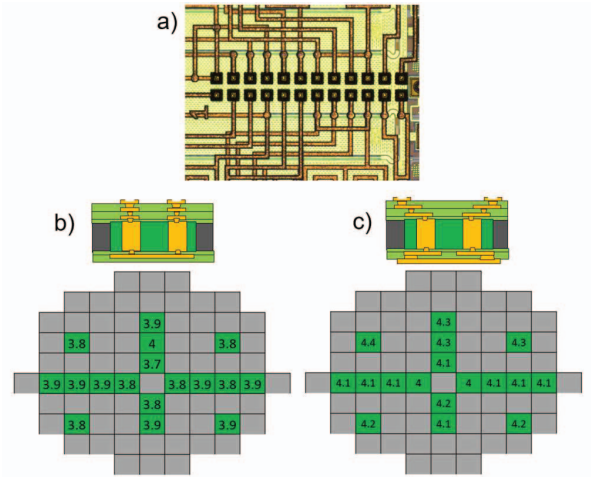


Fig. 12. a) 2x12 bond pads used for testing the electrical continuity of various package interconnect daisy chains at the wafer level. Wafer-level test results of daisy chains linking the front-side UBM, RDL metal layers connected to backside RDL metal traces through prefabricated mold vias in a b) stacked via , and in a c) staggered via configuration. Numbers inside the box indicate the resistance of the daisy chain in ohms.

To ensure the integrity of the integration process concerning electrical continuity, metal interconnect daisy chain structures are implemented within the OE fanout interposer. These daisy chains interconnect various package elements, including front-side RDL metal traces, micro vias, through-mold interconnects, and backside RDL metal traces. To streamline the testing process at the wafer level, specialized probing structures featuring a 2x12 pad configuration are integrated on both sides of the interposer. Using an automated test equipment system (V93K, Advantest Pte Ltd) for Multi-channel SoC testing in conjunction with a wafer prober enables comprehensive testing of all daisy chains for continuity. Analysis of the test results validates that all daisy chains maintain uninterrupted connectivity, with no detected open defects. Some of the results of wafer level interconnect continuity test are shown in Fig. 12. After full integration, the package's warpage is measured at less than 25 µm, aligning well with modelling predictions and ensuring no negative effects on subsequent assembly processes.

## VI. Conclusions

The demonstrated wafer-level processed, heterogeneously integrated platform paves the way for higher-speed, scalable optical transceivers. It eliminates the need for discrete component assembly and removes signal disruptions like those in wire bonds, leading to enhanced signal performance. The package's high-speed interconnects, linking EICs to PIC, showcase an impressively low insertion loss of less than 0.05dB at 28GHz. Interconnects from EIC to the substrate register below 0.4dB at 28GHz in which the vertical through package via insertion loss is measured at under 0.2dB at 28GHz and below 0.5dB at 56GHz. As a result, the package interconnect is capable of supporting high-speed signals exceeding 100Gbps. This platform can be further expanded by integrating with larger ASICs, such as switches or GPUs, making it ideal for high-performance computing and hyper-scale data center applications.

## Acknowledgment

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