Development of 4 die stack module using Hybrid bonding approach

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***Abstract*— Die stacking is commonly used in memory modules. Solder micro-bumps and through silicon via (TSVs) are common interconnects, and it may not viable or suitable for device that has bump pitch 10µm or below. Solder interconnects have issues related to brittle intermetallic compound, solder cracked, solder merging, and long duration process if local thermos-compression bonding is adopted.**

Hybrid Bonding is an attractive approach for die stacking as it can eliminate all the issues of solder interconnects. However, it involves other issues such as stringent surface morphology, demands in high surface's cleanliness, and the need for high temperature annealing process. In this work, we developed processes such as Cu and organic/inorganic dielectrics CMP, Temporary bonding & de-bonding, Damascene Cu process on temporary carrier bonded wafers, and particle free dicing required for chip stacking using Chip-to-Chip/Chip-to-Wafer (C2C/C2W) hybrid bonding. We also demonstrated 4 die stack module using C2C/C2W hybrid bonding approach.

Keywords-Hybrid bonding; chip to wafer bonding; die stacking; Cu dishing; surface roughness

I. INTRODUCTION

Multi-die stack is adopted vigorously by industry to enable multi-functional module with small form factor [1, 2]. The communication between the dies is accomplished by having Through Silicon Via (TSV) in the dies except for the top-most die. Further form factor and performance enhancement are achieved by using hybrid bonding instead of solder bonding. Solder material has issues such as solder merging and voids created by interdiffusion [3, 4, 5] at finer pitch <20µm. Hybrid bonding with oxide-to-oxide bonding or polymer to oxide bonding helps to eliminate these solder related issues and push the interconnect pitch down to below 10µm.

Hybrid bonding involves bringing two very flat surfaces together at low or room temperature and formed a very strong bonding interface between them. The subsequent annealing process at elevated temperature allowed the Cu material to expand and inter-fused together to form the Cu-Cu interconnects. Typical surface roughness of the bonding surface needs to be ~ 0.3nm with ~5nm Cu dishing and particles free surfaces are required to achieve good bonding. Die stacking using hybrid bonding brings another challenge to the bonding process. It must ensure the top side of the bonded unit is clean enough and flat enough to accept the subsequent die to stack on top of each other [6].

Die stacking needs to take care of the surface's condition of the die that was tacked on the wafer and the top surface of the die should be ready for the subsequent die tacking. The passivation's material must be friendly to the adhesive used in TBDB process. In this work, we had evaluated different dielectric materials for die stacking and demonstrated the 4-dies stack module using chip-to-wafer hybrid bonding approach and optimized processes.

II. INFORMATION OF THE TEST VEHICLES

The 4-dies stack module consist of three daisy chain test dies of 50µm and the top die of 100µm thickness. The daisy chain test die size is of 6x13mm. One side of the die's passivation is of silicon oxide (TEOS) and the other side is either polymer or SiCN material. Polymer passivation has the advantage of more particles tolerant and less stringent on surface roughness as compared to oxide or SiCN material. Figure 1 shows the schematic of the 4 die stack module. The Cu pad diameter is 5µm at 10µm pitch. Total number of Cu pads in the memory die is 737,526. Through silicon via (TSV) was fabricated on the 1st three dies and the diameter of TSV is 4.5µm.

Table 1 tabulated the information of the test vehicle. Daisy chain structures are incorporated in the test vehicle to allow measurement of the individual daisy chain connection for die 1, 2, 3 & 4. This allows identification of the failure site in the failure analysis.

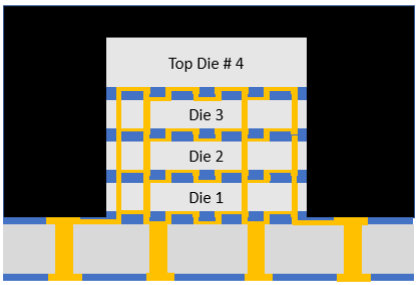

Figure 1: Schematic of 4 die stack module

Table 1: Information of test Vehicle

Description	Information
Memory test die size	6 x 13mm
Interposer size	15 x 18mm
Die 1 to 3 thickness	50µm
Die 4 thickness	100µm
Interposer thickness	50µm
Cu Pad diameter	5µm
Cu Pad Pitch	10µm
Total number of pads	737,526
TSV diameter	4.5µm

III. FABRICATION PROCESS FOR MEMORY DIE WITH TSV

The memory daisy chain test die with TSV was fabricated using TSV first approach whereby the TSVs were formed on the silicon wafer before the front side metal pads and re-route distribution line (RDL) are fabricated using Cu damascene process. The oxide and Cu pad's surface undergo chemical mechanical polishing (CMP) process optimization to achieve the desired oxide roughness and Cu dishing. This is followed by temporary bonding of a carrier wafer using adhesive layer for the thin wafer handling during the subsequent backside processes such as thinning, TSV via revealing, passivation deposition, patterning and CMP to fabricate the backside metallization. The 50µm thin memory die with TSV and double hybrid bond pads was formed by debonding the carrier wafer and clean the adhesive from memory test wafer frontside. The fabrication process for the memory die with TSV and double side hybrid bond pads is illustrated in Figure 2.

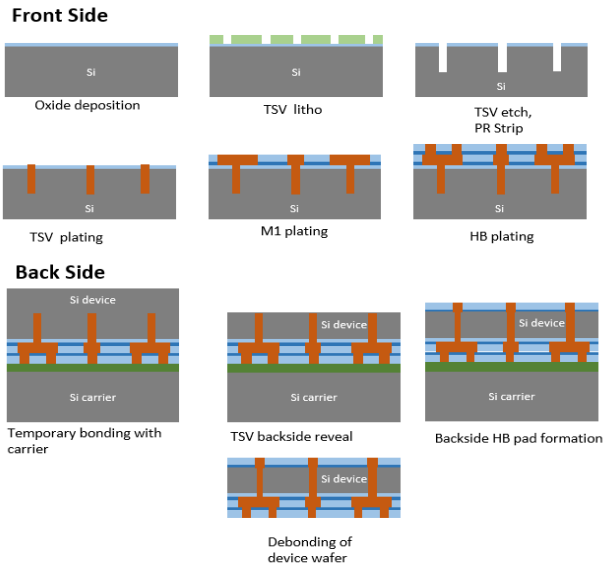

Fig 2: Fabrication Process for Memory die with TSV

IV. FABRICATION PROCESS FOR TOP MEMORY DIE

The top memory daisy chain die without TSV was fabricated using Cu damascene process. The fabrication process starts with depositing silicon nitride and oxide layer before lithography patterning of the photo resist. The silicon oxide was etched away before plating the Cu layer and CMP, followed by subsequent patterning and etching process for hybrid bond pad formation. The top surface undergoes CMP process to achieve the desired roughness and Cu dishing. The fabrication process for the top memory die without TSV is illustrated in Figure 3.

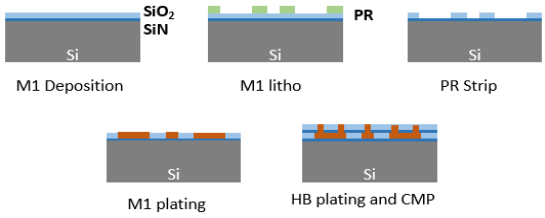

Fig 3: Fabrication Process for top Memory die

V. CHEMICAL MECHANICAL POLISHING

The surface of the die is of upmost importance as hybrid bonding demands very smooth surface and the Cu dishing is directly responsible for the formation of Cu-to-Cu joint. Chemical Mechanical Polishing (CMP) is used to prepare the surface of the die to achieve surface roughness of oxide below 0.2nm and Cu dishing below 5nm. The hardness and modulus of Silicon Oxide, SiCN and Polymer are different and thus the CMP process has been optimized separately to achieved good results. Figure 4 shows the AFM image of the die's surface indicating the oxide's roughness is ~0.2nm and Cu dishing ~ 5nm. Figure 5 shows the AFM image of the die's surface indicating SiCN's roughness ~0.3nm and Cu dishing ~ 2nm. Die with polymer passivation was having higher surface's roughness ~ 5nm and deeper Cu dishing ~ 20nm as showed in Figure 6. Surface roughness of polymer may not need to be the same level as oxide as it is more softer than oxide and thus it may be able to achieve good bond on oxide passivation. High Cu dishing is of major concern as it may not be able to form good Cu-Cu joints. CMP process has also been optimized for the wafers with polymer and Cu pads to achieve the Cu protrusion of 5 to 7nm as shown in Figure 7.

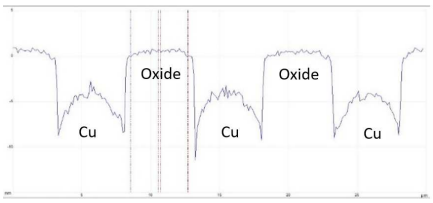

Figure 4: AFM image for die with oxide and cu pad

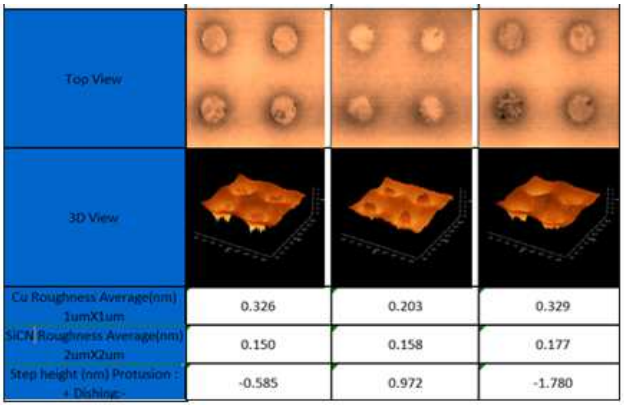

Figure 5: AFM scan images for die with SiCN and Cu Pad

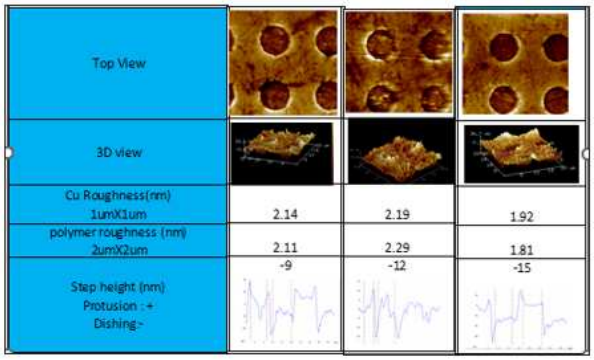

Figure 6: AFM scan images for die with Polymer and Cu Pad

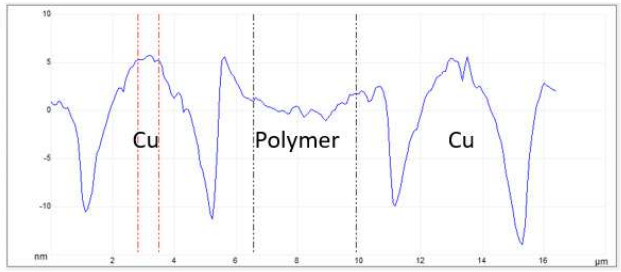

Figure 7: AFM scan showing Cu protrusion of 5 to 7nm

VI. Die Stacking Process Flow

The wafer was diced using protective layers during the discing process [7]. The protective layer was stripped after the dicing process. It was proven that the yield of the diced wafer improved from 10% to 90% with the protective layer. Particles on the die's surface will cause poor hybrid bonding quality. The singulated dies were subjected to plasma and DI water clean prior to pick up and place on the bottom interposer wafer that was also treated by plasma and DI water rinse. The whole process is illustrated in Figure 8.

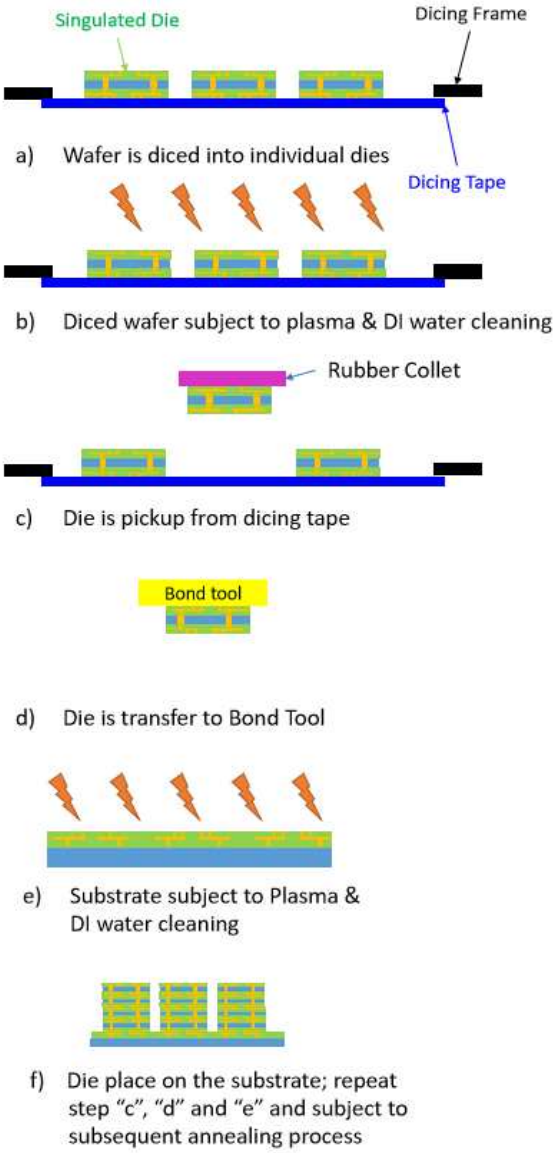

Figure 7: Chip to wafer bonding for 4-dies stack module

VII. "Oxide to Oxide" Chip to Chip Bonding Evaluation

Chip to chip bonding was initially carried out to identify potential issues before moving to chip to wafer bonding. The chip was bonded on the substrate using 30N for 10sec at room temperature. The bonded samples were subjected to CSAM. CSAM images as shown in Figure 9 indicate good bonding only at the centre of the die. The edges of the die suffered from poor bonding. Further analysis on the singulated dies indicated that the dicing process is the main cause of this failure. Step profiling at the area near to the saw street revealed that there was metal protrusion along the saw streets as shown in Figure 10, and this could be the

reason for the poor bonding quality at die edge area. The dicing process was optimization using two steps cut to eliminate the metal protrusion at saw street.

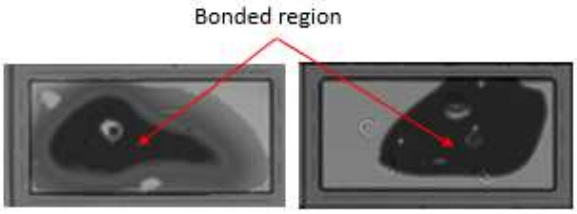

Figure 9: CSAM image for bonded units

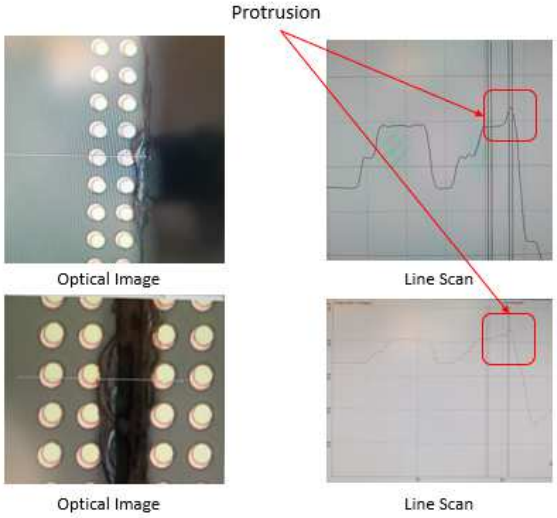

Figure 10: Optical image and line scan along saw street

VIII. "POLYMER TO OXIDE" CHIP TO CHIP BONDING EVALUATION

Two polymers from different supplier were evaluated. The bonding quality of polymer on oxide was evaluated initially by using blanket passivation before moving on to die with passivation and Cu pads. The blanket polymer die of 3x3x0.775mm was bonded on blanket oxide die of 8x8x0.775mm using bonding force range from 10 to 50N for duration of 3sec, followed by annealing at 300ºC for 1hr in the case of Polymer 1. The CSAM and die shear test has been carried out to study the bond interface integrity. The bonding parameters used for this chip-to-chip bonding study are tabulated in Table 2 and bonded samples shown in Figure 11. Dies with polymer 2 were tacked on the 8x15x0.775mm substrate with oxide passivation using force range from 50 to 100N, temperature range from 300 to 250C while maintaining the substrate's temperature at 150C. Table 3 tabulated the bonding parameters used for polymer 2.

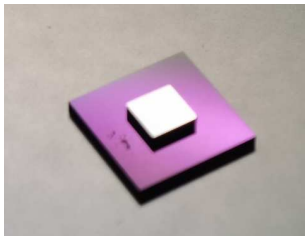

Figure 11: Chip to Chip Bonded Sample

Table 2: Parameters for "Polymer 1 to Oxide" chip to chip bonding study

No	Chuck T (ºC)	Bond T (ºC)	Bond force (N)	Bond Time (s)
1	25	25	10	3
2	25	25	30	3
3	25	25	50	3

Table 3: Parameters for "Polymer 2 to Oxide" chip to chip bonding study

No	Chuck T (ºC)	Bond T (ºC)	Bond force (N)	Bond Time (s)
1	150	300	100	5
2	150	300	100	3
3	150	350	100	3
4	150	300	50	5
5	150	300	50	3
6	150	300	50	3

CSAM analysis done on both polymer 1 & 2 bonded samples indicated good bonding interface without any voids or delamination as shown in Figure 12. The shear strength registered more than 20MPa with failure mode of silicon cracked which is comparable to oxide-oxide shear strength for both polymer 1 & 2.

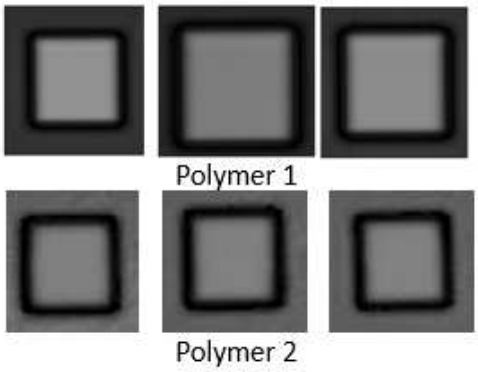

Figure 12: CSAM images for the "Polymer on Oxide" bonded dies for both polymer 1 & 2

The 6x13x0.05mm die with Cu pads and one side polymer 1, another side oxide passivation was bonded on

the bottom substrate with oxide passivation and Cu pads as shown in Figure 13. Die tacking study has been carried out by varying bond temperature ranges from 35ºC up to 300ºC, bond force ranges from 50N to 100N together with 3 sec bond time and chuck set at room temperature for die with polymer 1. Die with polymer 2 tacking study involves bond temperature range from 100 to 350C with force from 30 to 150N for 3sec with chuck set at room temperature.

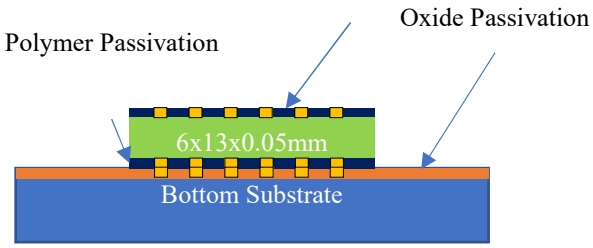

Figure 13: Schematic diagram of polymer die on oxide substrate

The die with polymer 1 tacking process DOE parameters and tacking test results are tabulated in Table 4. Tacking between the polymer 1 and oxide was successful for bonding with elevated temperature at and above 200ºC as show in Figure 14. The bonding temperature needs to be above or near the glass transition temperature of the polymer in order to bond successfully on the oxide passivation. The 4-dies stack module was subjected to annealing at 250ºC for 2hrs to enable Cu-Cu joint.

Table 4: Bonding result for polymer 1 on oxide passivation

Run	Chuck T (ºC)	Bond T (ºC)	Bond force (N)	Bond Time (s)	Results
1	25	35	50	3	Not bonded
2	25	35	100	3	Not bonded
3	25	100	50	3	Not bonded
4	25	100	100	3	Not bonded
5	25	100	100	3	Not bonded
6	25	150	100	3	Not bonded
7	25	200	100	3	Bonded
8	25	250	100	3	Bonded
9	25	300	100	3	Bonded

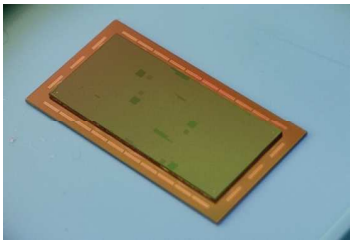

Figure 14: 4-die stack module with “Polymer 1” bonded on “Oxide” passivation with Cu Pads.

X-section illustrated the interconnects for all four dies as shown in Figure 15. There is miss-alignment of the bottom die to the substrate which can be corrected further in the bonding process.

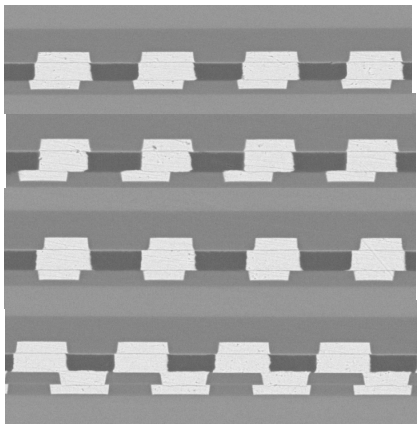

Figure 15: X section image of 4 die stack module

The die with polymer 2 tacking DOE results is tabulated in Table 5. Tacking between the polymer 2 and oxide passivation was successful with elevated temperature for both bond tool and chuck as shown in Figure 16.

Table 5: Bonding result for polymer 2 on oxide passivation

Run	Chuck T (ºC)	Bond T (ºC)	Bond force (N)	Bond Time (s)	Results
1	25	100	30	3	Not bonded
2	25	100	100	3	Not bonded
3	25	100	150	3	Not bonded
4	25	200	100	3	Not bonded
5	25	200	150	3	Bonded
6	25	250	150	3	Bonded
7	25	300	150	3	Bonded

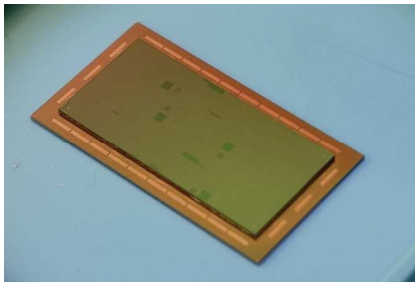

Figure 16: 4-die stack module with “Polymer 2” bonded on “Oxide” passivation with Cu Pads.

IX. “SiCN to Oxide” Chip to Wafer Bonding Evaluation

The bonding quality of SiCN passivation on SiCN and oxide passivation was study using blanket passivated dies

and also with Cu pads. The blanket SiCN wafer is diced into 3x3x0.775mm. The individual SiCN blanket die was bonded on the oxide wafer with force of 10N for 3 sec followed by annealing at 350ºC for 3hours. Die shear test was conducted to check whether it can achieve similar bonding strength of oxide-to-oxide bonding ~ 20MPa. Figure 17 shows the wafer populated with SiCN dies.

The die (6x6x0.2mm) with Cu pad was prepared with SiCN passivation and bonded on wafer with oxide passivation at force of 20N/3sec. X section was done to reveal the Cu-Cu interface between the die and the wafer.

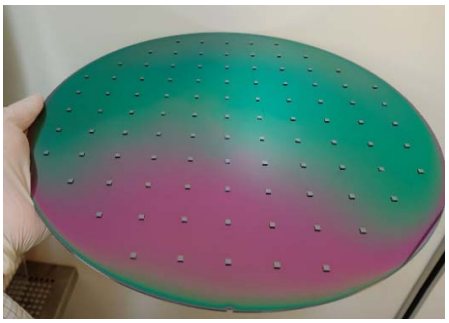

Figure 17: Image of SiCN dies on Oxide Wafer

Shear test was conducted on bonded SiCN blanket dies on wafer with oxide passivation and the results are tabulated in Table 6. The silicon die cracked during the shear test, and this indicated good bonding quality as it exhibits silicon fracture strength. Figure 18 shows the image of the bonded unit after the shear test. The average shear strength of 29MPa is comparable to oxide to oxide shear strength.

Table 6: Shear Strength of SICN to Oxide bonded Units

No	N/mm2
1	25.39155
2	27.33938
3	20.4593
4	27.18787
5	36.85617
6	37.94617
Average	29.19674

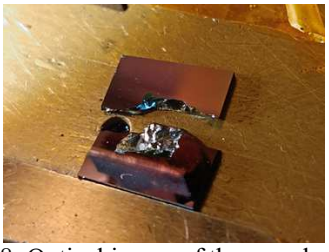

Figure 18: Optical image of the sample after shear test

The die with Cu pad and SiCN passivation was tacked successfully on the wafer with SiCN passivation as shown in Figure 19. Figure 20 showed the cross-section that indicated good Cu-Cu interface was achieved with SiCN-on-SiCN bonding configuration. These results indicated SiCN passivation is possible for the double side passivation of the stacked dies.

Figure 19: SiCN dies with Cu Pad tacked on SiCN wafer

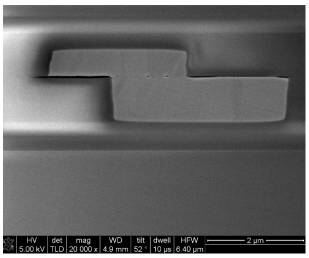

Figure 20: Good Cu-Cu interface for SiCN die bonded on wafer with SiCN passivation

The SiCN dies with Cu pad was tacked successfully on wafer with oxide passivation as shown in Figure 21. The X - section image as shown in Figure 22 indicated good Cu-Cu interface. This indicated that SiCN passivation is a good candidate for subsequent die stacking configuration with SiCN on backside of the die and Oxide on front side of the die.

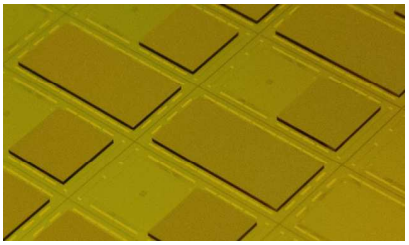

Figure 21: SiCN dies with Cu pad tacked on wafer with oxide passivation

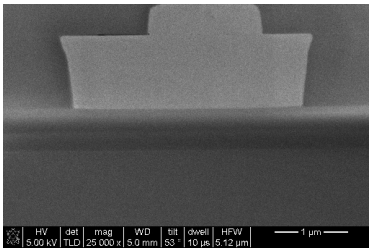

Figure 22: X Section of SiCN dies on wafer with oxide passivation

X. DIE TO WAFER STACKING EXPERIMENT

The dies with polymer and oxide passivation were tacked directly to the bottom wafer after both the diced wafer and bottom wafer were subjected to plasma and DI water treatment. Bonding force of 200N for 30sec with bonding temperature of 100ºC; 150ºC, 200ºC & 300C were tested out. 4-dies stack modules were bonded successfully with bonding temperature set at 200ºC for die with polymer 1 and at 300C for die with polymer 2 as show in Figure 23. Table 7 tabulated the results for the various bonding parameters.

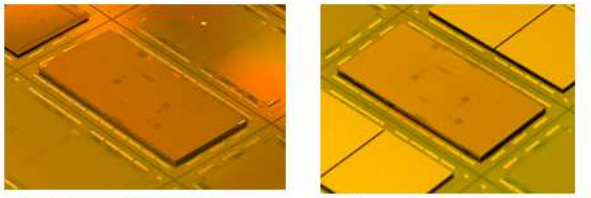

Figure 23: 4-dies stack module on wafer with Polymer 1 & Oxide bonding interface

Table 7: Bonding Results for Die with "Polymer and Oxide"

No	Chuck T (ºC)	Bond T (ºC)	Bond force (N)	Time (sec)	Bonding Results for Polymer 1	Bonding Results for Polymer 2
1	25	100	200	30	No bond	No bond
2	25	150	200	30	No bond	No bond
3	25	200	200	30	Bonded	No bond
4	25	300	200	30	-	Bonded

XI. SUMMARIES

This paper presented optimized wafer fabrication processes required for C2W hybrid bonding. CMP, wafer dicing and cleaning/surface activation are critical processes to achieve desired surface roughness & dishing, and clean surface respectively to achieve good hybrid bonding. Low temperature dielectric materials need to be selected for Cu damascene process on bonded wafers due to thermal budget limitation of TBDB materials used for thin wafer handling. We have demonstrated a 4-dies stack module using C2C/C2W hybrid bonding approach with the following findings.

(a) The dicing process should ensure no delamination or metal protrusion along the dicing edge and particle free surface as it impacts the quality of the bonding
(b) CMP process was optimized to achieve the desired surface roughness <0.3nm and Cu dishing <5nm.
(c) SiCN and Polymer passivation are the viable material on backside of the bonded wafers for the die stacking
(d) Polymer tacking is successful with elevated bonding temperature and able to tack the dies and further optimization is required to improve the die stack connectivity.

XII. ACKNOWLEDGMENT

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