Mechanistic Insight and Demonstration of Antiferroelectric-Gated Enhancement-Mode GaN HEMTs

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***Abstract*— This work presents mechanistic insight into polarization-assisted charge trapping in GaN HEMTs and demonstrates an enhancement-mode (e-mode) device employing an antiferroelectric (AFE) $Hf_{0.2}Zr_{0.8}O_2$ gate stack (AFE-HEMT). The AFE gate stack, featuring enhanced charge-trapping capability and zero remnant polarization (P_r), allows complete utilization of trapped electrons for channel depletion, resulting in a stronger positive threshold voltage (V_{TH}) shift compared with the ferroelectric (FE) gate stack. The AFE-HEMT achieves a V_{TH} of 1.9 V, with a maximum drain current (I_{D_MAX}) of 481 mA/mm and an on-resistance (R_{ON}) of 7.4 Ω·mm. Incorporating a floating gate structure (AFE-FG-HEMT) further enhances V_{TH} to 2.7 V with an R_{ON} of 6.5 Ω·mm, significantly improves charge retention, and yields negligible V_{TH} shift during positive bias stress, demonstrating a compelling pathway toward stable, normally-off GaN power devices.**

***Index Terms*— E-mode GaN HEMT, charge trapping, ferroelectricity and anti-ferroelectricity**

Enhancement-mode (e-mode) GaN HEMTs are critical for next-generation power electronics, offering intrinsic normally-off behavior for improved safety, simplified gate drive design, and reduced standby power consumption [1]. However, conventional GaN HEMTs are inherently depletion-mode (d-mode) due to the strong polarization-induced 2DEG at the heterojunction [2]. Achieving robust and scalable GaN HEMTs with true e-mode operation remains a key challenge. Several approaches have been explored to achieve e-mode behavior, including p-GaN gate [3], [4], recessed gate [5-8], and charge trapping layer (CTL) technology [9-12]. Among these, CTL-based approaches have gained attention for their tunability and compatibility with planar device processing. In addition to employing high-k materials as the blocking layer, the integration of nonlinear dielectrics (e.g. FE and AFE) can enhance charge injection [13-18]. While FE gate stacks—particularly doped HfO_2-based dielectrics (e.g. FE-HZO)—have attracted attention for their CMOS compatibility and scalability, the AFE-HZO gate stack offers unique benefits, including higher saturation polarization (P_s), larger dielectric constant, stronger depolarization effect, and minimal P_r, making it a highly promising candidate for e-mode GaN HEMTs.

In this work, we propose and demonstrate an e-mode AFE-HEMT incorporating AFE $Hf_{0.2}Zr_{0.8}O_2$. The working mechanism of AFE/FE-gated HEMTs is analysed in detail via band diagram and load-line analysis, supported by experimental validation. The results clearly showcase that AFE-HZO facilitates enhanced electron trapping, effectively depleting the 2DEG and achieving stable e-mode operation. This approach offers an alternative path for threshold control in GaN HEMTs, overcoming drawbacks of FE gate stacks.

As illustrated in Fig. 1, both AFE and FE gate stacks utilize polarization-assisted charge trapping to modulate V_{TH}. The switching mechanism of FE-FETs involving charge trapping has been investigated and is applicable to GaN HEMT [19-20]. During initialization, polarization of the HZO layer enhances electron injection and trapping at the HZO/Al_2O_3 interface in both AFE and FE devices, which can be qualitatively described using load-line analysis. The transistor load line shifts toward P_s (green dot) with the indication of charge trapping [Fig. 1(a) and (d)].

After initialization, the device behavior diverges. In FE-HZO, a large P_r persists. When trapped charge (Q_{Trap}) is insufficient to compensate P_r, the residual polarization field attracts electrons to the channel, shifting V_{TH} negatively. In the load line plot, the transistor load line shifts left after initialization, and the intersection point (light blue) between the transistor load line and the Q–V characteristic of the FE layer, which represents $Q_{FE} = Q_{Trap}$, lies below 0 V, indicating d-mode behaviour of the FE HEMT as shown in Fig. 1(b).

In contrast, the AFE-HZO gate stack exhibits a stronger depolarization effect. At V_{GS} = 0 V, Q_{Trap} exceeds Q_{AFE}, effectively repelling the 2DEG, leading to a strong positive shift in V_{TH}. The load line plot also shows that the intersection between the transistor load line and the AFE Q–V characteristic occurs at a positive voltage (light blue point), corresponding to enhancement-mode operation [Fig. 1(e)]. Moreover, the AFE phase of HZO generally exhibits a higher P_s and a larger dielectric constant than its FE counterpart, enabling enhanced charge injection, making AFE-HZO inherently more suitable for charge-trapping-induced e-mode operation in GaN HEMTs.

Although the negative V_{TH} shift in FE-gated GaN HEMTs agrees with several prior studies [21-23], there are studies showing positive V_{TH} shifts that cannot be fully explained by the conventional mechanisms. From the above analysis, the key distinction lies in the depolarization behavior after removal of the external bias, which determines whether the trapped charges can effectively dominate. By intentionally enhancing depolarization in FE gate stack, the post-initialization Q_{FE} can be reduced, achieving an AFE-like positive V_{TH} shift. For instance, introducing dielectric layers in the FE gate stack can enhance depolarization and suppress P_r [12]. The engineered FE case shows more noticeable depolarization effect, resulting in Q_{Trap} exceeding Q_{FE} after initialization, achieving e-mode operation as illustrated in Fig. 1(c). However, FE gate stacks intrinsically exhibit weaker depolarization than AFE counterparts. Excessive depolarization engineering effectively drives the FE state toward AFE behavior, further highlighting that AFE is inherently better suited for polarization-assisted charge trapping in GaN HEMTs.

To verify this work mechanism, AFE-HEMT was fabricated. The GaN-on-Si HEMT structure consists of 2 nm GaN capping layer, 7 nm InAlN barrier layer, 200 nm un-doped GaN, a thick buffer layer, and an 8-inch high-resistivity Si substrate. The schematic cross section of AFE-HEMT device is illustrated in Fig. 2(a). The gate stack consists of 4 nm Al_2O_3 dielectric layer, 10 nm AFE $Hf_{0.2}Zr_{0.8}O_2$ layer, and conventional

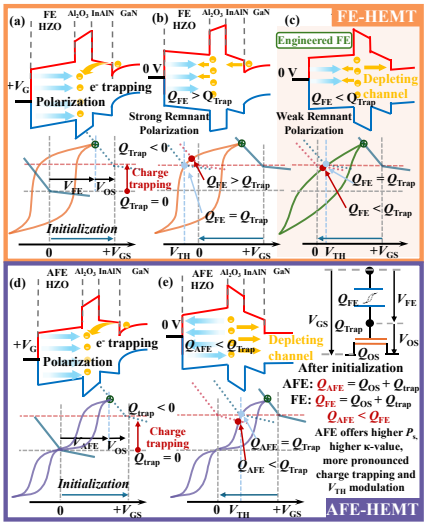

Fig. 1. Mechanism illustration of FE and AFE gate stacks with energy band diagram and load line analysis. During initialization, both (a) FE and (d) AFE gate stacks are polarized, enhancing electron injection. After initialization, (b) in conventional FE-HZO, V_{TH} shifts negatively as P_r is higher than trapped charges. (c) Only with engineered FE gate stack which has stronger depolarization effect can the device show positive shift in V_{TH}. (e) However, AFE-HZO device shows a positive V_{TH} attributed to the lower P_r.

Ni/Au gate metal. The gate region is precisely recess etched to enhance the threshold voltage and increase electron tunneling probability from 2DEG into the HZO/Al_2O_3 interface, facilitating charge trapping and positive V_{TH} shift [8].

The key fabrication steps are summarized in Fig. 2(b). The process begins with standard surface cleaning, followed by patterning of the source/drain (S/D) regions. A low-power inductively coupled plasma (ICP) etch using BCl_3/Cl_2 was performed to recess 5 nm of the barrier layer at S/D regions. A Ti/Al/Ni/Au metal stack was then deposited via e-beam evaporation and subjected to rapid thermal annealing at 600 °C for 30 s, forming ohmic contacts with a low contact resistance of 0.28 Ω·mm [24]. Subsequently, the gate region was patterned using electron beam lithography (EBL) and a gate recess etch was performed using ICP to remove 7.5 nm of the barrier layer, followed by mesa patterning and etching. Atomic layer deposition (ALD) was performed to deposit 4 nm Al_2O_3 and 10 nm $Hf_{0.2}Zr_{0.8}O_2$ at 250 °C. The gate electrode was then patterned and formed by Ni/Au deposition and liftoff. Finally, a post-metal annealing (PMA) step was conducted at 500 °C for 1 min to activate the AFE layer. For comparison, FE-HEMTs were fabricated with the same process flow using 10 nm FE $Hf_{0.5}Zr_{0.5}O_2$ film deposited at 300 °C by ALD. The FE or AFE behavior of HZO originates from its crystalline phase composition. Lower Zr content favors stabilization of the non-centrosymmetric orthorhombic phase, resulting in ferroelectric behavior, whereas higher Zr content promotes the tetragonal phase, leading to antiferroelectric behavior through a field-induced phase transition. A PMA step is required to crystallize the HZO film, introducing stress and activate the desired phase composition. Fig. 2(c) and (d) show cross-sectional HRTEM

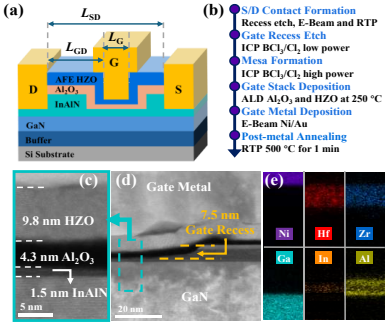

Fig. 2. (a) AFE-HEMT schematic diagram and (b) key process flow. (c) and (d) are the cross-sectional TEM images of AFE-HEMT gate region. (e) EDX elemental mapping shows distinct layers, suggesting no diffusion of atoms after PMA.

images of the gate region, confirming the thicknesses of Al_2O_3, HZO, and remaining barrier layers. EDX elemental mapping verifies distinct interfaces without atomic diffusion after PMA [Fig. 2(e)].

The antiferroelectric behavior of the $Hf_{0.2}Zr_{0.8}O_2$ thin film was evaluated using capacitance-voltage (C–V) and polarization-voltage (P–V) measurements on metal–ferroelectric–metal (MFM) capacitors. Fig. 3(a) presents the C–V characteristics under two voltage sweep ranges (±3 V and ±3.5 V) for samples subjected to PMA at 500 °C and 600 °C for 1 min. Fig. 3(b) displays the corresponding P–V hysteresis loops for sweep ranges from ±1.5 V to ±3.5 V as the critical field of the ALD-grown AFE-HZO is 4 MV/cm. The pinched hysteresis loops confirm the antiferroelectricity of the $Hf_{0.2}Zr_{0.8}O_2$ layer. The positive P_s and P_r are annotated on the plots. While PMA at 600 °C slightly increases $+P_s$, which is beneficial in charge trapping, it also results in postponed depolarization during voltage ramp-down, as well as larger $+P_r$. In contrast, the sample annealed at 500 °C for 1 min exhibits relatively high $+P_s$, reduced $+P_r$, and improved leakage characteristics. Therefore, 500 °C/1 min PMA was selected as the optimal annealing condition for integration into the AFE-HEMT fabrication process. For comparison, a FE MFM capacitor was fabricated and subjected to the same PMA condition (500 °C, 1 min). As

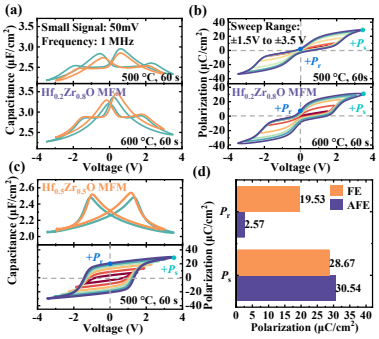

Fig. 3. (a) C-V and (b) P-V measurements of MFM structure with 10 nm AFE-Hf0.2Zr0.8O2 layer activated at different PMA temperatures. (c) C-V and P-V of MFM structure with 10 nm FE-Hf0.5Zr0.5O2 layer activated by PMA at 500 ºC for 1 min. (d) Ps and minimum Pr comparison between FE- and AFE-HZO.

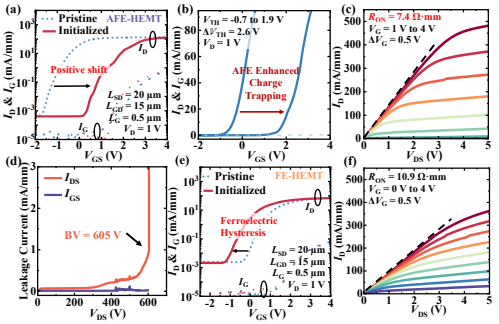

Fig. 4. (a) Log-scale I_D-V_G curves of AFE-HEMT. (b) I_D-V_D curves of initialized AFE-HEMT. (c) I_D-V_D curves of initialized AFE-HEMT. (d)Breakdown voltage of the AFE-HEMT. (e)Log-scale I_D-V_G plots of FE-HEM. (f) I_D-V_D curves of initialized FE-HEMT.

shown in Fig. 3 (c), the FE C–V curve demonstrates a single butterfly-shaped response with a lower overall capacitance compared to the AFE counterpart. The P–V loop exhibits a hysteresis loop with high $+P_r$. A comparison of $+P_s$ and $+P_r$ for AFE and FE capacitors is presented in Fig. 3(d). The AFE capacitor exhibits a higher $+P_s$ and significantly lower $+P_r$.

To explore the effectiveness of polarization on device operation, the DC characteristics of both AFE- and FE-gated HEMTs were evaluated. Both devices feature gate length L_G = 0.5 µm, gate to drain length L_{GD} = 15 µm, and source to drain length L_{SD} = 20 µm. As seen in Fig. 4(a) and (b), a clear positive shift in the I_D-V_G curve, attributed to electron trapping, is observed after initialization at V_{GS} = 5 V. These trapped charges induce a substantial positive threshold voltage shift from -0.7 V to 1.9 V extracted from linear extrapolation method—totaling 2.6 V—converting the device from d-mode to e-mode. The slight subthreshold swing degradation arises from charge loss during measurement due to interface-based trapping in the dielectric. The transconductance (G_M) peak is extracted to be 83.6 mS/mm after initialization at a drain voltage of 1 V. The output characteristics [Fig. 4(c)] reveal excellent current drivability, with I_{D_MAX} reaching 481 mA/mm and R_{ON} as low as 7.4 Ω·mm, demonstrating the effectiveness of AFE-HEMT in achieving normally-off operation with good performance. The breakdown voltage (BV) was defined at 1 mA/mm to reflect hard breakdown caused by source-drain failure, the AFE-HEMT exhibits a BV of 605 V, as shown in Fig. 4(d).

The FE-HEMT displays an anticlockwise hysteresis in I_D-V_{GS} curve [Fig. 4(e)], indicating ferroelectric switching behavior. The device undergoes a negative V_{TH} shift from 0.3 V to −0.9 V. This polarization-induced shift transforms the device into d-mode, which aligns with the conventional FE gate stack working mechanism. In Fig. 4(f), the FE-HEMT demonstrates an I_{D_MAX} of 357 mA/mm and exhibits a higher R_{ON} of 10.9 Ω·mm. Overall, the controlled experiment fully captures the theoretical analysis. The AFE-HEMT achieves a pronounced positive V_{TH} shift as expected, enabling stable e-mode operation with excellent on-current and low on-resistance.

To further enhance charge trapping capacity and retention, a floating gate (FG) structure was employed (AFE-FG-HEMT) through sputtering a 10 nm tungsten (W) layer between the Al_2O_3 and HZO layers. The corresponding band diagram [Fig. 5(a)] shows that electrons are confined within the FG. Compared to interface trap states, the FG structure offers a

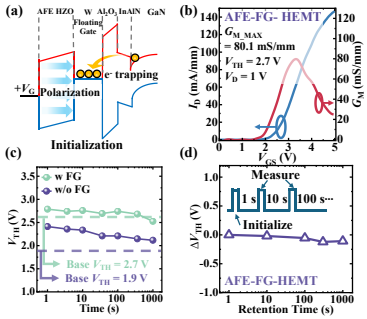

Fig. 5. (a) Band diagram of the AFE-FG-HEMT with floating gate in between Al_2O_3 and $H_{0.2}Z_{0.8}O_2$. Electrons are trapped in the floating gate during initialization. (c) Linear-scale I_D-V_G and G_M plots of AFE-FG-HEMT. (c) Time evolution of V_{TH} for AFE-FG-HEMT and AFE-HEMT under the same PBS test. AFE-FG-HEMT shows much lower V_{TH} shift. (d) Retention test of AFE-FG-HEMT. Stable V_{TH} with less than 120 mV shift is obtained after 1000 s.

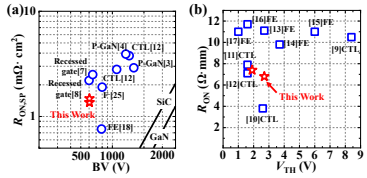

Fig. 6. (a) Benchmark of BV versus $R_{ON,SP}$ for the e-mode GaN devices with different approaches. (b) Benchmark of V_{TH} versus R_{ON} for e-mode GaN HEMT based on charge trapping mechanism, including CTL technique and FE-based HEMTs.

Table I
Benchmark of state-of-the-art E-mode GaN HEMTs with charge trapping mechanism

Ref.	V_{TH} (V)	G_M (mS/mm)	R_{ON} (Ω·mm)	ΔV_{TH} (1000s)
CTL [9]	8.4	30	10.49	—
CTL [10]	2.6	188.8	3.8	-2.2
CTL [11]	1.6	—	7.9	—
CTL [12]	1.6	54	7.1	-0.9
FE [13]	2.7	30	11.1	—
FE [14]	3.7	23	9.8	-0.8
FE [15]	6	142	~11	—
FE [16]	1.6	89.5	11.7	—
FE [17]	1	~90	11	-1
AFE (This work)	1.9/2.7	83.6/80.1	7.4/6.8	-0.12

larger trap density and suppresses de-trapping effects, enabling a larger V_{TH} shift and improved retention characteristics.

Electrical characterization results are presented in Fig. 5(b). Under the same initialization bias of V_{GS} = 5 V, the AFE-FG-HEMT exhibits a further V_{TH} shift to 2.7 V while maintaining a high G_{M_MAX} of 80.1 mS/mm, suggesting enhanced trapping is achieved with minimal mobility degradation.

The reliability was assessed using the positive bias stress (PBS) test. For PBS test, devices were stressed at V_{GS} = 5 V for 1000 s after initialization. During the stress, pulsed I-V measurements were performed to extract V_{TH}. The results are plotted in Fig. 5(c). The device with floating gate structure exhibits much smaller V_{TH} shift compared with devices without floating gate. This confirms minimal trapping/de-trapping and stable device behaviour. exposure. Retention was further evaluated by monitoring V_{TH} without bias after initialization [Fig. 5(d)]. The AFE-FG-HEMT demonstrates excellent

retention, with less than 0.12 V of V_{TH} drift (ΔV_{TH}) over 1000 s. These results reveal that the FG design effectively stabilizes V_{TH} over time, making the AFE-FG-HEMT a promising and robust device for long-term e-mode power application.

Fig. 6(a) summarizes the e-mode GaN devices achieved via different approaches, providing a benchmark of specific on-resistance ($R_{ON,SP}$) versus breakdown voltage metric [3], [4], [7], [8], [12], [18], [25]. Fig. 6(b) and Table I benchmark the device performance with the state-of-the-art e-mode GaN HEMTs with charge trapping mechanism including CTL and FE gate stacks [9-17]. Our devices demonstrate a relatively high V_{TH}, low R_{ON}, and stable reliability characteristics, showcasing the potential of e-mode GaN HEMT with AFE gate stack for power applications.

In conclusion, this work presents mechanism insights and the demonstration of an e-mode GaN HEMT utilizing AFE gate stack. The proposed AFE-HEMT achieves effective charge trapping, enabling robust normally-off operation, while AFE-FG-HEMT further enhances the reliability, offering a promising pathway toward reliable and scalable e-mode GaN power devices.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

DATA AVAILABILITY

The data that support the findings of this study are available within this article.

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