GaN-on-Si HEMTs for Low Voltage FR2 Applications Enabled by Reactive-Sputtered n^{++}-GaN Ohmic Contacts

Yihao Zhuang, Siyu Liu, Qingyun Xie, Hanlin Xie, Tomita Kazuyoshi, Tetsu Kachi, Hiroshi Amano, Subramaniam Arulkumaran, and Geok Ing Ng

***Abstract*—This letter reports GaN-on-Si high-electron-mobility-transistors (HEMTs) employing reactive-sputtered Ge-doped n^{++}-GaN ohmic contacts for low-voltage FR2 applications. A low sputtered n^{++}-GaN/2DEG interfacial resistance of 0.06 Ω·mm is achieved for the InAlN/GaN heterostructure. The transistor achieves a low on-resistance of 0.91 Ω·mm and a maximum drain current of 2.03 A/mm, resulting in excellent output power of 0.51, 1.25, and 2.44 W/mm at V_{DS} = 3, 5, and 8 V at 28 GHz, respectively. These results demonstrate the strong potential of RF GaN HEMTs employing sputtered n^{++}-GaN ohmic contacts.**

***Index Terms*—InAlN/GaN, sputtered ohmic contacts, RF HEMT, low voltage operation, FR2.**

I. Introduction

The FR2 user equipment market, covering 5G mm-wave bands such as n258 (24.25–27.5 GHz), n260 (37–40 GHz), and n261 (27.5–28.35 GHz), represents a tremendous opportunity for GaN-on-Si HEMTs, owing to their high power, high efficiency, large-scale manufacturability, and low cost [1], [2]. However, such applications typically require low supply voltages (<10 V), making efficient operation a critical challenge for wide-bandgap semiconductors, as device performance is strongly constrained by on-resistance (R_{on}). Thus, it is necessary to introduce advanced device technologies, including high electron density heterostructures [3], [4] and regrown ohmic contacts which reduce parasitic resistance [5], [6], [7].

To achieve low contact resistance (R_c), regrown ohmic contact techniques based on molecular beam epitaxy (MBE) and metal-organic chemical vapor deposition (MOCVD) have been widely used, achieving contact resistances below 0.2 Ω·mm [6], [8], [9], [10], [11], [12], [13]. Although MBE-regrown n-GaN typically offers higher Si dopant concentration and improved uniformity [14], [15], [16], its low growth rate and limited wafer size restrict throughput and scalability. In contrast, MOCVD supports large-wafer processing but suffers from Si dopant incorporation limitations due to heavy compensation effects [17], [18]. Furthermore, both approaches generally require temperatures exceeding 750 °C [9], introducing additional challenges for process integration. Recently, low-resistivity sputtered n-GaN has been successfully deposited using sputtering systems [19], [20], [21], and pulsed-sputtered n-GaN with Si-doping has been demonstrated for ohmic contacts on AlGaN/GaN heterostructures [22], indicating its promise for GaN HEMTs. Sputtered n-GaN has also offered low resistance ohmic contacts with higher achievable concentration, higher deposition rate, lower cost and low temperature deposition, which align well with the requirement for reduced R_{on} in low-voltage GaN-on-Si HEMTs. However, the integration of such a technique in RF GaN HEMTs has not yet been demonstrated.

This work demonstrates the use of reactive-sputtered Ge-doped n^{++}-GaN ohmic contacts for the InAlN/GaN heterostructure, and its integration in an RF GaN HEMT. Ge doping (in this work, 1.9×10^{21} cm^{-3}) enables higher doping concentrations than conventional Si doped n-GaN. The characterized transistor achieved low R_{on} of 0.91 Ω·mm and a high $I_{D,max}$ > 2 A/mm, even with a relatively large source-drain distance (L_{SD}) of 2.5 µm. Excellent saturated output power (P_{sat}) was achieved at 3 to 8 V at 28 GHz. These results demonstrate the strong potential of reactive-sputtered Ge-doped n^{++}GaN ohmic contacts for low voltage RF transistors.

II. Fabrication and Ohmic Characterization

The designed GaN-on-Si HEMT structure is presented in Fig. 1. The epitaxial stack, from top to bottom, consists of a 2 nm

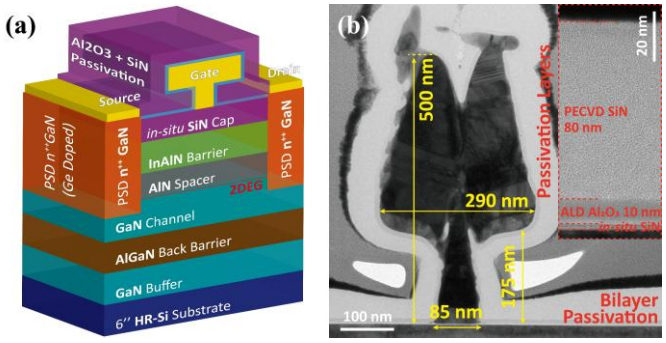

Fig. 1. InAlN/GaN-on-Si HEMTs employing reactive-sputtered n^{++}-GaN ohmic contacts. (a) Schematic of the designed device structure. (b) Transmission electron microscopy (TEM) image of the T-gate and passivation.

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SiN cap, a 7 nm InAlN barrier, a 2 nm AlN spacer, an 80 nm GaN channel, a 250 nm AlGaN back barrier (BB), and a C-doped GaN buffer grown on high-resistivity Si (111) substrate (5 kΩ·cm) by MOCVD. The combination of a thin GaN channel and an AlGaN back barrier provides strong electron confinement, effectively suppressing short-channel effects and mitigating trapping effects originating from the buffer [23]. Hall measurements indicate a carrier sheet density (N_s) of 2.26×10^{13} cm^{-2}, electron mobility (μ) of 1442 cm^2/V·s, and sheet resistance (R_{sh}) of 190 Ω/sq. The devices feature a source-drain distance (L_{SD}) of 2.5 µm (n^{++}-GaN to n^{++}-GaN), a π-shaped gate-feed configuration with a total gate width (W_g) of (2×16) µm, and a gate length (L_g) of 85 nm. The gate-edge-to-source n^{++}-GaN spacing (L_{gs}) is designed to be 1 µm. The contact metal is separated by 1 µm from the edges of the n^{++}-GaN regions in all characterized patterns.

The device fabrication flow is illustrated in Fig. 2(a). The ohmic region was recessed by 50 nm using Cl_2-based inductively coupled plasma reactive ion etching (ICP-RIE). After cleaning by organic solvents, an SC-2 (HCl/H_2O_2) pretreatment for conducted for 5 min. 80 nm Ge-doped n^{++}-GaN was grown at 600 °C at a rate of 6.3 nm/min in a radical-enhanced reactive sputtering system [20]. Each source was sputtered with an Ar gas plasma generated by a DC or RF generator. The sputtered Ga and Ge particles, along with N radical source, reached the substrate surface and underwent chemical reactions. As shown in Fig. 2(b), a clear boundary between the polycrystalline and deposited crystalline GaN regions could be observed. 25% tetramethylammonium hydroxide (TMAH) solution was used to selectively etch the polycrystalline GaN at room temperature, followed by a short, buffered oxide etch (BOE) treatment to remove the regrowth hard mask while minimizing damage to the *in-situ* SiN cap layer, which serves directly as the gate dielectric in the MIS-gate structure. Preserving the integrity of the in-situ SiN layer effectively suppresses interface-state-induced trapping effects.

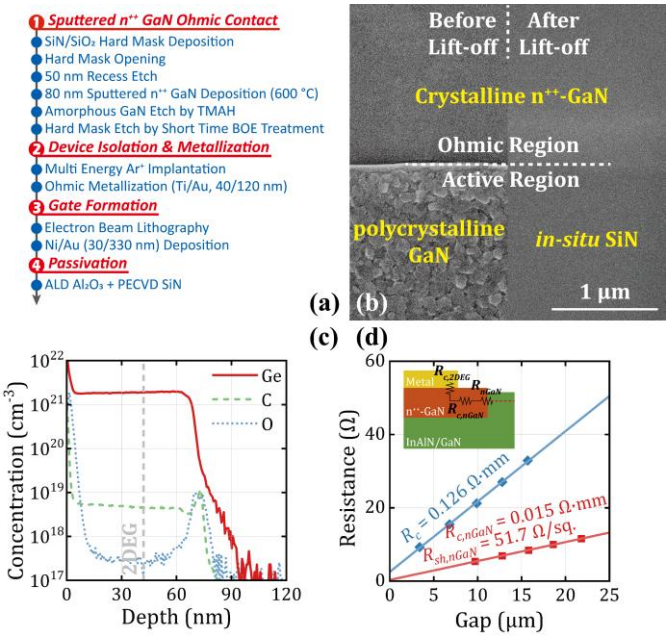

Fig. 2. (a) Fabrication process of the InAlN/GaN-on-Si HEMTs with sputtered n^{++}-GaN regrown ohmic contacts. (b) Scanning electron microscopy (SEM) image of the boundary between active and ohmic regions before and after lift-off. (c) Element concentrations in the n^{++}-GaN region from SIMS. (d) TLM measurements on both HEMT structure and regrown n^{++}-GaN, which indicate an n^{++}-GaN/2DEG interfacial resistance of 0.06 Ω·mm.

TABLE I
RF GaN-HEMTs using regrown and sputtered GaN ohmic contacts

Barrier	Method	Dopant	$R_{c,nGaN}$ (Ω·mm)	$R_{sh,nGaN}$ (Ω/sq)	$R_{c,2DEG}$ (Ω·mm)	Affiliation
InAlN	Sputter	Ge	0.02	51	0.06	This Work
AlGaN	PSD	Si	0.06	8	0.21	U Tokyo '24 [22]
InAlN	MBE	Si	0.05	99	-	Cornell '20 [9]
InAlN	MBE	Si	0.06	67	0.08	Notre Dame '12 [8]
InAlN	MOCVD	Si	0.04	142	0.11	CAS '21 [34]
InAlN	MOCVD	Si	0.05	31	0.1	Xidian '23 [11]
InAlN	MOCVD	Si	-	90	0.04	IMEC '24 [34]
InAlN	MOCVD	Si	0.02	190	0.02	IMEC '25 [13]
AlN	MOCVD	Si	0.02	100	-	
AlGaN	MOCVD	Ge	0.08	-	0.05	Panasonic '16 [35]
AlN	MBE	Si	0.03	81	0.06	Xidian '23 [10]

*The data were extracted according to the reported values, where available.

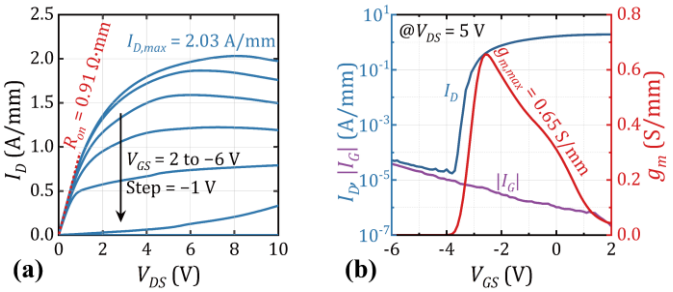

Fig. 3. DC characteristics of a transistor with L_g = 85 nm, L_{SD} = 2.5 µm, and W_g = 2×16 µm. (a) Output I_D-V_{DS} characteristics. (b) Transfer I_D (g_m)-V_{GS} characteristics.

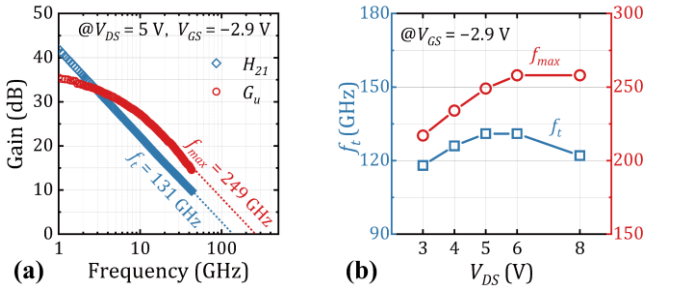

Fig. 4. (a) Small-signal performance, showing f_t/f_{max} = 131/249 GHz (after de-embedding) at V_{DS} = 5 V. (b) Dependency of f_t/f_{max} on V_{DS}. The data were measured after TRL calibration and de-embedded using on-wafer open and short patterns.

An average Ge doping concentration of 1.9×10^{21} cm^{-3} was obtained in the sputtered n^{++}-GaN, according to secondary-ion mass spectrometry (SIMS) (Fig. 2(c)). This doping concentration resulted in a carrier concentration of 2.1×10^{20} cm^{-3}, characterized by Hall measurement. Based on transfer length method (TLM) performed on HEMT structure and n^{++}-GaN (Fig. 2(d)), the total contact resistance (R_c) of 0.126 Ω·mm, the n^{++}-GaN/Metal interfacial resistance ($R_{c,nGaN}$) of 0.015 Ω·mm, and the n^{++}-GaN sheet resistance ($R_{sh,nGaN}$) of 51.7 Ω/sq. were extracted. The lateral resistance within the n^{++}-GaN layer (R_{nGaN}) is calculated as 0.052 Ω·mm based on the measured sheet resistance and the designed spacing. By subtracting $R_{c,nGaN}$ and R_{nGaN} from the total R_c, the n^{++}-GaN/2DEG interfacial resistance ($R_{c,2DEG}$) is extracted to be 0.059 Ω·mm. The extracted R_{sh} from TLM measurements is 191 Ω/sq, which

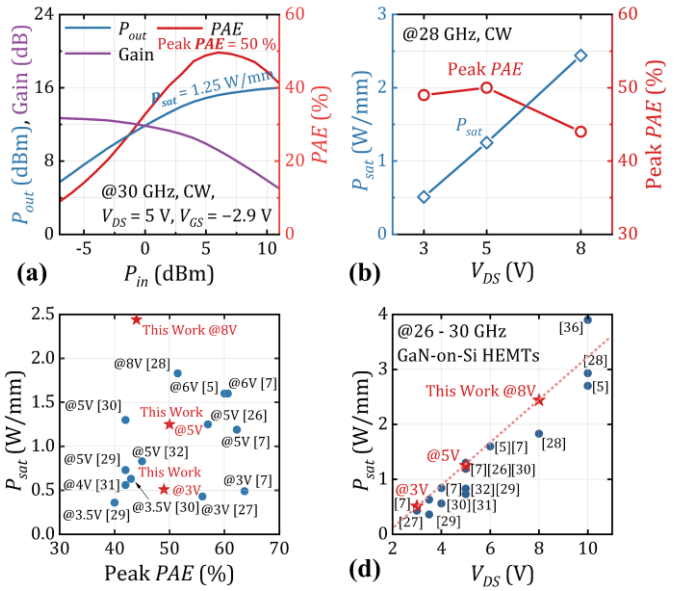

Fig. 5. Power performance of the characterized device at 28 GHz. (a) Power sweep at V_{DS} = 5 V. (b) P_{sat} and peak *PAE vs.* V_{DS} ranging from 3 to 8 V. Benchmark of the fabricated device with other GaN-on-Si HEMTs at 26−30 GHz. (c) P_{sat} *vs.* peak *PAE*. (d) P_{sat} *vs.* V_{DS}. This work achieves excellent P_{sat} across the benchmarked range of V_{DS}.

is consistent with Hall measurements performed on the as-grown wafer, indicating that the low-temperature sputtering process introduces negligible degradation to the heterojunction quality. Additionally, TLM measurements conducted before and after heating up to 500 K exhibit consistent characteristics, indicating stable and recoverable behavior without permanent degradation at elevated temperatures.

The performance of the sputtered GaN ohmic contacts was benchmarked with other RF InAlN/GaN HEMTs using regrown ohmic contacts in Table I. Reactive-sputtered n^{++}-GaN achieves low contact resistance at both interfaces and $R_{sh,nGaN}$, comparable to typical values obtained using MBE or MOCVD. The reactive sputtering deposition achieved the highest doping concentration and lowest deposition temperature among the reported techniques, while ensuring competitive ohmic contacts at a fast deposition rate. Although $R_{c,2DEG}$ is relatively low compared with reported values, it can be further reduced toward the theoretical limit (0.017 Ω·mm) defined by the single-interface quantum injection limit [14], [24] by employing damage-free atomic layer etching (ALE) and improved surface recovery treatments.

III. Results and Discussion

As shown in Fig. 3(a)–(b), $I_{D,max}$ of 2.03 A/mm, low R_{on} of 0.91 Ω·mm, and g_{mmax} of 0.65 S/mm were achieved despite the large L_{SD}, thanks to the Ge-doped reactive-sputtered n^{++}-GaN ohmic contacts and InAlN/GaN epitaxial structure. The MIS-gate structure with the well-preserved in-situ SiN as dielectric and vertically scaled structure enabled good gate control, therefore achieving low leakage and high on/off ratio >1.0×10^5 (Fig. 3(b)). To further evaluate trapping effects and validate the effectiveness of the preserved in-situ SiN cap layer and the additional ex-situ bilayer passivation, pulsed I–V measurements were performed. The device exhibits a current collapse of 5% and 23% for the gate-lag ($V_{GS,Q}$, $V_{DS,Q}$) = (-5, 0) V and both lag ($V_{GS,Q}$, $V_{DS,Q}$) = (-5,10) V, respectively. The observation of f_{max} > 200 GHz even at V_{DS} = 3 V is indicating the strong potential of the fabricated transistor for low-voltage FR2 applications (Fig. 4(c)–(d)).

Load-pull measurements were performed at 28 GHz using passive tuners under continuous-wave mode, with V_{DS} ≤8 V. The device was biased at V_{GS} = −2.9 V (corresponding to the peak f_{max}) and was tuned for optimum power. At V_{DS} = 5 (3) V, a peak *PAE* of 50 (49) % with an associated output power (P_{out}) of 0.66 (0.26) W/mm was achieved, as shown in Fig. 5(a). And a saturated output power (P_{sat}) of 1.25 W/mm (0.51 W/mm) with associated PAE value of 41% (32%) was obtained. Benefiting from the preserved in-situ SiN cap layer and the additional ex-situ bilayer passivation, P_{sat} scales nearly linearly with V_{DS}, reaching 2.44 W/mm at 8 V (Fig. 5(b)), indicating minimal degradation from surface trapping [25].

A benchmark of low-voltage GaN-on-Si HEMTs in 26-30 GHz reveals that, the fabricated transistor achieves excellent power performance at low voltage (Fig. 5(c)–(d)). This is enabled by the reactive-sputtered n^{++}-GaN ohmic contacts, whereas several other reported transistors in this (low) voltage range employed MOCVD- or MBE-regrown GaN ohmic contacts, or aggressive lateral scaling. The combination of low-resistance ohmic contacts using reactive sputtering of GaN with Ge-doping, a high-current InAlN/GaN channel, and a vertically scaled structure with a thin channel and AlGaN back barrier ensures low R_{on}, high $I_{D,max}$, and strong 2DEG confinement, resulting in high power and linear gain. In addition, the combination of both *in-situ* and *ex-situ* passivation provides effective surface traps passivation. These combined epitaxial and process optimizations enable the outstanding power performance across the entire low-voltage operating range. Further improvements are expected through device scaling, particularly by reducing L_{SD}.

IV. Conclusion

This work demonstrated RF GaN HEMTs on Si substrate with Ge-doped sputtered n^{++}-GaN ohmic contacts. Enabled by the reactive-sputtered Ge-doped n^{++}-GaN ohmic contacts, the fabricated InAlN/GaN-on-Si HEMTs achieve low n^{++}-GaN/2DEG interfacial resistance, low R_{on}, high $I_{D,max}$, and high f_{max} starting at V_{DS} = 3 V despite a relatively large L_{SD}, resulting in excellent P_{sat} across the benchmarked V_{DS} range of 3–8 V. The observation of promising performance in low voltage FR2 operation validates reactive-sputtered n^{++}-GaN ohmic contacts as a promising ohmic contact technology for the next-generation RF GaN HEMTs.

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