Process and Integration Challenges for Via Last TSV (from top) on Functional LNA SOI wafers for 3D Heterogeneous chiplet integration

Xiangyu Wang, Mihai Dragos Rotaru, Yu Haitao, Mingchinq Jonq, Chai Tai Chong, King-Jien Chui
Institute of Microelectronics (IME), A*STAR (Agency for Science, Technology and Research),
2 Fusionopolis Way, #11-165 Innovis Tower, Singapore 138634
E-mail: wangxy@ime.a-star.edu.sg, Tel: (65) 67705764, Fax: (65) 62503694

Abstract

In our previous work, we discussed the demonstration of 10µm x 100µm Via-Last TSV (from top) fabrication on a blanket SOI Wafer, as illustrated in Fig 1(a) [1]. Analysis of the RF measured data on the mechanical test vehicle (MTV) wafers revealed that the TSVs' inductance and resistance were minimal and had a negligible impact on the RF performance [1]. This paper further investigates the process integration of Via-Last TSV (from top) fabrication on an actual low-noise-amplifier (LNA) device wafer. We observed the differences between the blanket SOI wafers and the LNA wafers in terms of incoming wafer surface topography and top oxide thickness uniformity. As a result, these differences pose a different set of process challenges in TSV formation on the frontside of the actual LNA device wafer as compared to a blanket SOI wafer. The step height at the pad area of the LNA wafers, measured by a laser microscope (Fig 2(c)), was approximately 1.3um. This topography could introduce potential residue defects, as depicted in Fig 3. Hence, additional process development is necessary to flatten the wafer surface to prevent the occurrence of any residue defects. Another process challenge faced by the actual LNA device wafer lies in the etching of the TSV. The total dielectric thickness of the LNA wafers is much higher than that of the dummy SOI wafers used in the previous study [1]. As such, achieving optimal TSV etching will require additional process tuning.

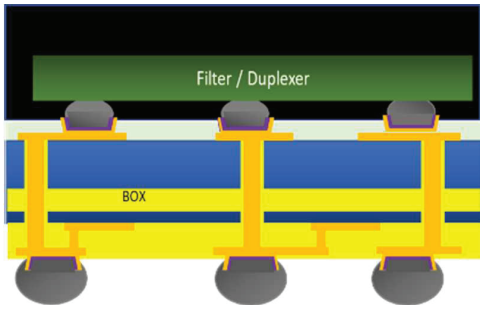

Fig.1 Schematic of the 3D chiplet package: LNA interposer and duplexer chip

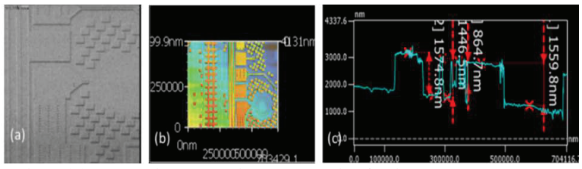

Fig.2(a) SEM image of LNA wafer before TSV process; Fig.2(b) optical image of LNA wafer before TSV process by laser microscope; Fig. 2(c)step height of aluminum pad area of LNA wafer before TSV process

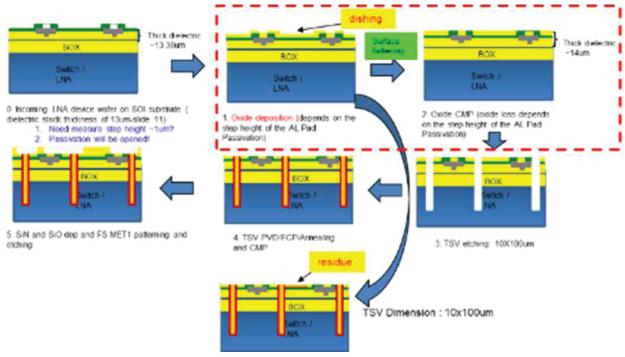

Fig.3 Copper residue caused by pre-layer topography with no surface planarization

Process Challenges - LNA wafer surface planarization

It is crucial to achieve wafer surface planarization prior to TSV fabrication to avoid potential defects caused by copper residue during TSV overburden CMP removal (as depicted in Fig.3). Previous work has indicated that pre-layer wafer topography could lead to copper residue on subsequent layers [2]. As such, we propose two methods for planarizing the incoming wafer surface: (i) dielectric deposition with planarization, and (ii) an alternative approach using a reverse mask. In the first approach, only dielectric deposition and planarization steps are employed, but for the latter approach, additional process steps including a reverse mask design, lithography and dielectric etch-back are needed. Due to the process margin of the lithography and etching and for the convenience of the reverse mask design, the conditions of the incoming LNA wafers used in the two methods were also different as shown in Fig.4 (a) and (b).

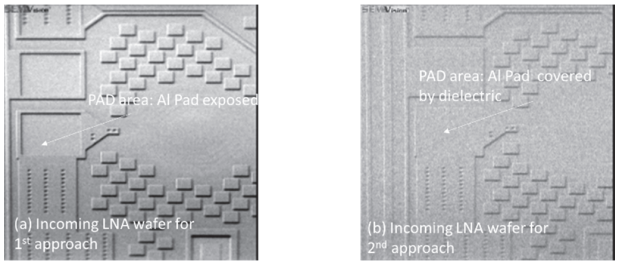

Fig.4(a) SEM image of incoming LNA wafer surface for the first approach; Fig.4(b) SEM image of incoming LNA wafer surface for the second approach

The planarization method is as illustrated in Fig.5. This involves dielectric deposition and planarization as the primary steps. Precise control of the dielectric film thickness,

uniformity, and subsequent planarization process is important. The final dielectric thickness on top of the pad must be measured or obtained for downstream etching process, ensuring proper landing on the aluminum pad layer without under-etching or over-etching. The dielectric film thickness to be deposited is primarily decided by the step height of the aluminum pad.

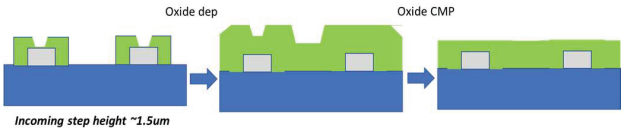

Fig.5 Dielectric with planarization process flow

The second latter method involves more complexity compared to the first method, due to the requirement of an additional mask for the reverse mask etching process. An additional reverse mask is designed and patterned to etch away protruding dielectric material at areas over the aluminum pads. Design of the reverse mask layer is as illustrated in Fig.6. Fig.7 illustrates the process flow for this approach. A dielectric layer is first deposited over the wafer. The reverse mask is then used to pattern and etched away the dielectric over the Al pad structures to reduce the topography. However, this reverse mask etch step does not achieve complete flattening. Another planarization step is required to completely flatten out the topography. It should be noted that the planarization process of the two approaches differ in terms of the amount of dielectric removal. The first approach primarily relies on planarization, resulting in considerable dielectric loss. In contrast, the second approach benefits from partial flattening after the reverse etching, leading to significantly reduced dielectric loss during the planarization step.

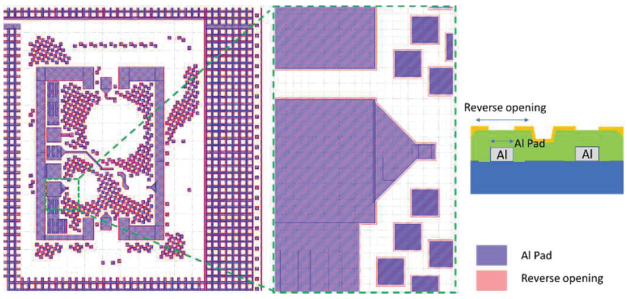

Fig.6 reverse mask design and the schematic of the aluminum pad with top dielectric layer

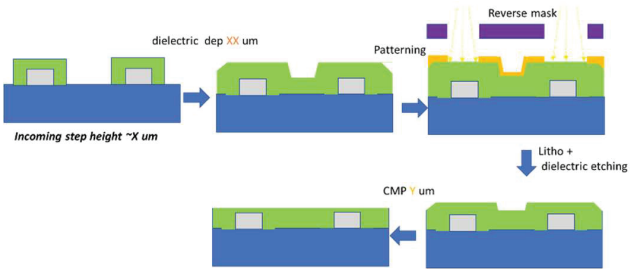

Fig.7 planarization with reverse etching process flow

Process Challenges - TSV etching on thick oxide

In our previous study [1], the TSV fabrication was conducted on the SOI wafers with a 1µm oxide layer. However, the current LNA SOI wafers possess multiple back-end-of-line (BEOL) dielectric layers, and the total dielectric thickness is over 10µm, posing a challenge for TSV etch. In addition, the surface planarization method described in the previous section introduces an additional 1 to 2µm of oxide layer before TSV fabrication. Schematics in Fig. 8(a) and 8(b) shows the distinctions between the wafers utilized in the previous study and the current one. For the LNA wafers in this study, an optimized oxide etching process has been developed to ensure a proper landing on the silicon prior to silicon TSV Bosch etch. During the etching development, it was observed that both over-etching and under-etching of the thick oxide substantially impacted the TSV silicon etching profile [5]. Fig. 9(a) displays the SEM cross-section result of the TSV etching profile, revealing striations along the TSV sidewalls. Our investigation identified that this defect mainly arose from under-etching of the top oxide layer. An optimized oxide etching process was thus developed to address this issue and ensure an accurate landing on the silicon surface after the oxide etching. Furthermore, the oxide etching profile plays a very pivotal role in TSV CD design considerations. Unlike the straight TSV silicon etching profile, the thick oxide etching yields a trapezoidal shape with a wider top CD. Given a targeted TSV CD of 10µm, the designed top CD for the thick oxide should be larger than 10µm, with precise sizing dependent on the slope of the oxide sidewall.

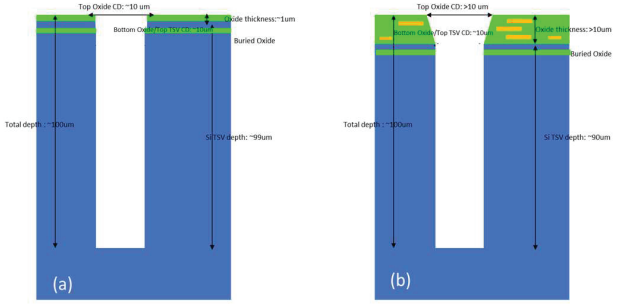

Fig. 8(a) TSV etching schematic on SOI wafers in previous study; Fig.8 (b) TSV etching schematic on the functional LNA SOI wafer

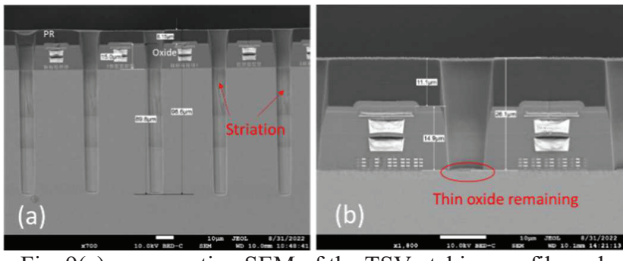

Fig. 9(a) cross section SEM of the TSV etching profile and striation defect at sidewall; Fig.9(b) cross section SEM of top TSV, interface of oxide and silicon

Result

Both surface planarization methods effectively flatten the LNA wafer surface, as depicted in Fig. 10(a) and 10(b). SEM

images from Fig.11(a) to Fig. 11(d) illustrate each step of the reverse etching approach. Notably, a final planarization step is necessary after the reverse dielectric etching, as slight topography persists in certain areas, as observed in Fig. 11(c). Conversely, employing the first approach, the pad opening area can be readily flattened without requiring further adjustments, as seen in Fig 12(b) and 12(c). When comparing these two methods, the reverse etching approach proves much more intricate than the other method. The former involves a greater number of process steps and presents heightened challenges for lithography and etching processes. Thus, in this study, the first approach was adopted to fabricate on the final testing wafers.

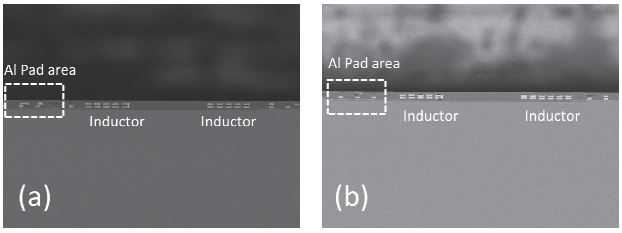

Fig. 10(a) cross section SEM of the LNA wafer surface after dielectric with planarization; Fig.10(b) cross section SEM of the LNA wafer surface after reverse etching

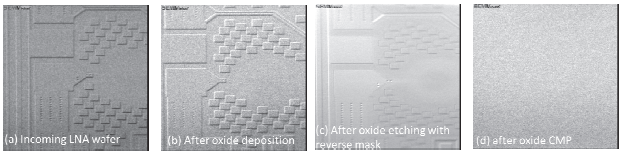

Fig. 11(a) the SEM images of incoming LNA; Fig.11(b), (c), (d) wafer after each step of the reverse etching approach

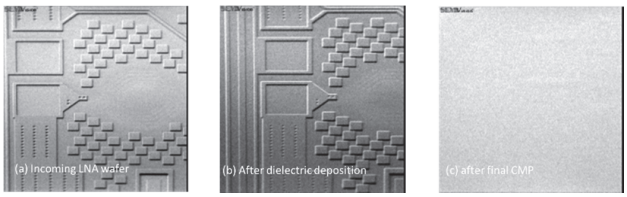

Fig. 12(a) the SEM images of incoming LNA; Fig.12(b), (c) wafer after each step of the dielectric with planarization

The final assessment of surface planarization involves inspecting the presence of any copper residue after TSV CMP process. Fig.13(a) displays an optical microscope image of the wafer surface after TSV Cu CMP. This observation is validated by the EDX results as shown in Fig. 13(b), conclusively indicating the absence of TSV copper and the barrier at the blanket area adjacent to the TSV. In Fig. 14(b), an SEM image of the inductor area is showcased, and the EDX analysis solely detected silicon and oxygen signals. This outcome signifies the success of the surface planarization by the first approach.

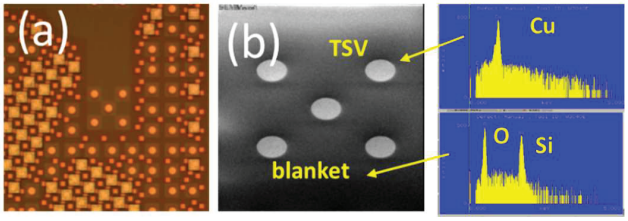

Fig. 13(a) optical microscope image of the wafer surface after TSV CMP Fig.13(b) SEM image and EDX after TSV CMP

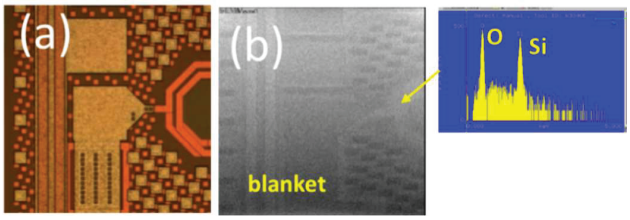

Fig. 14(a) optical microscope image of the wafer surface inductor area after TSV CMP; Fig.13(b) SEM image and EDX of inductor area after TSV CMP

Through several iterations of process adjustments, successful achievement of the 10µm x 100µm TSV etching on the thick oxide was realized. Cross-section SEM results are illustrated in Fig.15(a). The oxide etching profile takes on a trapezoidal shape with a wider opening on the top. Comparatively, the silicon etching profile remains notably straight in contrast to the oxide etching profile. The TSV sidewalls appear smooth, free of significant defects. Post TSV etch depth is approximately 112µm, while the TSV critical dimension (CD) at the top is around 10µm. Notably, there remains approximately 7µm of photoresist on top of the oxide layer after the thick oxide and TSV silicon etching, as depicted in Fig 15(a). This observation indicates that the employed photoresist in this study is suitably adequate for this multi-step etching process.

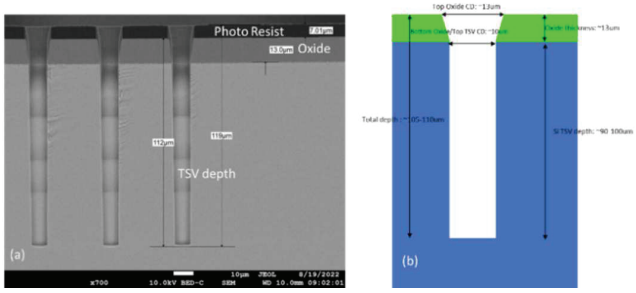

Fig. 15(a) Cross-section SEM of TSV etching profile; Fig.15(b) TSV etching schematic on the LNA SOI wafer

Fig.16 shows the cross-section image of the final 3D chiplet package. The duplexer chip is attached to the back side of the LNA chip with embedded TSV, while the front side of the LNA chip was subsequently attached to a PCB board. Void-free TSVs through the LNA chip provides electrical connections between the duplexer and the PCB.

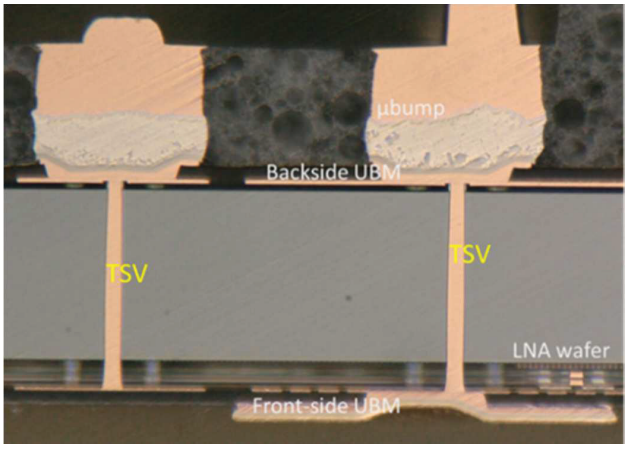

Fig. 16 cross-section optical image of the 3D chiplet package

Last but not least, electrical RF testing was performed. Measured RF results matched with the simulation as shown in Fig. 17 and Fig.18. A full discussion of the 3D modeling for the 3D integrated LNA and BAW duplexer is given in [6]. The RX channel's measured gain stands at approximately 20dB within the operational bandwidth, and the insertion loss remains below -40dB across the same range. Further measurements were conducted on additional samples, yielding consistent and repeatable results. This consistency underscores the success of fabricating the via-last TSVs on the LNA wafers.

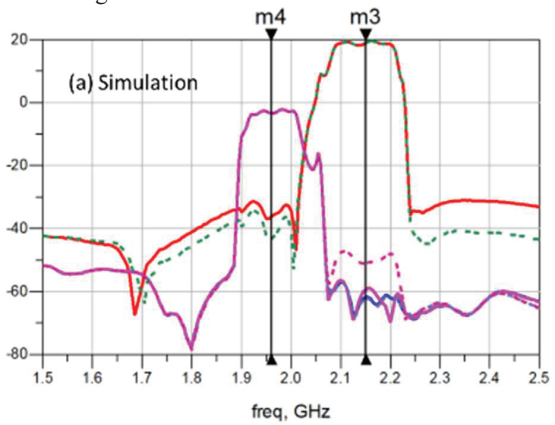

Fig. 17 simulation result of 3D stack insertion loss and gain

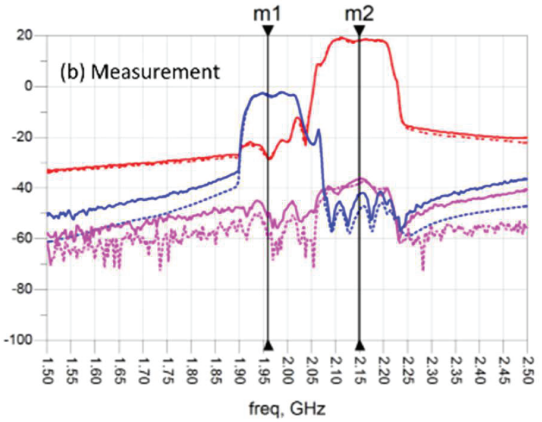

Fig.18 measurement result of 3D stack insertion loss and gain

Conclusions

In this study, the process and integration challenges of the via-last TSV fabricated on the LNA wafers have been discussed. Two main challenges are the incoming wafers surface planarization and the TSV etching development on the thick dielectric wafers. The 10µm x 100 µm void-free TSV has been successfully fabricated from the front side of the LNA wafers and was proved functional by the final RF testing.

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