Optimization of the CMP process for direct wafer-to-wafer oxide bonding

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Abstract

Direct wafer-to-wafer oxide bonding is an efficient method for the 3D integration of heterogeneous or homogeneous substrates and occupies a significant place in the advanced packaging technology portfolio. With multiple back-end of the line (BEOL) interconnect metallization layers, complexities in underlying film topologies may translate to significant variations in the surface topology and flatness at the bonding layer. During bonding, such variations can lead to unbonded void defects at the bond interface. For ensuring effective and reliable bonding with minimal defects, surface non-uniformities need to be planarized using a well-controlled chemical mechanical polishing (CMP) process, particularly important for fine-pitch hybrid bonding. In this study, It is demonstrated that CMP is a crucial factor for achieving void-free bonding and the quality of bonding is closely linked to CMP conditions. Systematic investigation has been carried out to improve surface topography on device wafers via CMP process optimization. The results have potential implications for optimizing Cu/dielectric fine-pitch wafer-to-wafer hybrid bonding processes.

Introduction

Increasing interest in automation and digitalization driven by artificial intelligence (AI) is resulting in the demand for high performance electronic systems with multiple functionalities [1]. Realizing such systems requires advancements in electronics packaging technologies, as conventional monolithic packaging is no longer sufficient. Thus, three-dimensional integrated circuit (3D IC) packaging is becoming a key solution for fabricating systems with high performance [2]. Metal/dielectric fine-pitch hybrid bonding is an important process technology for fabricating such 3D IC systems. In this process, while initial bonding between the dielectrics takes place at room temperature provided the surface is atomically smooth and free from particles [3], surface imperfections typically lead to void generation and reduced bonding strength [4]. In addition, excellent surface planarity is also a major requirement for achieving high bonding throughput.

In the case of conventional CMOS transistor device scaling, metal interconnect schemes become more complex requiring increasing number of metallization levels node-over-node [5]. Increase in the number of interconnect layers may significantly affect surface topography at the nanometer scale at higher metallization levels. While such small non-uniformities are not a major concern for conventional packaging, they are of significant concern for hybrid bonding and the bondability of such wafers needs to be assessed prior to bonding [6].

With growing interest in hybrid bonding processes, layer pattern effects on surface topography and hybrid bonding need to be understood. However, this is not well-explored in the literature. As schematically illustrated in Figure 1(a), the presence of intricate multilayer patterns in the underlying layers has been observed to induce surface irregularities, which can affect bonding performance, thus necessitating a comprehensive investigation.

Further, to achieve good bonding, it is necessary to effectively eliminate the irregularities transferred from underlying patterns onto the top bonding surface. Thus, optimization of the surface layer topography becomes imperative. Chemical mechanical planarization (CMP) is a key process method to planarize the surface layers to achieve atomic-level surface roughness [7] and plays a critical role in the subsequent processes, as evident in Figures 1b and 1c. Only upon adequate surface planarization can direct bonding be executed efficiently [8].

Thus, in this study, we systematically examine the effect of underlying metallization patterns on the surface topography of the top bonding layer and consequently, dielectric bonding. Systematic surface and interface investigation has been carried out to improve surface topography on device wafers via CMP

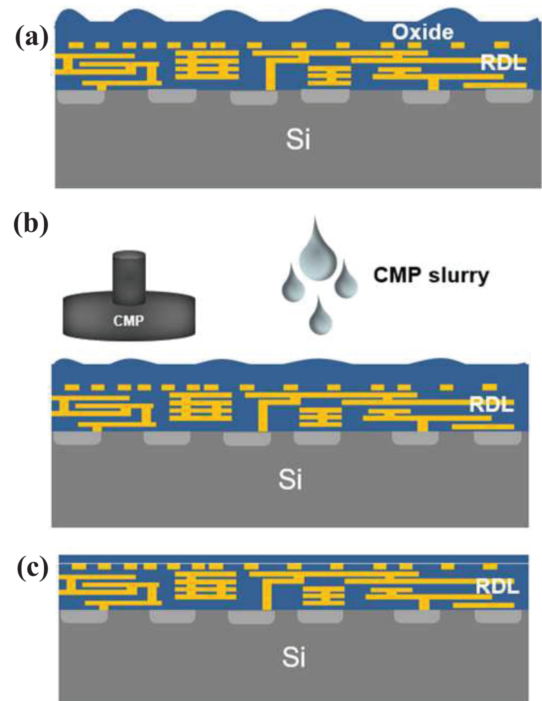

Figure 1. Schematic of CMP process optimization for mitigating surface non-uniformities and minimizing voids, (a). Non-planar surface. Topography of the underlying Cu bond pad layer will be translated to the oxide layer, (b). Removal of "x" nm of oxide by CMP to planarize the surface and inspection the bonding interface by CSAM after bonding, (c). Removal of "y" nm of oxide by CMP and inspection of the bonding interface by CSAM after bonding

process optimization. CMP process characteristics on device wafers have been investigated upon direct bonding of blanket oxide surfaces. The investigation is discussed in detail in the following sections.

Methodology

In this experiment, 300 mm, double-side polished p-type Si wafers have been used. Wafers with fine-pitch bond pad layer consisting of 1 µm Cu pads at 2.5 µm pitch were fabricated using a conventional Cu damascene process sequence. An 8 kÅ thick SiO_2 dielectric film was then deposited over the Cu pads as an interlayer for subsequent fusion bonding with carrier wafers. These wafers are referred to as device wafers, heretofore. This was followed by CMP to planarize the deposited SiO_2 on the device wafers. As carrier wafers, polished TEOS-deposited Si wafers were used. Fusion bonding was performed between the device and carrier wafers, after pre-treatment of the surfaces by N_2 plasma and DI water rinse. The resulting bonded interface was assessed using confocal surface acoustic microscopy (C-SAM) inspection under a liquid medium, for device wafer topography measurement.

Results and Discussion

To understand the effect of surface topography of the SiO_2-deposited wafers on bonding, different thicknesses of oxide were progressively removed from the device wafers by CMP, followed by fusion bonding with an oxide-deposited carrier wafer. C-SAM measurements were utilized for detecting interfacial voids after fusion bonding.

C-SAM inspection results of the bonded interface, with various thicknesses of oxide removed from the device wafers (no removal, low, moderate, high) are shown in Figures 2(a) to (d). The control wafer without oxide CMP (Figure 2(a)) shows poor bonding with huge bonding voids, indicating poor surface topography, likely translated from the underlying process layers. Moreover, wafer slippage occurred during the bonding of such wafers, further confirming poor bonding. Furthermore, a reduction in the bonding interface voids with increase in the oxide removal thickness on the device wafer was observed, which may be attributed to an improvement in surface topography across the wafer resulting from CMP. Furthermore, bonding improvement was observed starting from the wafer center to the edge gradually as removal thickness increased and complete bonding without bonding interface voids was achieved (Figure 2(d)), corresponding to the highest oxide removal thickness in the range studied. In addition, from Figure 2(a) (no CMP) to Figure 2(d) (highest oxide thickness removal), the bonding ratio, defined as the ratio of bonded to unbonded area, increased significantly, suggesting improved contact area

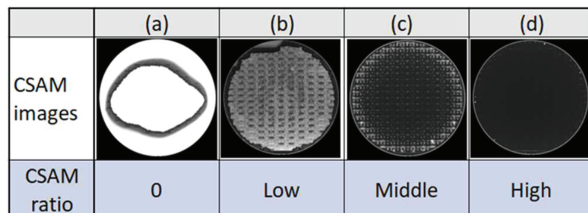

Fig. 2. C-SAM interface inspection of the fusion bonded wafers and bonded area ratio of splits with various thicknesses of oxide removed (low to high).

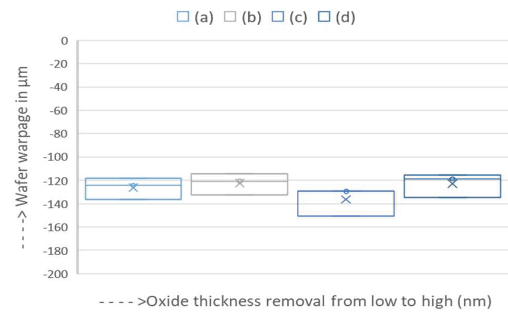

Fig. 3. Wafer warpage observed with different CMP oxide removal thicknesses from low (a) to high (d)

and topography of the bonding surface and enhanced bonding quality.

In addition, wafer warpage and bow height are measures of wafer flatness. To further understand the effect of wafer warpage and bow on bonding quality, these measurements were performed on the device wafers. Wafer warpage can affect the wafer shape, which could lead to uneven cross-wafer bonding performance. Figure 3 displays the warpage of device wafers with different thicknesses of oxide removed by CMP as indicated in Figures 3(a) to 3(d). All the wafers show compressive stress and no noteworthy differences in the wafer shape profile or wafer bow height (122-137µm) are observed across different CMP oxide removal thicknesses. It suggests minimal dependence of wafer warpage or bow on the bonding interface, as the oxide thickness removed increases.

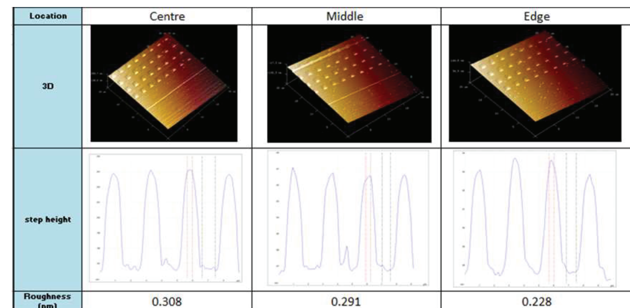

Fig. 4. Surface condition measured by AFM for CMP condition indicated in Figure 2a. Micro-scale surface topography caused by Cu protrusion transferred to the top surface be detected and cause wafer non-bonded.

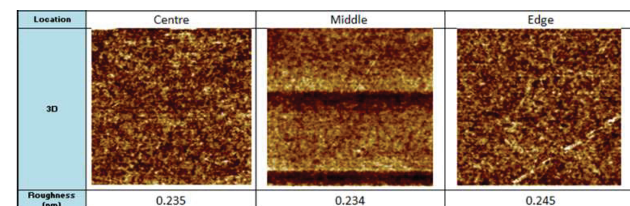

Fig. 5. Surface condition measured by AFM for CMP condition indicated in Figure 2b. No more transferred Cu protrusion Micro-scale surface topography be detected. And surface roughness be minimized.

In addition, micro-scale surface topography variation was studied through AFM shown in Figures 4 & 5.

Figure 4 shows the AFM measurement results for oxide deposited wafers without CMP, corresponding to Figure 2a. Hilocks observed in the top oxide film were transferred from the underlying Cu layers, causing unbonded wafer regions. After the 1st CMP process (corresponding to Figure 2b), this Cu protrusion was removed, and a flat surface was obtained and the AFM results are shown in Figure 5. Surface roughness (Ra) at all the locations was less than 0.25 nm. Even though the resulting roughness was adequate for fusion bonding [7], from the CSAM images (Figure 2b), interface bonding voids still existed. For the subsequent middle and high CMP processes (Figure 2c & 2d), even though the surface roughness change was marginal, no Cu protrusion could be detected, and C-SAM showed an improved bonding interface with reduced voids.

Wafer bow and micro-scale roughness are two key factors to control for fusion bonding. These two factors may be problematic for bonding quality, especially for wafers with complex underlying films and different densities of Cu pads. Thus, hybrid bonding was studied next.

Figure 6 shows the CSAM inspection results for hybrid bonding of two device wafers, with the similar conditions to the middle CMP. It may be noted that these device wafers are similar to those used for fusion bonding with carrier wafers, but without the interface dielectric layer.. The CSAM image shows that the center area is well bonded, but the wafer edge has many voids which is similar to fusion bonding.

From the perspective of pattern design, the die consists of some areas with sparse design with a bigger oxide pad (P1), while some areas have dense patterns with smaller Cu pads (P2). Some of researcher did study for sparse and dense design within same die [9-10], here we study more designs within one wafer.

From these inspections, the effect of thickness variation on the bonding interface voids can be observed. Figure 7 shows the analysis of oxide thickness and bonding grey level results from wafer edge to center. The grey level is defined as mean histogram data at the selected area, which is proportional to the bonding void of the CSAM image. A higher grey level score corresponds to more bonding voids. The yellow dotted line shown in the figure indicates the oxide thickness from the edge

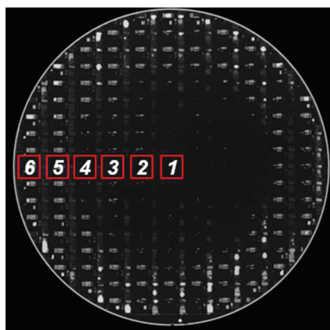

Fig. 6. Middle CMP proceeded hybrid bonded wafer CSAM images. The Center area shows good bonding for both sparse and dense designs, but the wafer edge shows many voids, especially in dense areas. Number 1 to 6 indicates the wafer die location from center to edge.

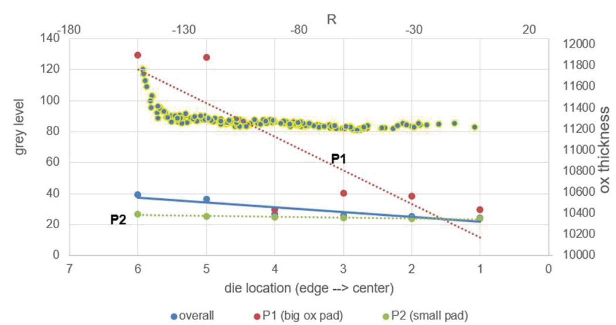

Fig. 7. Data analysis for hybrid bonded wafer. The yellow dot line shows oxide thickness from edge to center and red, green, and blue; dots represent a grey level of P1(sparse area), P2(dense area), and overall, respectively

to the center, while the red, green, and blue dots represent the grey levels of sparse area (P1), dense area (P2) and overall die, respectively.

From the wafer center (die 1 to 6), oxide thickness remains uniform, but larger variation is observed from die 5 to 6. The grey level for the sparse area (P1) is quite close from die 1 to die 4 but increases at the wafer edge (dies 5 and 6) and is closely related to the oxide thickness. Thus, oxide thickness variation could be an important factor for wafer bonding with bonding quality improved at uniform oxide thickness.

However, for dense areas (P2), the grey level remains uniform from center to edge (die 1 to 6), which is different from the sparse area (P1). This means bonding quality is not only related to oxide thickness, but also Cu density. In other words, non-uniform Cu density design will make the CMP process more complex.

Figure 8 shows the AFM scan results at (a) sparse area (P1) and (b) dense area (P2). For the sparse area, the big oxide pad causes non-uniform local pattern density and non-uniform topography. The topography difference between the Cu pad and oxide pad is far higher than the topography difference between

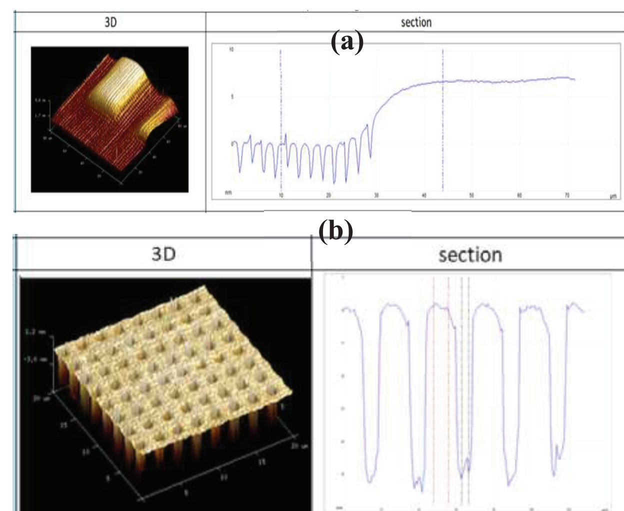

Fig. 8. AFM scans image at (a) sparse area (P1) and (b) dense area (P2).

Cu pads, which caused bonding voids in the sparse area. For the dense area shown in Figure 8(b), due to more uniform design, even dense area has more Cu pads, but surface topography is much better than sparse area, which brings better bonding quality compared to sparse area.

Conclusion

In this paper, it is demonstrated that surface topography is a crucial factor for achieving void-free bonding and the quality of bonding is closely linked to CMP conditions. The influence of CMP on hybrid bonding quality is discussed with focus on surface topography. Surface topography variation at the sub-micro to micro-level explains the significant bonding quality difference that occurs despite minimal warpage variations. In addition, the impact of oxide CMP removal thickness on hybrid bonding is studied. This demonstration could be a potential solution for future micro-void analysis across the bonded interface.

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