A Nanowatt Temperature-Independent Tunable Active Capacitance Multiplier with DC Compensation in 0.13-μm CMOS

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***Abstract*—This paper presents a nanowatt active capacitance multiplier (ACM) with enhanced tunable capacitance multiplication factor and temperature-independent current control for Artificial Internet of Things (AIoT) sensor applications. The proposed circuit is based on second-generation voltage conveyor (VCII) topology and biased in subthreshold region for high energy efficiency. An improved stacked translinear loop is designed to achieve temperature-independent bias with reduced power consumption. A DC compensation circuit is incorporated to compensate the output DC offset due to active bias circuit current, so that ACM can directly interface with other ultra-low power circuits. The proposed circuit is implemented in a standard 0.13-μm CMOS process. Simulation results show that the 3-dB bandwidth is from 0.04 Hz to 8 kHz and the multiply factor can be tuned from 337 to 561 with power consumption in the range of 41.6 nW to 46.4 nW. The achieved figure-of-merits (FoMs) is compared favorably with the other state-of-the-arts.**

Keywords—capacitance multiplier, voltage conveyor, translinear loop, DC compensation.

I. INTRODUCTION

Ubiquitous intelligent sensing is becoming a trend with the fast evolvement of artificial Internet of Things (AIoT) networks. Analog front-end (AFE) is a key building circuit block in AIoT system to sense the output of sensor and perform signal amplification and signal conditioning. The output of AFE will be digitized and then do further signal processing in digital domain. In many low-frequency sensing applications such as bio-signal acquisition, ambient sound detection and environmental vibration sensing, the target signal frequency falls in the range of DC to less than 10kHz. To filter out DC and other out-of-band noises, AFE usually requires a filter with a high-pass corner at close to DC, so that the useful information can be preserved.

Large capacitance is required to achieve such a low cutoff frequency. Modern CMOS technology offer a few options to implement capacitor on-chip, namely, metal-insulator-metal (MIM) capacitor, metal-oxide-metal (MOM) capacitor and MOS capacitor. The capacitance of these three types of capacitors is usually proportional to the area occupied by the capacitor. Limited by the unit area capacitance density, it is very challenging to implement large capacitance beyond nanofarad on chip. Off-chip lump capacitor can be used as a solution. However, for the design such as multichannel AFE, multiple capacitors up to tens or even hundred are required. It is impossible to connect so many off-chip capacitors to the on-chip AFE circuit.

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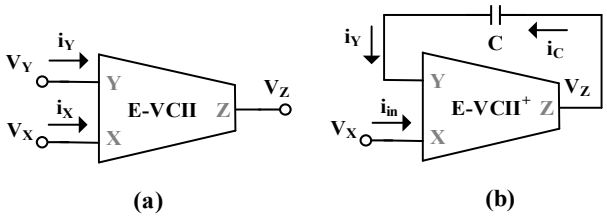

Fig. 1. E-VCII structure diagram. (a) Symbolic representation of E-VCII; (b) VCII based ACM.

Active capacitance multiplier (ACM) is a promising alternative solution to boost capacitance using active circuits [1, 2]. There are two basic ACM structures: Current Mode (C-Mode) and Voltage Mode (V-Mode). Compared with V-Mode, C-Mode ACM is more widely used in low-power circuits due to its straightforward implementation, lower internal voltage swing and lower supply voltage requirements [3]-[10]. Nevertheless, for C-Mode, a larger multiplier factor means a larger quiescent current and more considerable power dissipation, which challenges low-power design. Recently, a tunable nanowatt ACM was reported in [3]. An electronically tunable ACM based on second-generation voltage conveyor (VCII) [11]-[14] is shown in Fig.1 [3]. The relationship of VCII is shown in (1) for a positive amplification factor K.

$$\begin{cases} I_X = K \cdot I_Y & \text{(Current Convey)} \\ V_X = V_Z & \text{(Voltage Convey)} \\ V_Y = 0 \end{cases} \tag{1}$$

It is worth mentioning that for ideal VCII, node Y and node Z are low impedance nodes for current mode operation while node X is a high impedance node, hence capacitance can be multiplied. However, the ACM shown in Fig. 1 still has its performance limitations such as high corner frequency (80Hz), limited multiplier factor and most importantly, the DC bias current of ACM flows into the following stage circuit. This current will cause significant DC bias change of the subsequent stage and may lead to malfunction of the circuit block. These three limitations limit the practical application of nW-level ACMs with other circuits.

In this paper, a nanowatt tunable ACM is presented. The proposed circuit is based on VCII and operates in the subthreshold region for high energy efficiency. A stacked translinear loop is designed to achieve high energy efficiency and temperature-independent bias with reduced power consumption. A DC compensation circuit is incorporated to remove the output DC component due to bias circuit, so that the ACM can interface with other ultra-low power circuits directly with DC couple.

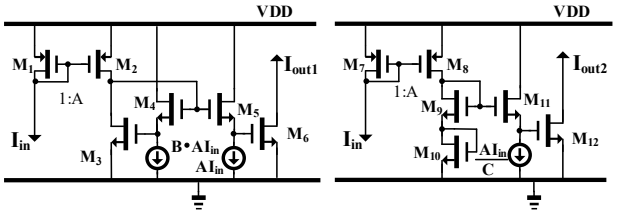

Fig. 2. The TL working in capacitance multiplier. (a) Traditional TL, (b) the proposed stacked TL.

The rest of the paper is organized as follows. Section II introduces the structure of the proposed capacitance multiplier and the circuit block design details. Section III shows the simulation results and Section IV concludes the paper.

II. Proposed Capacitance Multiplier

A. Stacked Translinear Loop

Translinear Loop (TL) is a simple yet valuable circuit for current transmission [15, 16]. The TL implements tunable current amplification and is temperature independent. Fig. 2 (a) shows traditional TL used in ACM [3]. In the subthreshold region, when $V_{ds} > 0.1V$, the drain current of MOS transistors is written as:

$$I_d = \frac{W}{L} I_{d0} e^{\frac{V_{gs}-V_{th}}{nU_T}} \tag{2}$$

where V_{gs} and V_{th} are the gate-source voltage and the threshold voltage of the transistor, n is the subthreshold slope factor, I_{d0} is a temperature-dependent constant for the identical size transistors, U_T is the thermal voltage (26mV at room temperature), μ is the constant of carrier mobility and C_{OX} is the gate-oxide capacitance.

In Fig. 2 (a), it can be observed that:

$$V_{gs3} + V_{gs4} = V_{gs5} + V_{gs6} \tag{3}$$

Inserting (2) into (3) gives:

$$I_{d3} \cdot I_{d4} = I_{d5} \cdot I_{d6} \tag{4}$$

Considering the current mirror $M_{1,2}$ and the given current sources, it can be derived that:

$$I_{out1} = B \cdot AI_{in} \tag{5}$$

From (5) it can be observed that the TL output current is tunable and can realize tunable current amplification in ACM circuit by externally controlled B.

The proposed improved TL is shown in Fig. 2 (b). The transistors $M_{9,10}$ are diode-connected to reuse the drain current. Similarly, it can be observed that:

$$V_{gs9} + V_{gs10} = V_{gs11} + V_{gs12} \tag{6}$$

$$\text{and} \quad I_{d9}^2 = I_{d10}^2 = I_{d11} \cdot I_{d12} \tag{7}$$

Considering the current mirror $M_{7,8}$ and the given current source, it can be derived from the following:

$$I_{out2} = C \cdot AI_{in} \tag{8}$$

The proposed TL is also temperature insensitive with the cancellation of U_T. To compare the power consumption, suppose B=C to achieve the same magnification. The ideal power consumption of these two TL can be derived:

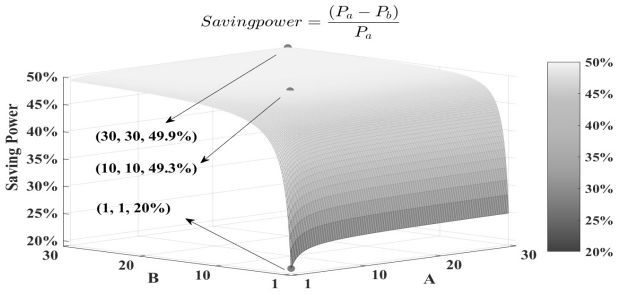

Fig. 3. Saving power of the proposed Translinear Loop (TL) versus different A and B.

$$P_a = (1 + 2A + 2BA) I_{in} V_{dd} \tag{9}$$

$$P_b = (1 + A + \frac{A}{B} + BA) I_{in} V_{dd} \tag{10}$$

Subtract (9) from (10):

$$P_a - P_b = (1 + B - \frac{1}{B}) A I_{in} V_{dd} \tag{11}$$

According to the principle of ACM, I_{in} needs to be amplified. Therefore, all the A, B and C should be larger than one. Based on this, it can be observed that $P_a - P_b$ is always larger than zero. This shows that the power consumption of the proposed TL is always lower than that of the traditional TL when achieving the same effect of amplifying current and the amplification factor (BA or CA). As shown in Fig.3, the range of saving power consumption is from 20% to 50%.

B. 2-Stage Tunable VCII Based Capacitance Multiplier

The schematic of the proposed tunable VCII-based ACM is depicted in Fig. 4(a). It consists of two stages of identical current amplification circuit. Two stages ensure the transistor can still operate stably in the subthreshold region with large current amplification. The super-source-follower consisting of M_{19} and M_{20} implements the voltage following of V_Z to V_X. And a physical MIM capacitor C is connected between nodes Y and Z. At node Y in Stage-1, the wide-swing current mirror (M_{1-4}) provides the first current amplification. Then the current is further amplified by a stacked TL (M_{5-8}). The AC is squared after passing through stage 2.

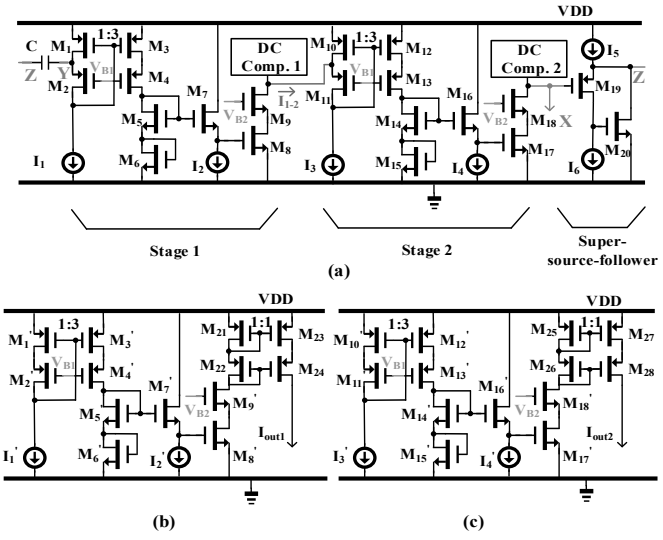

Fig. 4. (a) the proposed tunable VCII-based capacitance multiplier. (b) the block of DC Compensation 1. (c) the block of DC Compensation 2.

TABLE I. Transistors Aspect Ratio

Transistor	W/L (μm/(μm)
$M_{1\text{-}4}$, $M_{10\text{-}13}$, $M'_{1\text{-}4}$, $M'_{10\text{-}13}$	1/6
$M_{5\text{-}8}$, $M_{14\text{-}17}$, $M'_{5\text{-}8}$, $M'_{14\text{-}17}$	1/12
M_9, M_{18}	1/1
$M_{19\text{-}20}$	10/1
$M_{21\text{-}28}$	10/1

In Fig.4(a), between the first and the second stage, or between the second stage and node X, the current transfer is affected by the impedance, where the output impedance is expected to be infinite, and the input impedance is expected to be zero. Therefore, node Y is connected to the inner node of the wide-swing current mirror (M_{1-4}) and transistors M_8, M_9 form a common-source and common-gate structure to increase the output impedance. M_9 and M_{18} are extremely necessary. Because for ACM, the larger output impedance of stage-1 and 2 can achieve better low-frequency performance. It will be verified in the next Section.

Fig. 4 (b) and (c) show the circuits of DC compensation in the proposed ACM. The structures and transistor sizes of these two blocks are consistent with stage-1 and stage-2 to ensure $I_{out1} = I_{d9}$ and $I_{out2} = I_{d18}$. This minimizes DC I_{1-2} and I_X by providing drain current.

The total multiplier factor *K* and the impedance at nodes X, Y, Z are as follows:

$$K = 3^2 \cdot \frac{I_1}{I_2} \cdot 3^2 \cdot \frac{I_3}{I_4} = 81\frac{I_1 I_3}{I_2 I_4} \quad (12)$$

$$R_X = r_{o18} + (1 + g_{m18} r_{o18}) r_{o17} \approx g_{m18} r_{o18} r_{o17} \quad (13)$$

$$R_Y = \frac{1}{g_{m1} g_{m2} (r_{o2} \| r_{o1})} \quad (14)$$

$$R_Z = \frac{1}{g_{m19} g_{m20} (r_{o19} \| r_{Io6})} \quad (15)$$

where r_{on}, r_{Ion} and g_{mn} (for n=1,2,3……) are the output impedance of M_n and I_n and transconductance of the related transistor respectively.

III. Results and Disscusion

The proposed 2-stage tunable VCII-based ACM is implemented in a commercial 0.13-μm CMOS process. The power supply voltage is 0.6 V. Testing circuit is an RC low pass circuit, where R is 100 kΩ. The physical MIM capacitor used in the proposed circuit is a 0.626 pF. Transistors aspect ratios are shown in Table I. Both bias voltage V_{B1} and V_{B2} are set to 340 mV. Simple current mirrors implement all the current sources in Fig. 4. All I_1, I_1', I_3, I_3' are set at 1 nA. And I_5 and I_6 are set at 4 nA and 2 nA, respectively. The same values of I_2, I_2', I_4 and I_4' are varied from 380 pA to 490 pA to obtain different multiplier factors *K*.

In Fig. 5, the current gain of the first and second stages is theoretically 26.42 dB, where the total current gain from the node X to Y should be 52.83 dB. Furthermore, the voltage gain (Vx to Vz) is ideally 0 dB. These gains are relatively accurate in simulations. Considering -3dB as the cutoff frequency of the current convey [3], it can be observed that the current gain remains constant within the frequency from 20mHz to 21.8 kHz. However, as shown in Fig. 6, the bandwidth of the impedance of the capacitor is actually

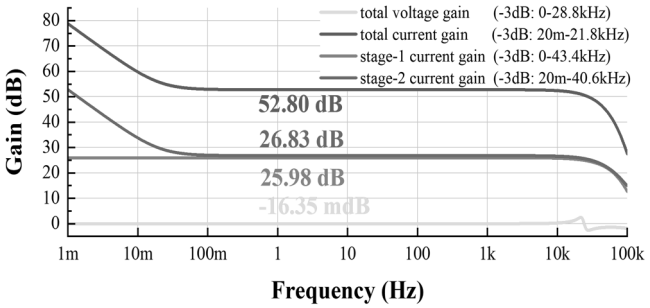

Fig.5. The AC gain of current and voltage conveys ($when\ I_2 = I_4 = 430\ pA$).

smaller than the bandwidth of the current conveys. This is because the simulated capacitance is also affected by the voltage convey (Vx to Vz). Therefore, 10% capacitance error is set as the cutoff frequency point. Under this stricter definition, this means that the operating frequency of the simulated ACM is from 40 mHz to 8 kHz. This can be well observed from Fig. 6 at different multiplier factors *K* from 20mHz to 8kHz. The values of R_X , R_Y and R_Z are 67.8 GΩ, 2 MΩ and 175 kΩ, respectively. Thanks to the common-source and common-gate structure, R_X is large enough to support low frequency performance.

In addition to bandwidth, the performance of ACM is often limited by errors. As shown in Fig. 7, as multiplier factor K is swept, it will cross the 0 % in the error curve. This work assumes ± 10 % error in the working boundary. However, in the implementation of tunable ACM, the error is not the parameter of primary concern. Tuning the multiplier factor K can effectively cover the error as long as the bandwidth keeps unchanged.

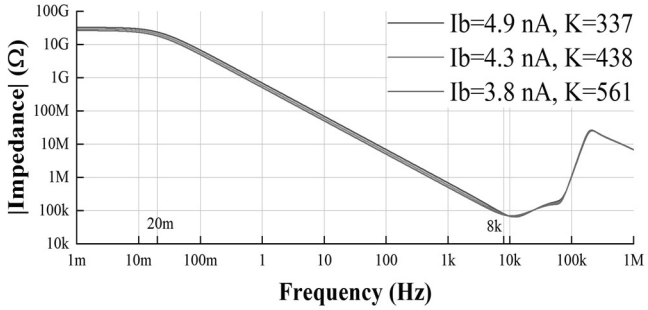

Fig.6. Amplitude frequency response of the simulated capacitor at different multiplier factor K ($I_2 = I_4 = 380\ pA, 430\ pA\ and\ 490\ pA$).

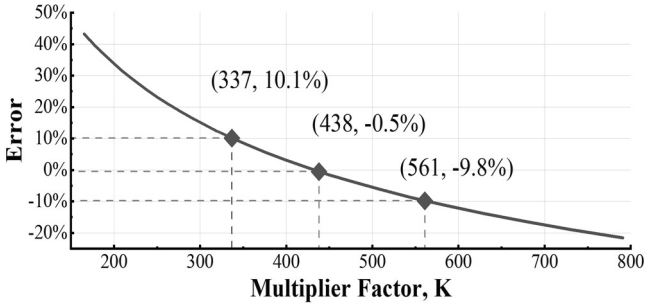

Fig.7. Error versus different multiplier factor K.

TABLE II. Benchmark with Prior Arts

Ref.	**This Work**	[3]	[7]	[5]		[17]	[6]	[4]
Tech. (nm)	130	180	180	180		NA	500	350
Topology	E-VCII+	E-VCII+	ICFOA	Class-AB current mirror		CFOA	Current mirror	2 OTA
Bandwidth (Hz)	40m-8k	80-40k	1-30k	750-200k	45-5k	20-2.8k	153-478k	10m-1k
Multiplier Factor	337-561	1-100	10-318	11.4	10.88	5	28	N.A.
Power (nW)	41.6-46.4	27-96	24000[a]	23760	302	N.A.	1320k	500-5000
Tunability	Yes (current)	Yes (current)	Yes (resistance)	No		No	No	Yes (current)
FOM (BC: best case; WC: worst case)	BC: 96.3k WC:64.8k	BC: 41.6k WC:1.5k	BC& WC:397.5[a]	BC& WC:95.6	BC& WC:178.5	N.A.	BC& WC:10.1	N.A.

[a] only one result when multiplier factor is 11

[5] FoM=K*Bandwidth/Power=K*(f_2-f_1)/Power

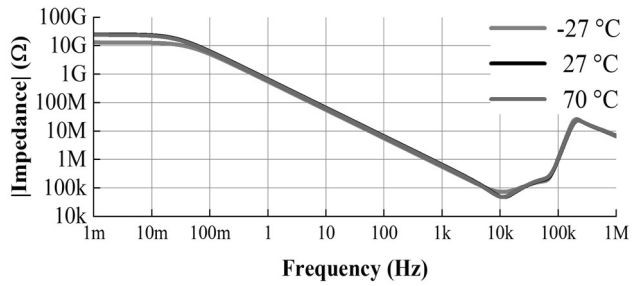

Fig.8. Amplitude frequency response at different temperatures when K=438.

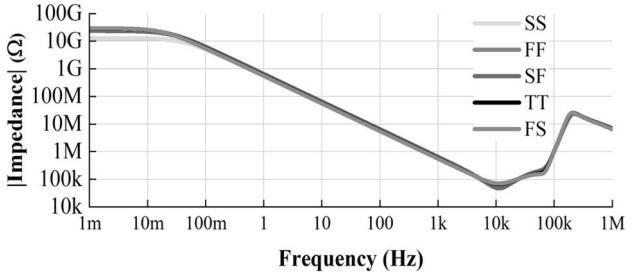

Fig.9. Amplitude frequency response at different corners when K=438.

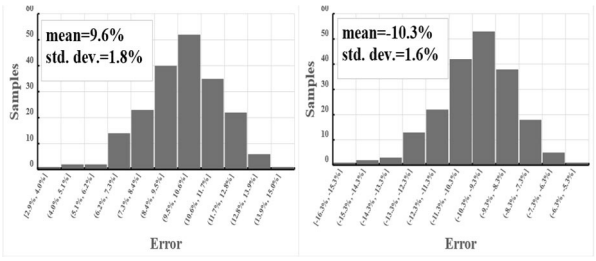

Fig.10. Monte Carlo simulations of the errors of the ACM when K=337 and K=561 with N=200 and σ=3.

The simulated DC operating point can verify the functionality of DC compensation. The simulated I_{1-2} and I_X are 0.2 nA and 4.1 nA (when K=438), respectively. Both these two are far less than 99 nA in [3] (when K=100). Although this block sacrifices almost one-half the total power consumption, it is essential for interfacing other low-power circuits, especially nW-level circuits. In addition, with lower requirement of K, it worth using only one stage of this work to achieve lower power consumption and pA-level DC output current with DC compensation.

In Fig.8 and Fig.9, the amplitude of the ACM impedance can be kept constant between 100 mHz and 8k Hz. The former agrees well with the temperature-independent analysis in Section II. As for corner simulation, SS corner performs the worst: the low-frequency cutoff is about 100 mHz. Fig. 10 shows the Monte Carlo simulation results (mismatch and process variations) of the ACM errors for two different values of K (337 and 561) over 200 runs. When K is 337, the average error is 9.6% with a standard deviation of 1.8%. Similarly, when K is 561, the average error is -10.3% with a standard deviation of 1.6%. The possible shifts from the intended error after the fabrication would be compensated by adjusting the bias currents I_2, I_4 so that the desired error would be achieved. Furthermore, the simulated value of the integrated input referred noise (IRN) is 82.3 μVrms, with a frequency range of 1 Hz to 8 kHz. In typical ACM applications, the presence of front-end modules such as amplifiers, provides adequate gain and renders this noise level acceptable.

Benchmarking with the works [3]-[7] and [17] targeting the low-power grounded ACM in Table II, higher figure-of-merits (FoM) figures indicate better comprehensive performance. This work simulated the best FoM with the state-of-the-art thanks to the subthreshold region and stacked TL, which has a high energy efficiency. So the worst case in this work is better than the best cases in other works. At the same time, under the nanowatt power consumption, this work successfully continues to expand the multiplier factor and improve the low-frequency performance.

IV. Conclusions

In this paper, a nanowatt temperature-independent tunable active capacitance multiplier with high energy efficiency is proposed, which achieves the best FoM and lowest power consumption with large multiplier factors. A new translinear loop is proposed to show high energy efficiency. In addition, after enhancing the low-frequency performance, the capacitance multiplier is expected to be applied in low-frequency sensing AIoT applications. Moreover, the proposed circuit greatly compensates for the DC output, making the capacitance multiplier interface other ultra-low power circuits more friendly. The future work is to apply this active capacitance multiplier structure to fully integrated on-chip low-frequency filter design to save overall chip area.

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