

A 310nA DCM Hysteretic Buck Converter with 95.8% Peak Efficiency and Greater Than 90% Efficiency in 10 μ A-100mA Load Range for Battery Powered IoT Sensors

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Abstract— This paper presents a discontinuous conduction mode (DCM) hysteretic buck converter for battery-powered Internet of Things (IoT) sensors. To reduce the quiescent power consumption, a duty-cycled comparator with delay compensation feedback loop is used in the zero current detector (ZCD). This feedback loop generates a self-calibrated comparator input offset to compensate for the comparator propagation delay. Additionally, a dynamic biasing scheme is applied to the hysteretic comparator to enhance the conversion efficiency under light load. The proposed buck converter was implemented in a 55-nm CMOS BCDLite process with an active area of 0.76 mm $\times$ 0.69 mm. With 310 nA quiescent current, this buck converter supports load currents in the range of 1 μ A – 300 mA with output voltage 0.8 V – 2.2 V. In particular, greater than 90% efficiency is maintained for load current from 10 μ A to 100 mA with 95.8% peak efficiency.

Index Terms— Buck converter, hysteretic control, low quiescent current, wide load range, discontinuous conduction mode.

I. INTRODUCTION

WITH the rising demands for smart homes, Industry 4.0, and personalized healthcare systems, the market for miniaturized low-power Internet of Things (IoT) sensors has grown tremendously. This growing demand has enhanced the research interest on power management units (PMUs) to optimize the power consumption across various applications [1-3]. Li-ion battery is a widely used power source for IoT devices due to its high energy density, long life cycle, and low cost. However, the output voltage of Li-ion battery varies significantly during the entire discharge cycle, typically in the range of 4.2 V to 2.5 V. Power management circuits such as low-dropout regulators (LDO) [4-6] and DC-DC converters [7-26] are essential blocks in a battery

powered system. With the continuous process scaling of modern CMOS chip fabrication technology, the integrated circuit (IC) supply voltage is reduced to 1.2 V or below. Therefore, high-efficiency DC-DC buck converter becomes a critical block to step down the variable battery output voltage to the stable voltage levels required by the ICs.

On the other hand, most IoT sensors spend most of their time in low-power or sleep modes when minimal energy is consumed, the DC-DC converter must function effectively under light load conditions [7]. During these light-load conditions, achieving high efficiency becomes particularly challenging, as controller's power consumption becomes dominant. On the other hand, when IoT sensors are activated for data acquisition or wireless communication, the load current can increase rapidly to hundreds of mA. Therefore, the buck converter must be able to handle a wide range of load with high conversion efficiency.

Various design techniques have been proposed to address these challenges. In terms of control scheme, Pulse Frequency Modulation (PFM) is suitable for light load conditions, while Pulse Width Modulation (PWM) is preferred for heavy load. To maintain high efficiency across wide load current ranges, multi-mode control that combines PFM and PWM has been adopted. Multi-mode converters require mode selection circuitry [7-9] or extra operation mode between PFM and PWM [10-11] to achieve seamless mode transitions, which leads to increased design complexity. One of the popular PFM control schemes is the Constant On-Time (COT) controller which generates a constant on-time to charge the output voltage. However, the inductor peak current has strong dependency on the input and output voltages. To resolve this, Adaptive On-Time (AOT) control has emerged as an attractive alternative with the additional advantage of improved transient response [9], [11-

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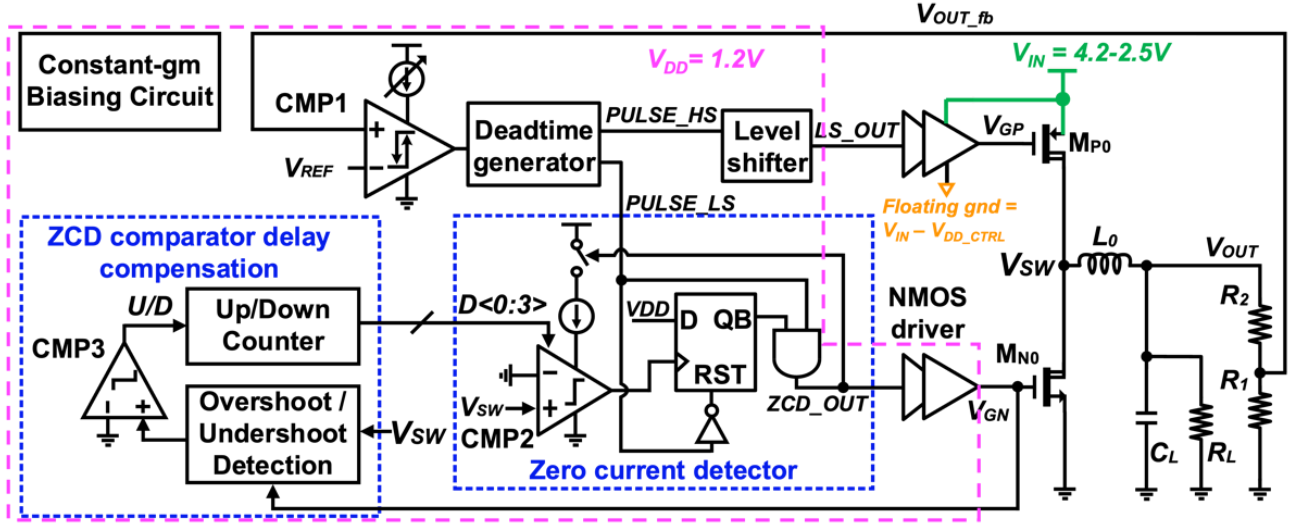


Fig. 1. Block diagram of the proposed DCM buck converter.

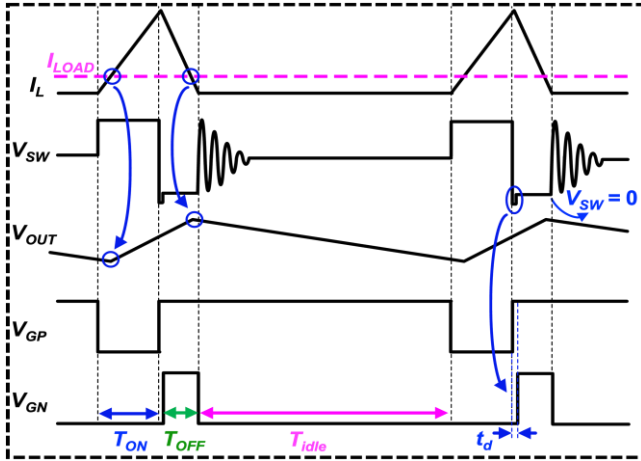


Fig. 2. Steady-state buck convert key node waveforms when M_{N0} is turned off without offset.

13], [15]. Hysteretic control [14, 15] is also widely adopted for its simplicity in design with only one comparator required to achieve the ripple-based control function, providing the benefit of lower power consumption. Furthermore, discontinuous conduction mode (DCM) operation has the advantage of inherent stability without any compensation circuit, which further reduces the design complexity [14-15]. For DCM operation, a zero current detector (ZCD) is required to monitor the current flow through the inductor and provide a signal to turn off the power switch at accurate timing to prevent the reverse current [16-20]. Hence low-power, low offset ZCD is a key building block in DCM-mode buck converter.

In this paper, a high-efficiency DCM hysteretic buck converter is presented. This design is an improved version of [26] with enhanced performance. Additional comprehensive system and circuit analysis as well as measurement results are presented in this paper. To reduce the quiescent power while maintaining high conversion efficiency, a comparator delay compensation loop is proposed for duty-cycled ZCD

comparator to achieve precise turning-off timing control for inductor reverse current reduction. This technique greatly relaxes the offset and speed requirements for ZCD comparator. In addition, a dynamic biasing scheme is applied to the hysteretic comparator. The DCM-only operation is maintained for the entire load current range from 1 μ A to 300 mA, providing inherent stability for the regulator while removing the necessity for complex loop compensation circuit. Greater than 90% efficiency is maintained for load current from 10 μ A to 100 mA with 95.8% peak efficiency.

The rest of this paper is arranged as follow. Section II presents the overall buck converter architecture and the hysteretic control. Section III describes the circuit implementation of key circuit blocks. Measurement results are presented in Section IV and Section V concluded the paper.

II. PROPOSED ARCHITECTURE

A. Architecture

The architecture of the proposed buck converter is shown in Fig. 1. It comprises a hysteretic controller, a power stage and an off-chip inductor. The controller consists of a dynamically biased hysteretic comparator CMP1, a deadtime generator, level shifters and a zero current detector (ZCD) with delay compensation loop for comparator CMP2. The converter down converts a 4.2-2.5 V input voltage V_{IN} from a Li-ion battery to a 0.8-2.2 V output V_{OUT} . The steady-state DCM operation waveform is shown in Fig. 2. The feedback voltage V_{OUT_fb} generated from the resistive feedback network is monitored by CMP1. The on-time T_{ON} for the high-side power switch M_{P0} is generated by the hysteresis window of CMP1 while ZCD determines the duration T_{OFF} when the low-side power switch M_{N0} is on. When V_{OUT_fb} drops below the lower hysteresis bound, CMP1 turns on M_{P0} and the charging phase T_{ON} starts. M_{P0} remains conductive until V_{OUT_fb} rises above the upper hysteresis bound. Thereafter, M_{P0} turns off and the charging phase ends. After a deadtime t_d , M_{N0} turns on and the discharging phase T_{OFF} starts. The inductor current I_L reduces

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until it crosses zero and C_L starts discharging when $I_L < I_{Load}$. The ZCD circuit detects the zero-crossing point and turns off M_{N0} , then the buck converter moves into idle state T_{idle} until the start of next charging cycle.

B. Hysteretic Control Analysis for DCM operation

The voltage-mode buck converter hysteretic control relies on a hysteretic comparator to turn on the PMOS power switch once the output voltage drops below the lower bound of the hysteretic band and turns it off once the output voltage rises above the higher bound of the hysteretic band. At steady state, the peak-to-peak value of output voltage ripple equals to the effective hysteretic band V_{He} ,

$$V_{He} = \Delta V_{OUT_p-p} \quad (1)$$

The switching frequency f_s can be derived as [15]

$$f_s = \frac{2\alpha_1 I_{Load}}{(1 + \frac{\alpha_1}{\alpha_2}) I_P^2} \quad (2)$$

where $\alpha_1 = \frac{V_{IN} - V_{OUT}}{L_0}$ is the inductor charging rate, $\alpha_2 = \frac{V_{OUT}}{L_0}$ is the inductor discharging rate, and I_P is the inductor peak current. For hysteretic control, I_P is determined by solving the following quadratic equation [15],

$$V_{He} = \frac{I_P^2}{2\alpha_1 C_{Load}} - (\frac{I_{Load}}{\alpha_1 C_{Load}} - R_{ESR}) I_P \quad (3)$$

Assuming $R_{ESR} \ll \omega_s C_{LOAD}$, when $I_{Load} \ll \sqrt{2\alpha_1 C_{Load} V_{He}}$, (3) can be simplified and I_P can be solved as:

$$I_P \approx \sqrt{2\alpha_1 C_{Load} V_{He}} \quad (4)$$

Substituting (4) into (2), (2) can be written as

$$f_s = \frac{I_{Load}}{(1 + \frac{\alpha_1}{\alpha_2}) C_{Load} V_{He}} \quad (5)$$

Therefore, for $R_{ESR} \ll \omega_s C_{LOAD}$, when $I_{Load} \ll \sqrt{2\alpha_1 C_{Load} V_{He}}$, switching frequency is proportional to I_{Load} .

For $R_{ESR} \gg \omega_s C_{LOAD}$, (3) can be simplified to

$$I_P = \frac{V_{He}}{R_{ESR}} \quad (6)$$

Substituting (6) into (2),

$$f_s = \frac{2\alpha_1 I_{Load} R_{ESR}^2}{(1 + \frac{\alpha_1}{\alpha_2}) V_{He}^2} \quad (7)$$

Therefore, for $R_{ESR} \gg \omega C_{LOAD}$, switching frequency is also proportional to the load current I_{Load} .

C. Power Switch Switching Timing Analysis

Fig. 3 illustrates two scenarios when M_{N0} is turned off at non-optimum timing, either late or early. The charge transfer phases in one switching cycle are labelled in the waveform. t_1 and t_2 represents the optimal duration for charging and discharging. t_3 is the time error between t_2 and the actual discharging time. Due to this time error, there is residual charge in inductor L_0 . When M_{N0} is switched off late, a reverse current is induced in L_0 and it will flow through the forward-biased body diode of M_{P0} after turning off M_{N0} . Due to the body diode conduction, an

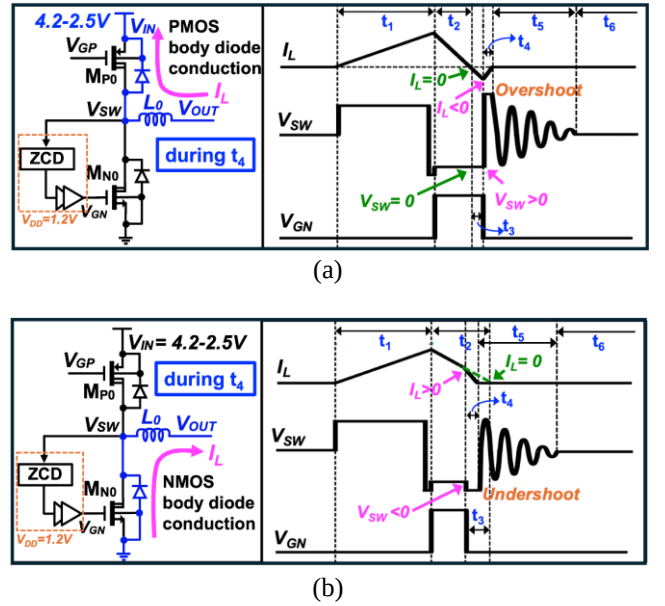


Fig. 3. Key circuit waveforms when M_{N0} is turned off at (a) late than zero current point; (b) early than zero current point.

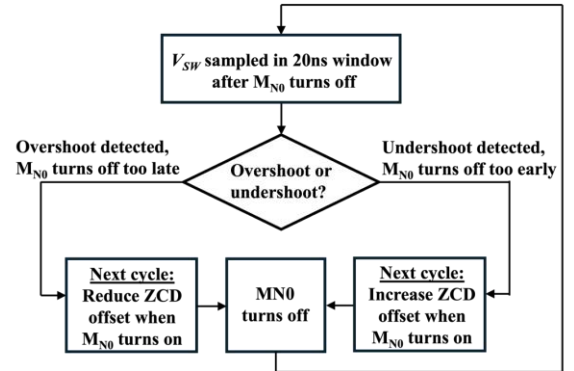


Fig. 4. Flow chart for ZCD delay compensation loop.

overshoot of V_{SW} is generated until the inductor is fully discharged. Similarly, when M_{N0} is turned off early, the remaining inductor current will be conducted through the forward-biased body diode of M_{N0} , and an undershoot of V_{SW} is generated. The duration of overshoot/undershoot caused by diode conduction is shown as t_4 . t_5 is the duration for parasitic ringing to fully discharge the inductor after diode conduction. During t_6 , inductor is fully discharged until the start of next cycle. The power loss due to ZCD time error can be analysed as below:

When M_{N0} is turned off too late,

$$t_4 = \frac{t_3 V_{OUT}}{V_{IN} + V_D - V_{OUT}} \quad (8)$$

$$P_{ZCD_error} = \frac{R_{DS_ON} \alpha_2^2 t_3^3}{4T_s} + \frac{V_D \alpha_2 t_3 t_4}{2T_s} \quad (9)$$

When M_{N0} is turned off too early,

$$t_4 = \frac{t_3 V_{OUT}}{V_D + V_{OUT}} \quad (10)$$

$$P_{ZCD_error} = \frac{V_D \alpha_2 t_3 t_4}{2T_s} \quad (11)$$

Equation (8) and (10) shows the overshoot/undershoot duration

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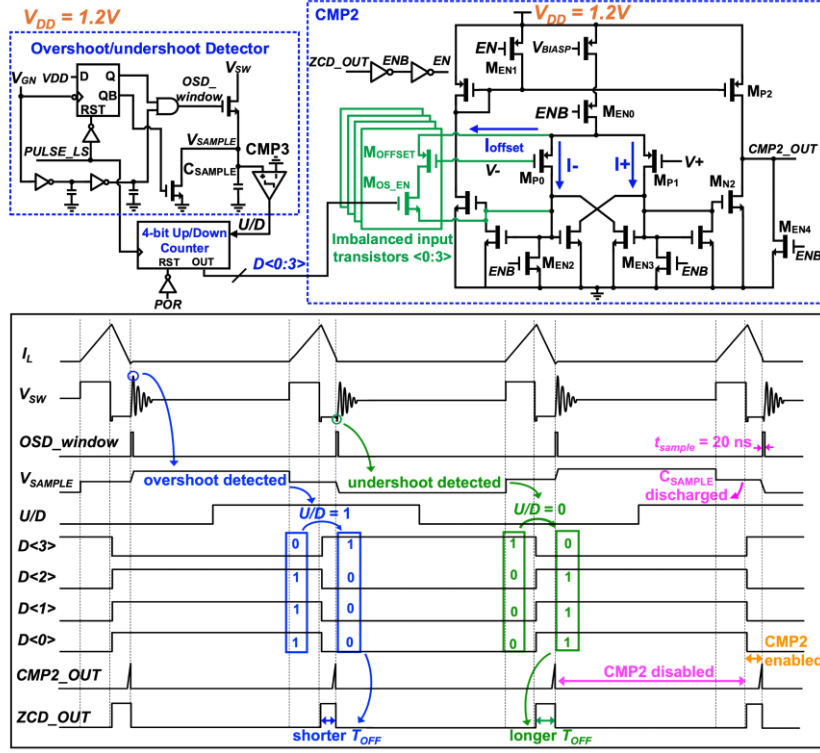


Fig. 7. Proposed delay compensation loop for ZCD and the corresponding timing diagram of key circuit nodes.

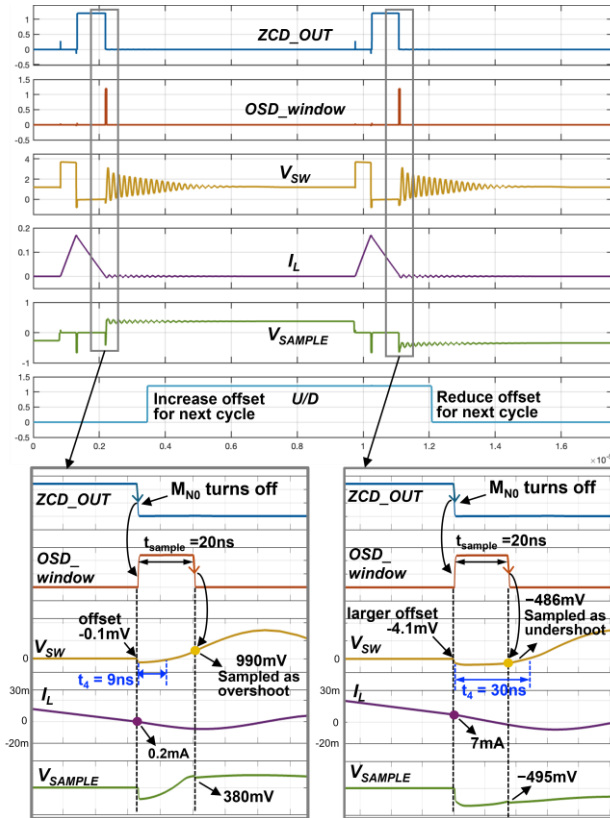


Fig. 8. Simulated waveform for the correction process of overshoot/undershoot detection error caused by the parasitic ringing.

strength of CMP2 output stage is reduced and CMP2 input offset increases one step (4mV). As a result, CMP2_OUT will be pulled up earlier before V_{SW} approaches zero to compensate for the delay. In the second cycle, an V_{SW} undershoot appears, indicating M_{N0} is turned off early. V_{SAMPLE} is charged to a negative voltage, and CMP3 output signal U/D will be zero. As a result, the counter output D<0:3> will count down by one bit from 1000 to 0111. A smaller size imbalanced input transistor of CMP2 is enabled, which reduces I_{OFFSET} and increases I_{+} , enhancing the pull-down current of CMP2, reducing CMP2 offset by 4mV back to the setting of the first cycle. The same process described above will repeat and the converter toggles between the adjacent optimal states.

As shown in Fig. 7, parasitic ringing is right after the period of overshoot/undershoot, hence there is concern on system stability if the parasitic ringing enters the sampling window of overshoot/undershoot detector. It should be noted that the parasitic ringing enters the sampling window when the duration of overshoot/undershoot (t_4) is shorter than the sampling window t_{sample} . This is because that the parasitic ringing only happens after M_{N0} , M_{P0} are turned off and the body diodes are not forward biased. Under this condition, V_{SW} node becomes a high impedance node and the residual charge on the parasitic capacitance resonates with L_0 to generate the parasitic ringing. Based on (8) and (10), t_4 is proportional to the ZCD output time error t_3 . If overshoot/undershoot detection error happens, the ZCD compensation loop counter changes in the wrong direction, ZCD output time error t_3 increases and in turn leads to longer t_4 . The parasitic ringing can be pushed out of the sampling window if the sampling window size and ZCD delay

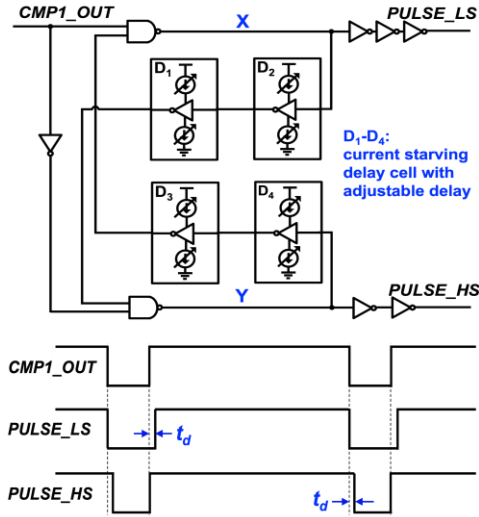


Fig. 9. Schematic of deadtime generator and key waveform.

compensation step size is designed properly. In the next cycle, correct detection of overshoot/undershoot will resume.

This process is illustrated using the simulation results shown in Fig. 8. Initially, the circuit switching point is tuned very close to the optimum point. In the first cycle, M_{N0} turns off earlier than the zero-crossing point at $V_{SW} = -0.1$ mV and the corresponding I_L is 0.2 mA. Since the current I_L cannot change the flow direction abruptly, M_{N0} body diode will be forward-biased until I_L crosses zero and a short period of V_{SW} undershoot ($t_4=9$ ns) is generated. Since M_{N0}, M_{P0} are turned off, the residual charge stored in the parasitic capacitor resonates with inductor L_0 and generates the parasitic ringing. As V_{SW} undershoot is only 9 ns, the following parasitic ringing will enter the sampling window. At the falling edge of sampling window, V_{SAMPLE} is sampled at 380 mV so an undershoot is detected wrongly as an overshoot and the counter increases 1 bit. Therefore, in the second cycle, M_{N0} turns off earlier than the first cycle at $V_{SW} = -4.1$ mV and the corresponding I_L is 7 mA. This larger offset results in an undershoot with longer duration ($t_4=30$ ns), hence the parasitic ringing falls out of the sampling window. V_{SAMPLE} is sampled at -495mV, indicating a correct detection of undershoot. This example shows the wrong decision due to the ringing interference can be corrected by the compensation loop. Furthermore, from measurement results shown in the next section, the V_{SW} ringing has a period of roughly 160 ns, which is much larger than the 20-ns window, so there is no possibility for multiple ringing cycles to enter the window and cause continuous wrong detections. In addition, it need to be highlighted that the precise zero-crossing detection also helps to minimize the residual charge in the inductor, hence further mitigate the parasitic effects.

C. Deadtime Generator

To prevent the shoot-through current when both M_{P0} and M_{N0} conduct simultaneously, a deadtime t_d is required between the falling edge of M_{P0} gate control signal V_{GP} and the rising edge of M_{N0} gate control signal V_{GN} . Therefore, the deadtime

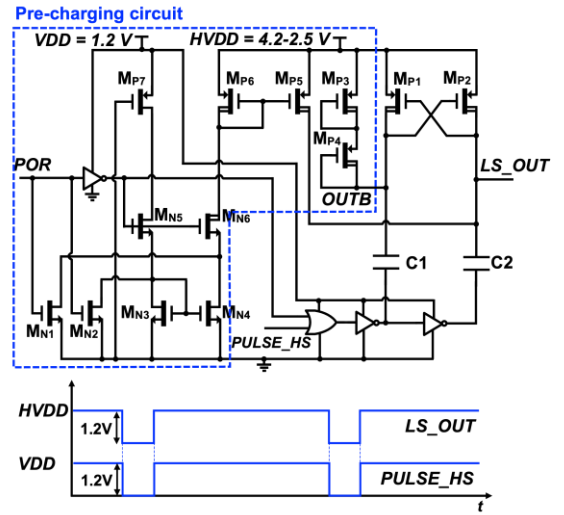


Fig. 10. Schematic of level shifter and key waveforms.

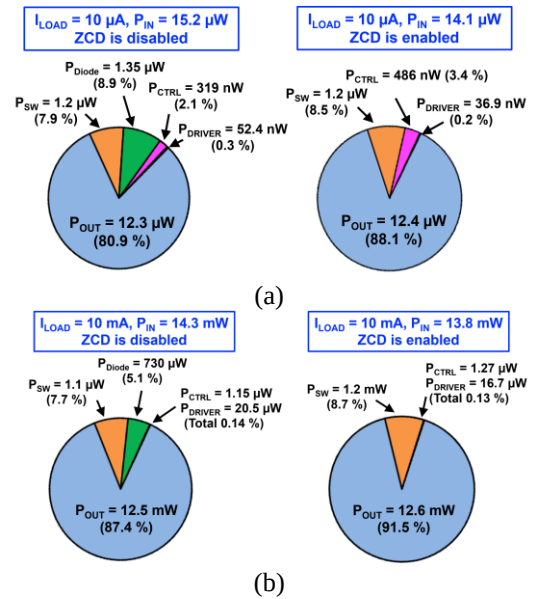


Fig. 11. Simulated chip power breakdown with ZCD disabled and enabled at (a) $I_{LOAD}=10\mu A$, (b) $I_{LOAD}=10mA$.

generator circuit, as shown in Fig. 9, is necessary to generate t_d . At the rising edge of $CMP1_OUT$, Y changes from 0 to 1. This rising edge of V_Y will propagate through delay cell $D3$ and $D4$, resulting in the change of X from 1 to 0. Neglecting the propagation delay of inverters and NAND gates, t_d between rising edge of $PULSE_{HS}$ and $PULSE_{LS}$ can be expressed as $t_d = t_{D3} + t_{D4}$. Therefore, M_{P0} will be switched off completely before M_{N0} starts to turn on. The same applies for the falling edge of $CMP1_OUT$, and t_d between falling edge of $PULSE_{HS}$ and $PULSE_{LS}$ can be expressed as $t_d = t_{D1} + t_{D2}$. Hence, M_{N0} will be switched off completely before M_{P0} starts to turn on.

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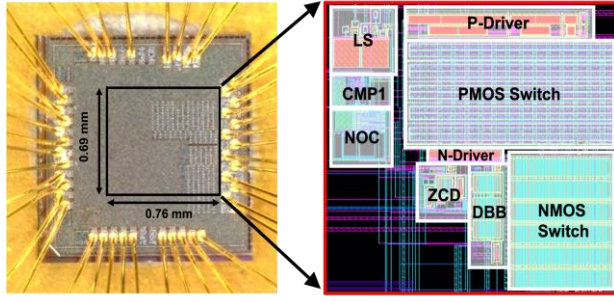


Fig. 12. Chip Micrograph and layout of key blocks.

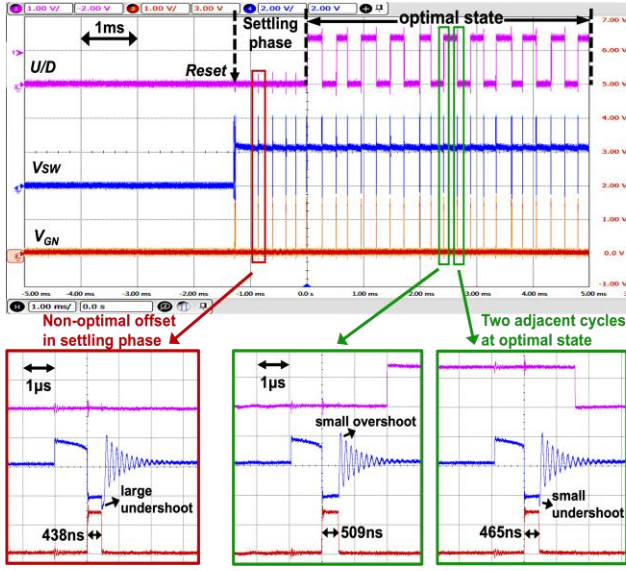
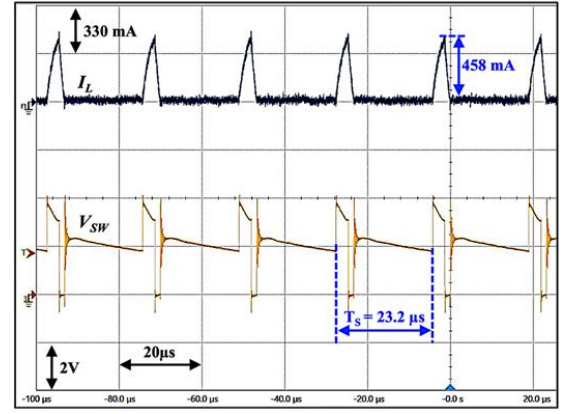


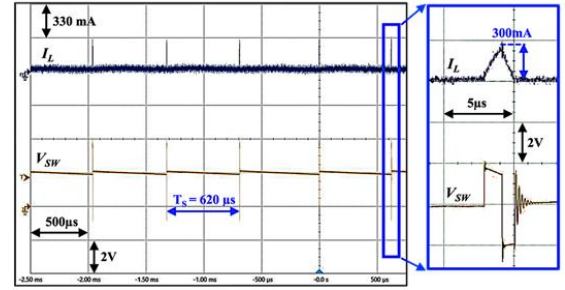
Fig. 13. Measured startup waveform, showing the CMP2 delay compensation loop operation.

D. Capacitive Level Shifter

The power switches M_{P0} and M_{N0} are thin-oxide HV CMOS devices. $|V_{GS}|$ for such devices cannot exceed 3.3V. V_{GP} is referenced to the HV supply HVDD to avoid any damage due to over drive voltage. Therefore, a level shifter is required to shift up the ground-referenced control signal to be HVDD-referenced while maintaining consistent signal swing. In this design, a capacitively coupled level shifter is adopted to minimize the quiescent current [29-30]. As shown in Fig. 10. This level shifter provides negligible input-to-output delay and zero static current consumption. This startup operation is carried out by the pre-charging circuit (M_{N1} - M_{N6} , M_{P3} - M_{P7}). During the pre-charging phase, POR is set to 0. M_{N5} and M_{N6} are turned on to enable the pre-charging circuits and a start-up current flowing from M_{P7} is mirrored to M_{N3-4} & M_{P5-6} . This current will charge C2 then LS_OUT will be charged up gradually to follow the ramp-up of HVDD. Meanwhile, OUTB will be charged up to $(HVDD - V_{SG_MP3} - V_{SG_MP4})$ and turns on M_{P2} to facilitate the charging of C2. The on resistance of M_{P5} is designed to ensure $(HVDD - LS_OUT)$ is always smaller than the threshold of HV PMOS in high-side driver. Therefore, the HV devices in the subsequent stage remain off during the startup



(a)



(b)

Fig. 14. Measured steady-state I_L and V_{SW} when (a) $I_{LOAD}=40$ mA and (b) $I_{LOAD}=1$ mA.

stage. After HVDD reaches the desired value, POR changes to 0. M_{N1-2} are enabled to turn off M_{N3-4} to cut off the start-up current. As a result, the pre-charging circuit is disabled. The level shifter core will be activated and operate in a steady state.

E. Power Breakdown Analysis

A circuit power analysis is performed to investigate the efficacy of the proposed ZCD delay compensation loop. The breakdown of chip power consumption with and without ZCD delay compensation is recorded in different load conditions. As shown in Fig. 11 (a), at light load condition of 10 μ A load current, the power efficiency is improved from 80.9% to 88.1% when the ZCD block is enabled. Similarly, as shown in Fig. 11 (b), with 10 mA load current, the system efficiency is improved from 87.4% to 91.5% when the ZCD block is enabled.

IV. MEASUREMENT RESULTS

The proposed buck converter was implemented in a 55-nm CMOS BCDLite process. Fig. 12 shows the chip micrograph and the circuit layout. The core circuit area is 0.76 mm $\times$ 0.69 mm. Fig. 13 shows the measured waveform of the ZCD circuit during the converter startup phase. After presetting the counter to '1000', the converter starts to operate with excessive input offset for CMP2, an V_{SW} undershoot is detected by the overshoot/undershoot detector. U/D remains low during the settling phase of the delay compensation loop, which means the offset keep decreasing to approach the optimal state. After a few cycles, U/D starts to toggle between 0 and 1 periodically and minimal V_{SW} overshoot and undershoot can be observed.

TABLE I
COMPARISON WITH STATE-OF-THE-ART WORKS

	This Work	[7] TCAS-I'20	[14] JSSC'18	[9] TCAS-I'22	[21] A-SSCC'23
Technology (nm)	55 BCDLITE	180 CMOS	130 CMOS	180	22
Area (mm ²)	0.53	1.1	0.14	0.55	0.45
Control scheme	Hysteretic	DCT+PWM	Hysteretic	AOT+DGM	PFM
Input voltage (V)	2.5-4.2	2-5	1.8-3.3	2.7-4.7	1.52-3.63
Output voltage (V)	0.8-2.2	0.8,1,1.2,1.8,3	1.2	1.6	0.925
Load current (A)	1 μ -300m	1 μ -50m	100n-2.65m	1 μ -100m	20 μ -40m
Inductor (μ H)	6.8	2.2	18	4.7	2.2
Output capacitor (μ F)	2.2	4.7	0.056	4.7	47
Output Ripple (mV)	35	25	29	40	8
Quiescent current (nA)	310	470	440	490	2500
Peak Efficiency (%) @V _{IN} /V _{OUT}	95.8 @ 3.2V/2.2V	94.7 @ 3.6V/3V	92.1 @ 1.8V/1.2V	92.1 @ 2.7V/1.6V	88.7 @ 3.3V/0.925V
Efficiency (%) @light load	90.8 @10 μ A	85.6 @10 μ A	62 @10 μ A	75 @10 μ A	65.1 @ 20 μ A
Efficiency (%) @heavy load	91.1 @100mA	90 @50mA	92.2 @2.65mA	76 @100mA	88.7 @40mA
Voltage droop/time (mV/ μ s) @ load step	35/3.2 @ 1 μ A-25mA	80/11 @ 6.67 μ A-50mA	30/0.2 @ 100nA-2.65mA	48/8 @ 5 μ A-80mA	NA
FOM (pA/%) ¹	1.14	11	26.8	6.5	1920

1: FOM from [7,9] = $I_{LOAD_min} \times I_q / (I_{LOAD_max} \times \text{Eff}_{light_load})$

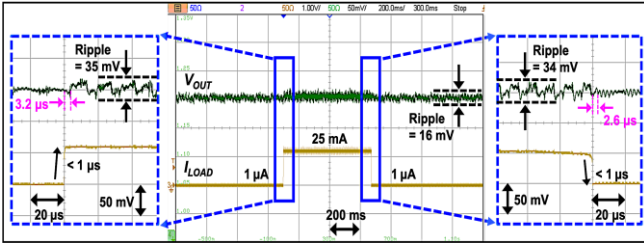


Fig. 15. Measured load transient response between 1 μ A and 25mA.

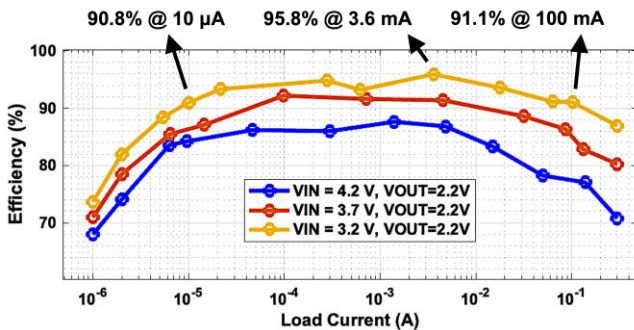


Fig. 16. Measured conversion efficiency with $V_{out}=2.2V$ versus load current at different input voltages.

Fig. 14 shows the measured steady-state inductor current I_L and voltage waveform of switching point V_{SW} at heavy load $I_{LOAD} = 40$ mA and light load $I_{LOAD} = 1$ mA conditions. For 40mA load, the converter operates at 43.1 kHz with 458 mA

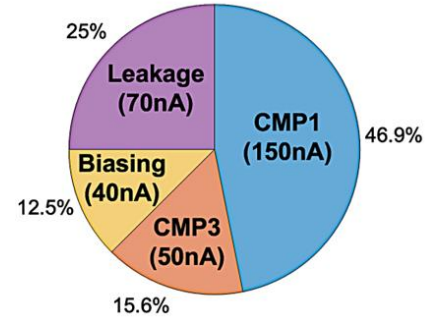


Fig. 17. Measured chip power consumption breakdown.

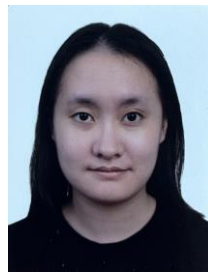
peak current, and for 1mA load, the converter operates at 1.6kHz with 300mA peak current. Fig. 15 shows the measured load transient response. The load current steps up from 1 μ A to 25 mA and then steps down back to 1 μ A. The converter regulates this load change with a ripple lower than 35 mV and less than 3.2 μ s transition time. The measured efficiency versus I_{LOAD} from 1 μ A to 300 mA is shown in Fig. 16. The measured efficiency is shown for variable V_{IN} from 3.2 V to 4.2 V, and a fixed V_{OUT} at 2.2 V. Peak efficiency of 95.8% is achieved at 3.6 mA. The overall chip quiescent current consumption is 310nA and the power breakdown is shown in Fig. 17. The circuit performance is summarized and compared with other state-of-the-art designs is Tab. I. The proposed buck converter achieved the highest peak efficiency and the widest load current range from 10 μ A to 100 mA while maintaining higher than 90% efficiency.

V. CONCLUSION

This paper presents a DCM hysteretic buck converter for battery-powered IoT sensors. To reduce the quiescent power consumption, duty-cycled comparator with delay compensation feedback loop is used in the ZCD and a dynamic biasing scheme is applied to the hysteretic comparator to enhance the conversion efficiency under light-load. This buck converter supports load current in 1 μ A – 300 mA range with output voltage 0.8 V – 2.2 V. Greater than 90% efficiency is maintained for load current from 10 μ A to 100 mA with 95.8% peak efficiency.

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