Design and characterization of low loss 50 picoseconds delay line on SOI platform

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Abstract: We design and experimentally demonstrate 50 picoseconds (ps) low loss delay line on 300 nm SOI platform. The delay line unit consists of straight rib waveguide and strip bend section linked by a transition taper waveguide. Low propagation loss of ~ 0.1 dB/cm is achieved on the straight rib waveguide. With taking into account both low loss and desirable delay, a complete design and characterization process for passive delay line is presented. Our measurement results show that about 0.7 dB excess loss is achievable for 50 ps delay. The loss can be further reduced by adjusting the layout parameters.

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OCIS codes: (130.3120) Integrated optics devices; (230.7370) Waveguides.

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1. Introduction

Silicon photonics allows for large scale integration of photonic components on small-size chip using complementary metal oxide semiconductor (CMOS) compatible technology. Optical delay line is one of the critical functional components in photonic systems, which is able to adjust the time and phase properties of signals through properly introducing optical delay and is essential for various applications such as optical buffers [1], interferometer [2] etc. On-chip tunable delay lines have been widely investigated, and various approaches such as nonlinear phenomena [3] or microring resonators [4] are applied to achieve tunable optical delay. The challenges lay in that this kind of delay lines normally work with relatively narrow operation bandwidth and large excess loss, and require large device size or high precision fabrication [5]. Recently, H. Lee et. al have demonstrated on-chip 27 meter ultra-low loss delay lines based on large-dimension special waveguides of triangle cross-section with smooth edges using optimized fabrication [6], which reveals the potential for ultra-long delay on integrated photonic platform. Routine silicon waveguide based passive delay lines with desirable delay are significant for many practical applications. They have the advantages of wide bandwidth, easy-to-integrate, compact footprint, and stable performance. Combined with thermo-optic switch or attenuator, passive delay lines are able to achieve the functions of digital delay lines or microwave filters etc. Low loss and precise group delay are two straightforward targets in design of passive silicon delay line. Many factors are involved for design and optimisation considerations such as group velocity of the waveguide structure, waveguide crosstalk isolation, and delay unit layout arrangement and so on. In this paper, by taking all these factors into account, we report a complete design and characterization process for passive delay lines. Several 50 ps delay line units are designed and demonstrated on 300 nm silicon platform for the first time. 300 nm silicon waveguides have better polarization insensitivity [7], and they are easy to integrate with photodiode or other components in certain applications. Besides, high efficiency grating couplers are more easily realized on 300 nm platform by single-etching fabrication process [8, 9]. However, 300 nm waveguides usually have larger roughness sidewall boundaries (compared with 220 nm Si waveguides), and thus it is intuitively challenging to achieve low propagation loss. By decreasing the optical intensity on the sidewall boundary through an increased large core-size silicon waveguide with a width of 3 μm, a low loss below 0.1 dB/cm has been demonstrated on 300 nm platform lately [10]. Here, we design two types of compact rib waveguides on 300 nm platform for delay unit fabrication. Through properly reducing the rib etching depth (i.e. reducing roughness sidewall area), a low propagation loss of ~ 0.1 dB/cm is realized in one of them. For the whole delay line structure, the hybrid waveguide idea [11, 12] is adopted for their layout design. We use the low loss rib waveguides for all the straight optical paths and quasi-single mode waveguides for the bend paths to guarantee that only fundamental mode is excited and traveling in the structure. The delay is properly designed through choosing the correct length for each section of the waveguides. We characterize both the loss and delay performance of the proposed delay line units. The measurement results show that the excess loss of ~ 0.7 dB per unit with a broadband operation is achievable for the desirable 50 ps delay. The loss can be further optimized by decreasing the delay line tracks and bend sections. We measure many fabricated delay line samples from two batches of wafers, and observe that the delay variation is within 3 ps.

2. Design and modeling approach

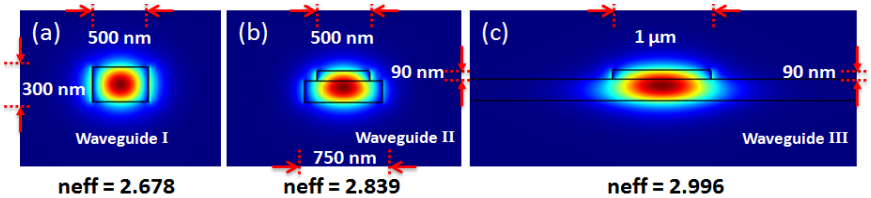

Fig. 1. The x component of E-field in the proposed strip and rib waveguides.

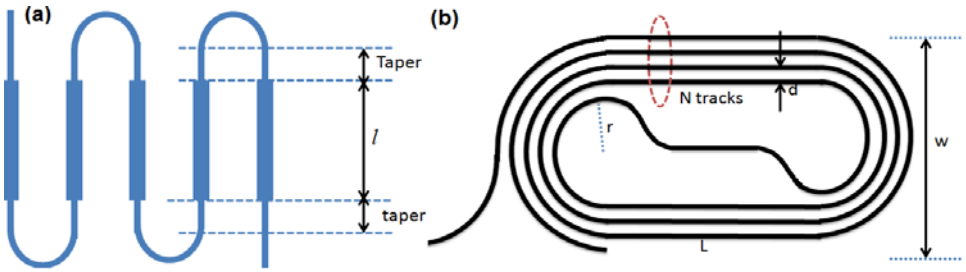

Fig. 2. (a) The cut back layout of the rib waveguides; (b) the main parameters for the delay line unit structure.

In order to design low loss delay line, the first step is to design low loss waveguide. In our schema, we use three types of silicon waveguides to compose the delay line unit. The optical field distributions in these waveguides are illustrated in Fig. 1, the structure dimension parameters and corresponding effective index of fundamental guided mode are also indicated. Fig. 1(a) is 500 nm × 300 nm strip waveguide (named by waveguide I) which is used for the bend section; Fig. 1(b) is a rib waveguide (waveguide II) with two etching steps, the top step has rib width of 500 nm and bottom step has width of 750 nm; Fig. 1(c) is also a rib waveguide (waveguide III) but it has wider rib width of 1 μm at top step and its bottom step has no etching sidewall inside the mode field reachable range (i.e. the sidewall boundary is far away enough and has little effect on the mode field). Since it is difficult to achieve pure single guided mode on 300 nm silicon waveguide, we mainly determine the waveguide dimension parameters according to the following two principles: firstly, we attempt to make the effective index difference between the fundamental mode and higher order modes as large as possible in order to reduce the possibility of intermodal coupling; secondly, the waveguide dimensions are optimized to make the high order modes weakly-confined and lossy in order to avoid their affects on the delay behavior. Through numerical simulations, we have found that 90 nm etch depth is good to achieve these purposes. We have adopted the cut-back method to characterize the loss performance of the two types of rib waveguides. The structure layout is arranged as shown in Fig. 2(a). For the low loss and mode excitation consideration, the taper length has been set as 20 μm and 200 μm for rib waveguides II and III, respectively. We have varied the waveguide length *l* as 200 μm, 800 μm and 1400 μm and measured the total insertion loss. The measurement result is given in Fig. 3. Fig. 3 (a) shows the result for rib waveguide II. A propagation loss of ~ 2.7 dB/cm is obtained from the slope of the fitting curve. Similarly, Fig. 3(b) indicates the propagation loss for rib waveguide III and it can be seen that a low propagation loss of ~ 0.1 dB/cm is achieved. The great difference in loss behavior of waveguide II and waveguide III is attributed to the different level of scattering loss from the sidewall area and electric field (E-field) distribution in both waveguides. From the field distribution shown in Fig. 1(b) and (c), it is obvious that waveguide II has larger sidewall area

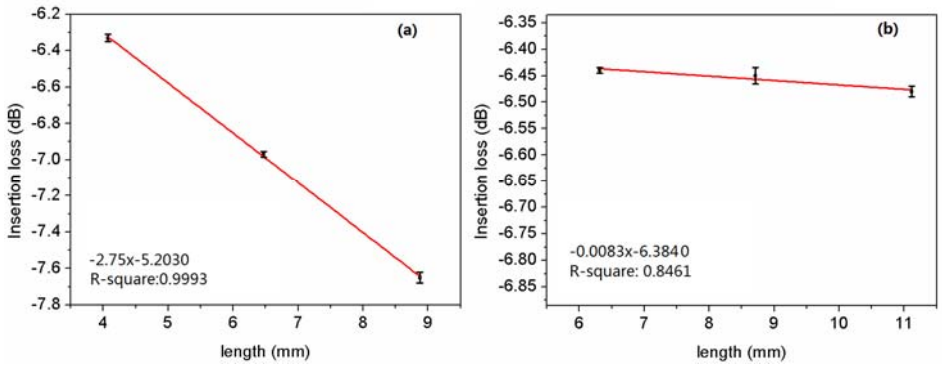

Fig. 3. The loss performance for (a) rib waveguide II and (b) rib waveguide III.

and relatively stronger E-field on the sidewall boundary (although the width of bottom step is deliberately increased to 750 nm), thus introducing larger scattering loss from the etching process induced sidewall roughness. However, for the waveguide III, only the top step has a rough sidewall boundary which is also relatively further away from the mode centre due to wider rib width of 1 μm, and this contributes to the much better loss performance as expected. With the three types of waveguide structures, we design two classes of delay line units named by type S1 and S2 for discussion convenience. Both S1 and S2 delay lines adopt waveguide I as the bend section, but S1 uses rib waveguide II and S2 uses waveguide III for their straight optical path. The top view of our proposed delay line unit layout is illustrated in Fig. 2(b). In our design we vary the structure dimension parameters such as, the track number N, internal bend radius *r* and spacing between neighboring tracks *d*, to characterize the delay property of the proposed delay lines. There are some basic length relations and restriction conditions required as proper design considerations. We list all these relations as below and the design problem is expressed as an optimisation model of Eq. (1) (length unit in μm):

$$\begin{aligned} &\min : \mathrm{Loss}(N, r, d, L, w_s, w_b) \\ &s.t. \begin{cases} delay = 50ps; r \ ? \ 10um; \\ d \ 吵 6um; L \quad 40um(S1); L \ ? \ 600um(S2). \\ S\ bend : L_{sb} = 2 ? \sqrt{30^2 \quad [^{(2r-d)}/_2]^2}; straight : L_s = (2N - 1) ? L \quad L - 60; \\ bend : L_b = p[r + (N - 1)d] / 2 + p(r + Nd) / 2 + [2pr + pd ?(N \quad 1)]N. \end{cases} \end{aligned} \tag{1}$$

Where, N, *r*, *d* and *L* are the structure dimension parameters which are illustrated in Fig. 2(b). The parameters, w_s and w_b are the propagation loss of the straight and bend waveguides which can be obtained by measurement. The objective is to make the loss of delay line as low as possible. It is to be mentioned that, on the internal track, we have used two S bends to bridge the straight and semi-circle bends and the length of each S bend can be approximated with the hypotenuse length of a rectangle as $30 \times (2r\text{-}d)/2$ μm^2. As for the restriction conditions, a minimum internal radius *r* of 10 μm is taken for low loss consideration; the spacing *d* between neighboring track waveguides is selected as 6 μm for good crosstalk isolation. In this case, the direct coupling length is much greater than the straight waveguide length *L*. Taking type S2 as an example, a more intuitive illustration is given in Fig.4. We can observe that the crosstalk is stronger for the waveguide spacing of 2 μm, since it is easy for power coupling to happen between these waveguides. For 6 μm spacing, there appears nearly no crosstalk between the waveguides. For type S1 (S2) delay line, the length of straight waveguide *L* should be larger than 600 μm (40 μm) since the transition taper section is set to 300 μm (20 μm) to guarantee low loss and no high order mode excitation in the transition section. To calculate the total delay of the structure, we should sum the group delay contributed by each section of the delay line unit. The characteristic group delay (per unit distance) of the three types of waveguides is calculated using Lumerical FDTD solutions [13]. For waveguide I, II and III, the characteristic group delay is 1.3529e+7, 1.2834e+7 and 1.2224e+7 ps/ km, respectively. Then, the delay restriction has been written in such a way that the sum of the product of the characteristic group delay and individual waveguides length of bend and straight sections is equal to 50 ps. Through analyzing the optimisation model, it is easy to obtain the conclusion that less number of tracks and shorter bend section can exert better loss

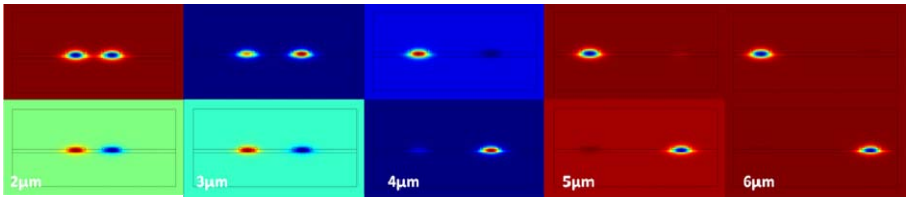

Fig. 4. Crosstalk between two neighboring waveguides versus spacing from 2 to 6 μm.

performance. This is more obvious for type S2 delay lines. The optimisation modeling method can solve sophisticated design cases while more restriction conditions and variations are involved. In this case, the potential optimized parameters can be determined with the help of some optimisation algorithms like genetic algorithm.

3. Fabrication and characterization

We fabricated the silicon waveguide based delay line in silicon-on-insulator (SOI) platform through Institute of Micro Electronics (IME) CMOS fabrication process. The fabrication has been done on an 8 inch SOI wafer with a 340 nm top silicon layer thickness and 2 μm buried oxide (BOX) layer. Thermal oxidation is adopted firstly in order to thin down the silicon layer to 300 nm. The device is patterned by DUV photolithography, followed by a two-step silicon reactive ion etching (RIE) down to the BOX layer. To increase the coupling efficiency between lensed fiber and the device, the waveguide ends were terminated with Spot Size Converters (SSC) having a length 200 μm and tip width 180 nm. The whole structure is finally covered by 1.1 μm silicon dioxide (SiO2) cladding layer. The normal fabrication technologies are used to make the delay line structures, which is compatible with real large-scale production. We have fabricated several different types of delay line units. The microscope photos of the structures are shown in Fig. 5. Two delay line units are labeled as examples to tell the difference between the fabricated type S1 and S2 delay units. The loss performance of the fabricated delay line units have been characterized initially. The loss measurement setup is shown in Fig. 6 (a). The polarization controller is adjusted to make the system work at TE polarization. A Power Meter (PM) has been used for the fiber-to-chip alignment and to record the received optical power. The spectral property is characterized by an optical spectrum analyzer (OSA). The different delay line units are labeled as delay line type (S1 or S2) followed by {N, *r*, *d*, *L*}. With reference to the fiber to fiber coupling loss, the measured insertion loss and spectral response for several kinds of delay line units are shown in Fig. 7. Fig. 7(a) is the measurement result for delay unit S2 {2, 10μm, 6μm, 969.229μm}. Through a linear fit to the graph between insertion loss versus the number of delay line units,

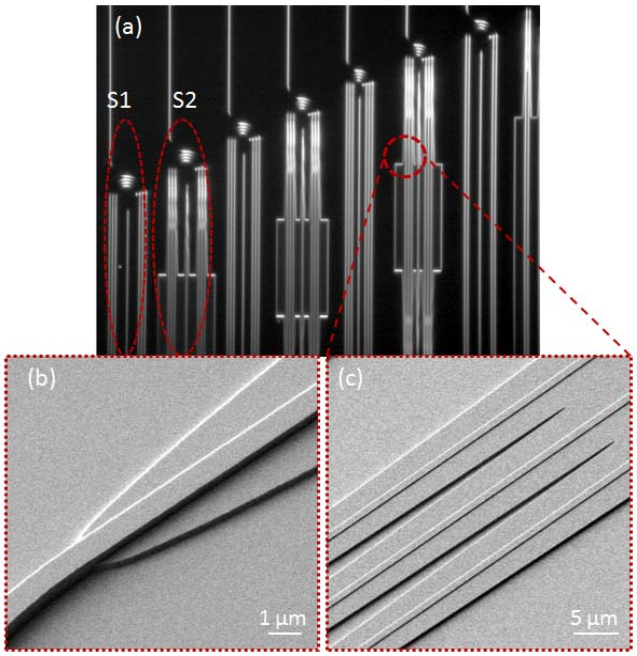

Fig. 5. The microscope photos of the proposed delay line units the structure top view (a) and the details (b) and (c).

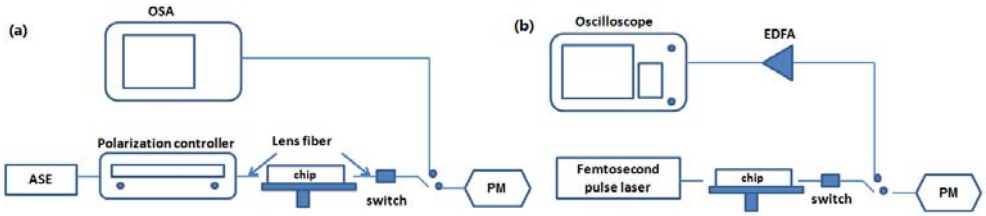

Fig. 6. (a) loss measurement setup and (b) group delay characterization setup.

an excess loss of ~0.7 dB per unit is achieved. The inset of Fig. 7(a) shows the recorded spectrum for the delay line with 1, 2 and 3 units. The fringe free spectrum indicates a wideband performance without any high order mode excited. Likewise, Fig. 7(b) and (c) illustrate the measurement results for delay line S2{3, 10µm, 6µm, 619.168µm} and S1{3, 10µm, 6µm, 619.168µm} with an excess loss of about 1.15 dB per unit and 2 dB per unit, respectively. Note that we have used the same straight waveguide length for type S1 and S2 delay lines due to close characteristic group delays of waveguide II and III. The spectral responses have shown a wideband operation. It is obvious that the type S2 delay units has better loss performance than S1 since they use much lower loss rib waveguide III. For type S2 delay lines, most of loss is introduced by the bend waveguide section. The measurement results also indicate that decreasing the number of tracks (i.e. reduce the length of bend section) will improve the excess loss performance, as predicted by the optimisation model.

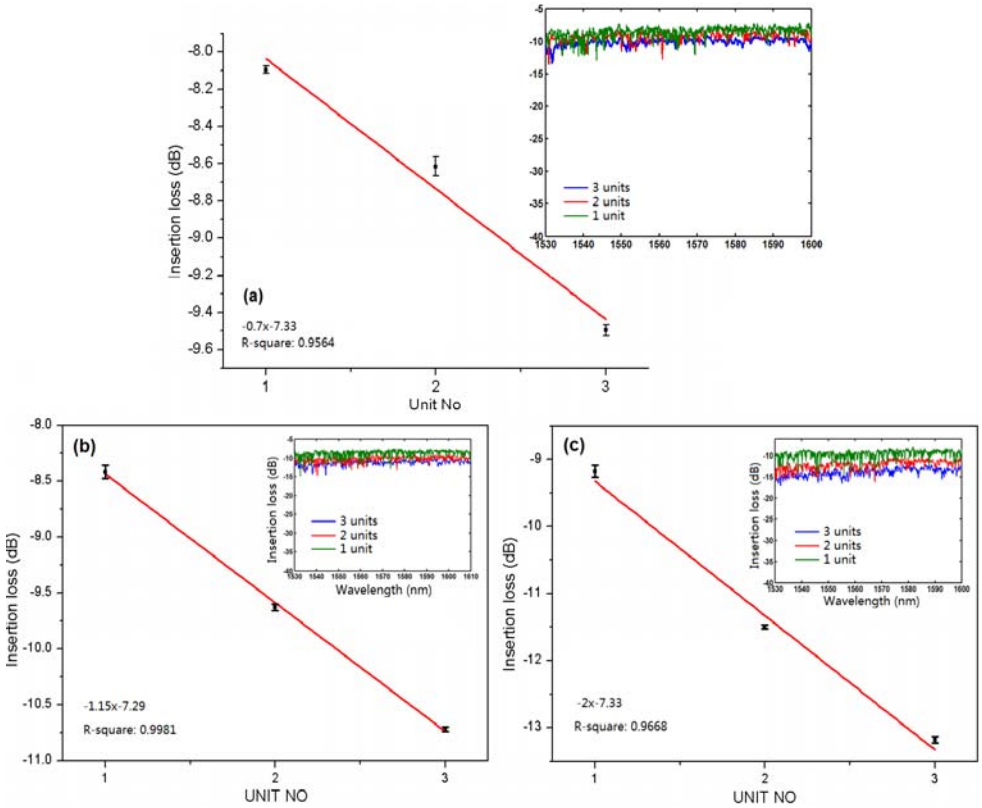

Fig. 7. The excess loss measurement for several type of delay units (a) S2 {2, 10µm, 6µm, 969.229µm}, (b) S2 {3, 10µm, 6µm, 619.168µm} and (c) S1 {3, 10µm, 6µm, 619.168µm}.

Then, we further characterize the delay property of the proposed delay line units using direct time domain method measurements. The measurement setup is illustrated in Fig. 6(b). We have used a femtosecond pulsed laser as light source with a fast optical oscilloscope to detect the amplified pulses from the delay line waveguides with 1, 2 and 3 delay units. Here, power meter is used only for fiber-to-chip alignment. We measured S2 type delay lines for their better loss performance. The measurement results of abovementioned S2 {2, 10μm, 6μm, 969.229μm} and S2 {3, 10μm, 6μm, 619.168μm} delay lines are shown in Fig. 8. It can be seen that the uniform intervals between two neighboring pulse is around 50 ps. By fitting the delay measurement results, it is clear that S2 {2, 10μm, 6μm, 969.229μm} gives 50 ps delay and S2 {3, 10μm, 6μm, 619.168μm} introduces about 52 ps delay. The observed delay variation mainly comes from the possible measurement reading error (due to the broadened pulses because of system bandwidth limitation) and the fabrication imperfection such as geometry deformation. We have measured many fabricated delay line samples from two batches of fabrications, and observed that the delay variation is within 3 ps.

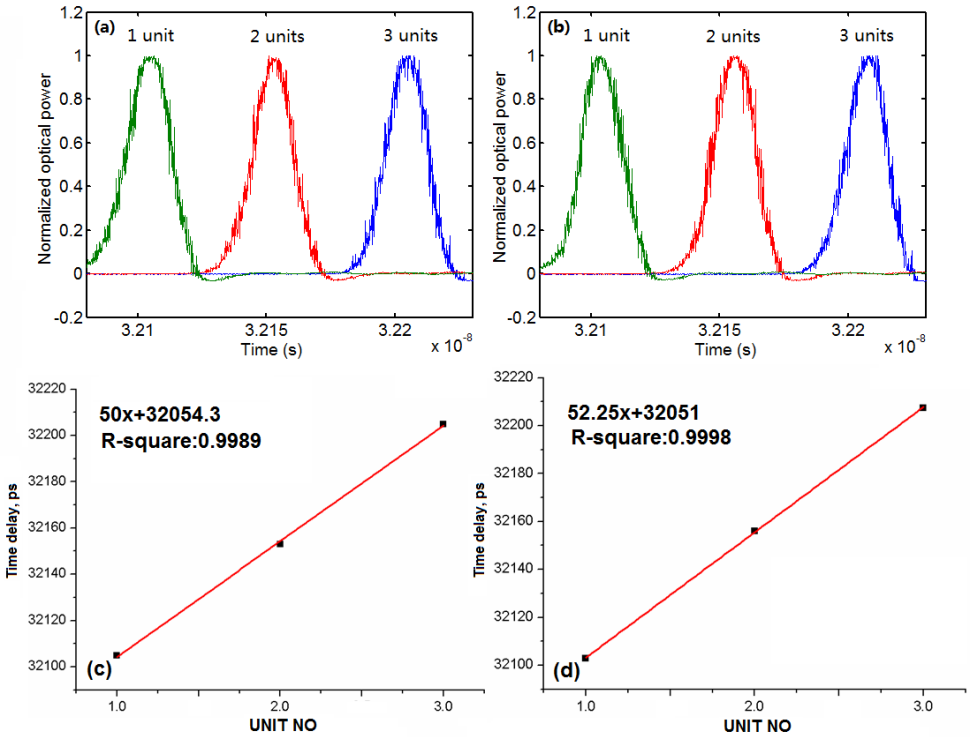

Fig. 8. The pulse delay measurement for delay units: (a) and (c) for S2 {2, 10μm, 6μm, 969.229μm}; (b) and (d) for S2 {3, 10μm, 6μm, 619.168μm} through 1, 2 and 3 delay units.

4. Conclusion

In summary, we have designed and demonstrated several 50 ps delay line units on a 300 nm silicon platform. The general approaches and critical considerations are summarized for silicon waveguide based passive delay line design and optimisation. Both the loss and delay performances have been characterized. We have demonstrated a low propagation loss of 0.7 dB per unit for 50 ps delay line unit.

Acknowledgments

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