A 29-31GHz, 0.4dB Amplitude Error & 1^0 Phase Error Beamforming IC and 20dB Dynamic Range Power Detector for SatCom Phased Arrays

Robin Kalyan[#], *Member, IEEE*, Yong-Joon Jeon[#], Yan Dan Lei, Chan Kuen Sim, Md Arif Ansari Hussain, *Member, IEEE*, Nur Aisyah Kuyob, Raja M Kumarasamy, *Senior Member, IEEE*, and Kevin Chai Tshun Chai, *Member, IEEE*

***Abstract*— This paper proposes a 30GHz beamforming transmitter IC (BFIC-Tx) with a compact power detector (PD). The PD utilizes a trace around the output GSG pad of BFIC-Tx, thus, does not need dedicated on-chip coupler area. Such PD enables closed loop power control thus, (i) enables power efficient phased arrays that are capable of adapting radiated power depending on scan losses; (ii) keeps the radiated signal within the emission limits spatially (side lobes) and spectrally (emission mask). In addition, proposed BFIC-Tx employs a modified Gilbert cell like single stage linear-in-dB variable gain amplifier (VGA) which provides 15.5dB gain range (5bits), 0.5dB resolution & 180^0 phase shift. Proposed PD has a 20dB dynamic range with only 0.3dB temperature drift across -40 to +85^0C. BFIC-Tx achieved state-of-art RMS gain error of <0.4dB, RMS phase error of <1.0^0, phase resolution of 5.6^0, PAE >10% at P_{1dB} of 11.4dBm.**

***Index Terms*— SiGe, BiCMOS, millimeter wave, beamforming, phased array, transmitter, SatCom on the move, 5G, Inter-satellite link.**

I. INTRODUCTION

3GPP study group [1] has laid out guidelines for 5G base stations in satellites to enable everytime everywhere broadband connectivity (maritime, in-flight etc). To fully exploit the potential, all the future satellite communication (SatCom) systems need to have phased array systems with narrow beamwidths (1-6^0) and wide scan angles up to 70^0 [2] – [4].

In a phased array, scan loss increases as scan angle increases, e.g., it is 3dB at 50^0 and 6dB at 70^0 [5]. A brute force way to compensate for scan loss is to increase the effective isotropic radiated power (*EIRP*) either by increasing the Tx output power (P_{OUT}) of each BFIC/antenna or by increasing the array size. Both approaches are highly power inefficient, with exponential increase in heat dissipation, challenging cooling solutions. This can be resolved by detecting individual P_{OUT} using power detectors (PD) and then regulate each P_{OUT} according to scan angle by controlling the bias current/voltage of BFIC-Tx. In this manner, BFIC-Tx and ultimately phased array output power adapts to the scan loss without compromising on power added efficiency (PAE). Moreover, such mechanism in a phased array allows better amplitude control (tapering) for optimal side lobe suppression. However, PD employs $\lambda/4$ based lossy/bulky couplers [6] – [7], thus, occupying significant chip area and are not affordable in BFICs whose area is restricted by the narrow ($\lambda/2$) pitch in phased arrays [5]. For example, the coupler area in [2] is about 25,000μm^2 which can be up to 25% of a BFIC-Tx. In [3], broadside coupling and parasitic substrate capacitors were utilized to significantly reduce the coupler area to 1600μm^2, yet this area is unaffordable in BFICs and is not employed in recent works [8] – [12].

Thus, this paper presents a temperature compensated PD with a compact coupler embedded in the output GSG pad, and thus, doesn't need a dedicated chip area. To best of our knowledge, such method of compact coupling is employed for the first time. Moreover, this paper presents a modified gilbert cell topology for VGA to overcome the limitations of conventional topologies [13] – [14]. The proposed VGA provides process/temperature independent 15.5dB linear-in-dB gain range in single stage by exploiting the exponential I_C-V_{BE} behaviour of BJTs. The remainder of this brief is organized as: Section II presents the system level analysis of overall phased array. Section III presents circuit description of proposed BFIC-Tx followed by results and discussion in Section IV.

II. SYSTEM LEVEL CONSIDERATION

To maintain single beam geostationary earth orbit (GEO) link or a multi-beam medium earth orbit (MEO) link for SOTM (SatCom on the Move) application, desired *EIRP* is of the order of 53dBW [2] – [3]. To achieve such high *EIRP*,

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[#]Robin Kalyan and Yong-Joon Jeon jointly shares the first authorship. Yong-Joon Jeon is presently with Qualcomm Inc, 4243 Campus Point Ct, San Diego, CA 92121, USA (email: yjjeon813@gmail.com)

Robin Kalyan, Yan Dan Lei, Chan Kuen Sim, Nur Aisyah Kuyob, and Kevin Tshun Chuan Chai are with the Institute of Microelectronics (IME), Agency for Science, Technology and Research (A∗STAR), 2 Fusionopolis Way, Innovis #08-02, Singapore 138634. (email: {robin_kalyan, yandl, sim_chan_kuen, nur_aisyah_binte_kuyob, chaitc}@ime.a-star.edu.sg)

Raja M. Kumarasamy is presently with Maxlinear Inc, 5966 La Place Ct Ste 100, Carlsbad, CA, USA, 92008 (e-mail: ksraja69@gmail.com).

Md Arif Ansari Hussain is presently with Huawei, Bouna Vista, Singapore 139345. (email: ahussainiitk@gmail.com)

TABLE I
ESTIMATED P_{OUT} AND P_{DC} FOR SOTM BFIC TX.

SOTM Scan Angle → ***Parameter ↓***	***≤55⁰ Scan***	***55⁰ - 70⁰ Scan***	***≤55⁰ Scan***	***55⁰ - 70⁰ Scan***
EIRP, dBW/dBmi	53.0/83.0	53.0/83.0	53.0/83.0	53.0/83.0
Array size, H×V ***(#*** / mm^2) @29GHz	*64×64 /* *320×320*	*96×96 /* *480×480*	*75×75 /* 375×375	*110×110 /* 550×550
# of antenna (*N*)	4096	9216	5625	12100
≈***P*$_{OUT}$*****,** dBm	13.0	12.5	10.0	10.0
P_{DC} of all BFICs in array[#] (@10% efficiency), kW	1.64	3.29	1.13	2.42
Beamwidth, °	1.9	1.3	1.7	1.1

*Using (1), considering G_e = 4.5dBi, *FL* = 1.0dB and *SL* + *TL* of 3.2dB+2.5dB @ 55^0, 6dB+6.2dB @ 70^0, respectively [2-5], [15].
[#]Dual-polarized array where each antenna element is fed by two independent PAs/RF chain, one each for H and V polarization, respectively.

phased array systems seem a promising solution which give a theoretical 4x improvement in EIRP for every doubling of the array size, since the power from BFIC-Tx chain goes up by 2x while the directivity/gain of antenna array also goes up by 2x. Mathematically, *EIRP* of a phased array can be written as:

$$EIRP = 20log_{10}N + G_e + P_{OUT} - Losses \quad (1)$$

where N is the number of antennas, G_e is the gain of each antenna, P_{OUT} is the output power of each amplifier/Tx chain. *Losses* in (1) include feed loss (*FL*), scan loss (*SL*), and tapering loss (*TL*). Typical values of G_e, P_{OUT} and *Losses* are considered for a linear phased array as given in footnote of Table I.

Thus, to achieve 83.0dBmi of *EIRP* at 55^0 scan angle will require P_{OUT} = 13dBm for N = 4096 (64x64 array), as can be calculated using (1). For P_{OUT} of 13dBm each Tx chain will have a DC power consumption (P_{DC}) of 0.2W @10% PAE, which translates to 1.63kW of P_{DC} for all BFICs in a dual-polarized phased array. These numbers are reported in column 2 of Table I. On the other hand, to achieve same *EIRP* of 83.0dBmi using an array of 75x75 antennas will need P_{OUT} of 10dBm with 1.13kW of P_{DC} of all BFICs in array as reported in column 4 of Table I. Thus, 75x75 phased array is ≈30% power efficient as compared to 64x64 phased array for scan angles ≤ 55^0. Similar is the conclusion for 55^0-70^0 scan angles as can be observed by comparing columns 3 and 5 of Table I. Further increase in array size will reduce the P_{OUT} and the total P_{DC} of all BFICs in array, however, such large, phased arrays are mainly limited by cost, size, weight, and regulatory requirements on installation. Thus, P_{OUT} per Tx. chain of 10-13dBm is desirable to meet the EIRP requirement along with optimal PAE, cost, and size of overall phased array.

III. CIRCUIT DESCRIPTION

The beamforming transmitter IC as shown in Fig. 1 is fabricated in 0.13µm SiGe process. Core area of chip is 2.45 x 0.85 mm^2.

A. Power Amplifier (PA)

Fig. 2 shows the schematic of proposed PA consisting of pseudo-differential driver and power stages. Driver stage uses cascode topology for higher gain, whereas, for power stage

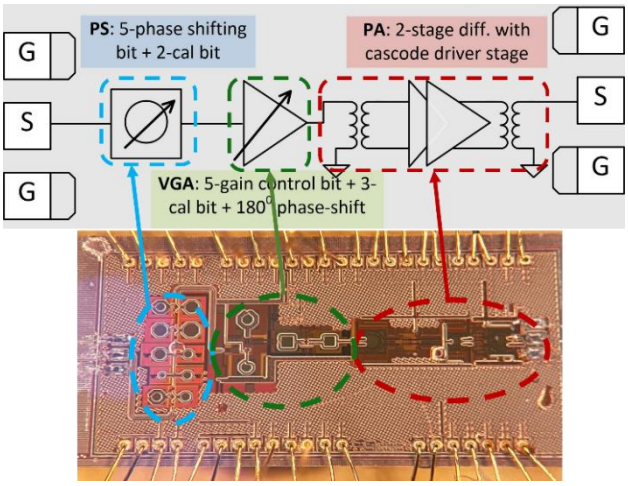


Fig. 1. Block diagram (top) and die micrograph of proposed (bottom) beamforming transmitter IC. Core chip area is 2.45x0.85mm^2

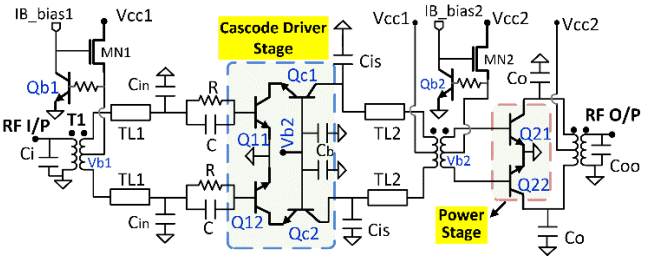
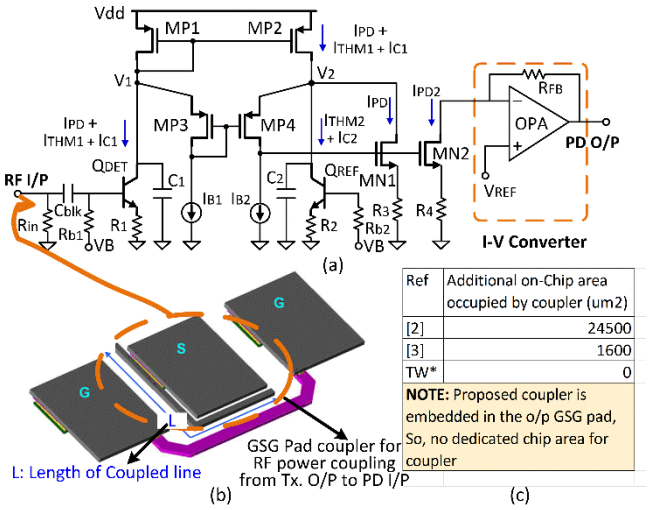


Fig. 2. Schematic of proposed 30 GHz PA. R = 30 Ω & C = 0.25pF, Ci = 0.2pF, Coo = 0.17 pF, Cin = 0.16pF, Cb = 0.5pF, Cis =0.07pF, Co = 0.08 pF, TL1: W/L = 15/40um, TL2: W/L = 15/130um



Ref	Additional on-Chip area occupied by coupler (um2)
[2]	24500
[3]	1600
TW*	0

NOTE: Proposed coupler is embedded in the o/p GSG pad, So, no dedicated chip area for coupler

Fig. 3. Schematic of proposed temperature compensated PD with coupler embedded in the RF ouptut pad.

common-emitter topology is utilized to maximize power extraction per unit transistor size. In addition, parallel power combining in power stage provides better linearity as compared to stacked/cascode topologies. Transistors Q11, Qc1, Q22, Qc2 are of 30um size. Transistors Q21 & Q22 are of 60um size to achieve the targeted OP1dB of >11 dBm. Detailed schematic of proposed PA along with all component values/dimensions is shown in Fig. 2.

B. *Temperature Compensated Power Detector (PD)*

Fig. 3(a) shows the schematic of proposed temperature compensated PD. Fig. 3(b) shows the arrangement of RF coupling from Tx/PA output to PD input using proposed pad coupler which is a trace embedded in the output GSG pad. Therefore, it doesn't occupy any additional chip area, thus, suitable for implementation in BFICs whose area is restricted by the narrow ($\lambda/2$) pitch in phased arrays. Fig. 3(c) shows the table for additional chip area occupied by the couplers in reported and proposed works. One can see from Fig. 3(c), by using proposed methodology there is an area saving of 1600 um^2 – 25000 um^2 compared to the state-of-art.

Q_{DET} & Q_{REF} (Fig. 3a) are of same size and operate under same bias conditions (V_B, V_1 & V_2) due to current mirrors formed by MP1-MP4. This ensures that Q_{DET} & Q_{REF} have same common mode currents, i.e., $I_{THM1} = I_{THM2}$ & $I_{C1} = I_{C2}$. Under such condition, current (I_{PD}) which is proportional to input power to PD will flow through transistor MN1 as shown in Fig. 3(a). I_{PD} is then scaled/amplified by transistor MN2 to I_{PD2}. Finally, an OPAMP based I-V converter is used to get an output voltage proportional to coupled power. The proposed PD demonstrates 20dB dynamic range from -5 to +15dBm with a temperature drift of only 0.3dB from -40 to +85^{0}C.

C. *Variable Gain Amplifier (VGA)*

Schematic of modified Gilbert cell like VGA with inbuilt 180^0 phase shifting feature and additional buffer stage is shown in Fig. 4. Transistor Q1 forms the 1st stage with L1 & C1 providing the input matching. Since, the biasing of Q1 is fixed and doesn't change with different gain states, input return loss of VGA is almost fixed. Variable gain is provided by changing the current difference of Q6 & Q7 (I_{Q6}-I_{Q7}) which in turn changes the current difference of Q2 & Q3 as per (2).

$$I_{Q2} - I_{Q3} = (I_{Q6} - I_{Q7}) * I_{Q1}/(I_{Q6} + I_{Q7}) \quad (2)$$

The current relationship in (2) is due to the translinear circuit formed by transistor pairs Q2-Q3 & Q6-Q7 [16]. While keeping a constant I_{Q6}+I_{Q7}, changing the differential currents I_{Q6}-I_{Q7} will result in changing the gain of the VGA. When the differential currents I_{Q6}-I_{Q7} take on negative values, signal undergoes 180^0 phase shift. I_{Q6}+I_{Q7} is mirrored to form total current of the differential pair Q2 and Q3, which is equal to I_{Q1} set by vbias1. I_{Q6} and I_{Q7} varies exponentially with the control word which determines respective V_{BE}. Thus, gain which is proportional to (I_{Q6}-I_{Q7}) varies in a linear-in-dB fashion with control word [16].

The cascodes (Q4-Q5) provides the isolation between the output and devices (Q2-Q3), thus, helps in reducing RMS phase errors for different gain settings. Transformer T1 will convert the differential outputs back to single ended. Q8 and Q9 acts as a buffer with fixed gain, and hence, output impedance is also isolated from variable gain 2nd stage. Thus, a compact input & output impedance (return loss) resilient gilbert-cell like VGA providing 15.5 dB gain control in 0.5 dB steps (5bits), with additional 3bits for calibration and 180^0 phase shift is proposed here. This VGA including the buffer stage shown in Fig. 4, consumes only 13.2mW power and occupies 0.2mm^2 in area.

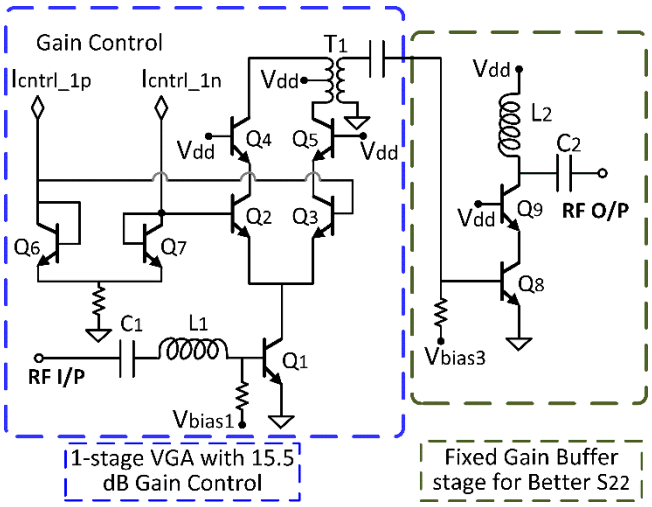


Fig. 4. Schematic of Modified Gilbert Cell like VGA with inbuilt 180^0 phase shift and additional buffer stage.

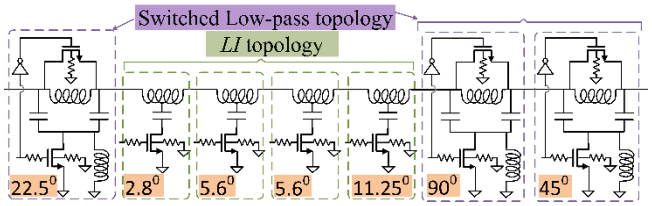


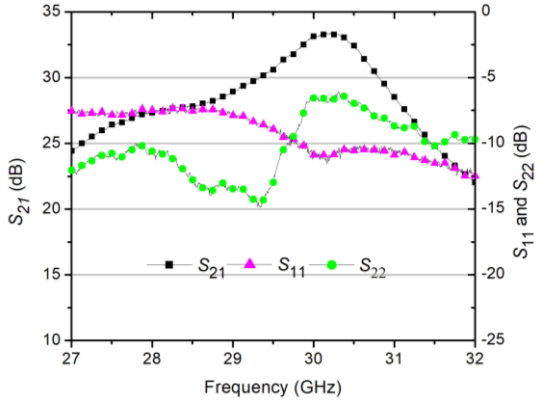
Fig. 5. Schematic of proposed PS.

D. *Phase Shifter (PS)*

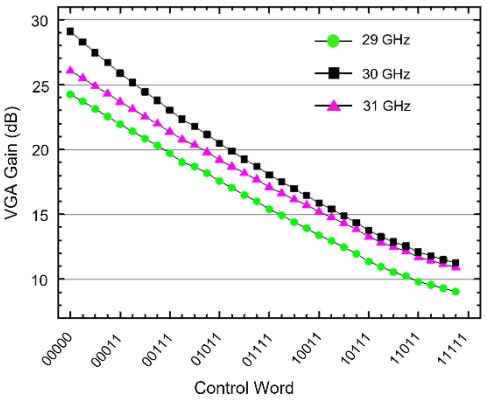
Fig. 5 shows the schematic of proposed PS which consists of 5-bits for phase shifting and 2-bits (2.8^0 and 5.6^0) for calibration. Loaded inductor (LI) topology as shown in Fig. 5 is used for 11.2^0, 5.6^0, and 2.8^0 cells. Characteristic impedance and phase shift are given by $Z_o = \sqrt{L/C}$ and $\theta = \pm\omega\sqrt{LC}$ respectively. Phase shift is achieved by changing C, however, it also changes Z_o as L is fixed, and hence, return loss is different in two phase states. To minimize the change in return loss (or Z_o) in two phase states, only LSBs are implemented using LI topology, so that change in C and Z_o is minimal. As shown in Fig. 5, switched filter topology is used for 90^0, 45^0 and 22.5^0 cells. The cells are ordered such that reflections between the cells is minimal so that overall return loss and phase shift is not affected by loading. All the shunt switches are implemented in triple-well n-MOSFET to reduce the leakage in OFF state.

IV. Result and Discussion

Measured results are shown in Figs. 6(a)-(f). Fig. 6(a) shows the measured S-parameters of proposed BFIC-Tx chip at max. gain and 0° phase settings. Small signal gain (S_{21}) of 32.5dB with 3-dB bandwidth from ~29-31GHz is achieved. Measured S_{11} and S_{22} are better than -10dB and -6dB, respectively over this band. As shown in Fig. 6(b), measured 15.5dB of linear-in-dB gain range & 0.5dB gain resolution with three more bits for calibration is achieved with only one stage VGA, which is state of the art. It is worth mentioning here that the VGA provides an 180^0 phase shift owing to its



(a)



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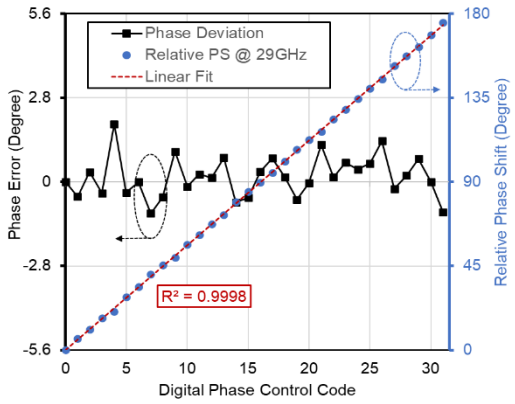
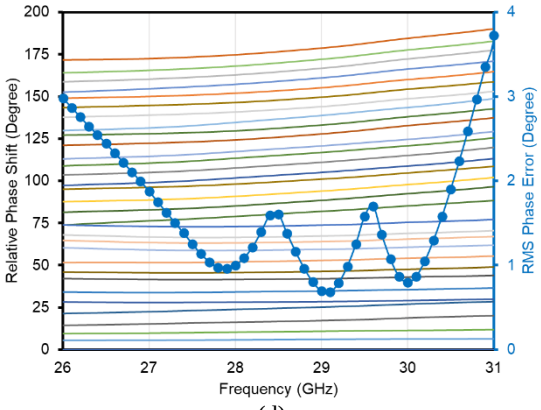
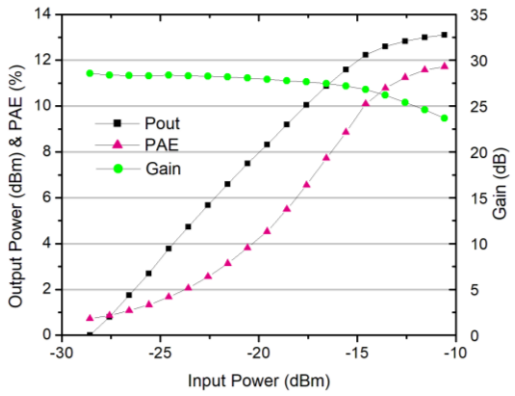


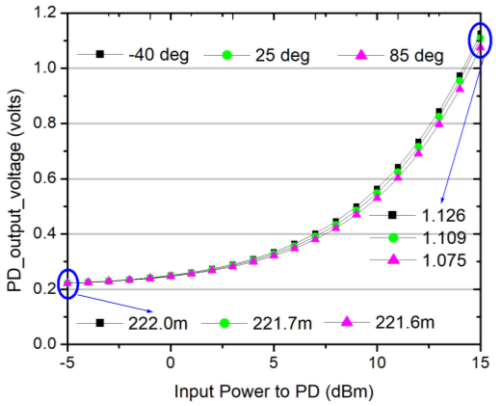
(c)



(d)



(e)



(f)

Fig. 6. Measured results of BFIC-Tx (a) *S*-parameters (b) VGA gain vs control bits (c) PS phase response vs frequency for different control bits (d) PS relative phase and phase error *vs* control bit after calibration (e) Output power, gain, PAE vs input power at 30GHz (f) Output voltage of power detector for -40^{0}C, 27^{0}C and 85^{0}C.

differential nature, thus, reducing 1-bit in PS (Corresponding to 180^0 phase) implementation. Figs. 6(c)-(d) shows the phase shifter response. Fig. 6(c) shows the phase error and relative phase shift vs control words at 29GHz. From Fig. 6(c), one can see an almost linear phase shift response with max. phase error of <2° at 29GHz. Fig. 6(d) shows phase response with 180^0 phase shift range from 26-31GHz with 5.6° phase resolution. One can also see from Fig. 6(d) that <1° of RMS phase error is achieved at calibrated frequencies (28GHz, 29GHz & 30GHz) which is state-of-art for transmitters reported with 6-bit phase shifters [11] – [12]. It is worth mentioning here that depending on the requirement, calibration frequency can be changed to minimize the RMS phase error for any operating band in the entire phase shifter operating range of 26-31GHz. Fig. 6(e) shows that P_{1dB} and P_{SAT} of 11.4dBm and 13.5dBm, respectively are achieved. Although these power levels are lower than the other references such as [8] – [12], which inherently lowers the achievable PAE for overall BFIC-Tx, yet such power levels (10-13dBm) results in lower system power consumption as described in section II. As can be deduced from Fig. 6(f), the proposed temperature compensated PD achieves 20dB dynamic range with only 0.3dB temperature drift. Fig. 7 shows the modulated signal measurement setup.

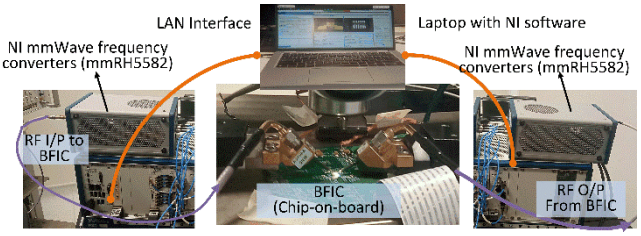


Fig. 7. Modulated signal measurement setup

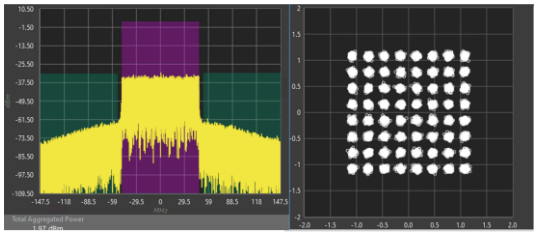


Fig. 8. Spectrum and constellation with 64-QAM signal for max. gain & 0^0 phase setting. Data rate = 600 Mbps. Measured Pavg = 5.75dBm, EVM= 4.2%, ACLR=-33.8dBc, ACPR=-33.4dBc.

NI-PXI vector signal transceiver with mmWave frequency converters up to 44GHz (mmRH-5582) is used to generate & capture the 64-QAM, 600 Mbps modulated signal at 30 GHz with a peak-to-average power (PAPR) of ≈6.5dB. Measured modulated results using 64-QAM signal result into an EVM of 4.2%, ACLR of -33.8dBc & ACPR of -33.4dBc as can be seen from Fig. 8. The corresponding average power level is about 5.5dBm which is 6dB back-off from P_{1dB}.

V. Conclusion

This paper presented a 29-31GHz BFIC-Tx IC with P_{1dB} of 11.4dBm which helps in minimizing overall phased array power consumption as described in Section II. Proposed IC utilizes a compact 5-bit linear-in-dB Gilbert-cell like VGA that provides 15.5dB gain control in single stage with additional 3-bits for calibration. Moreover, the proposed VGA also provides 180^0 phase shift, thus, helps in minimizing the number of dedicated phase shift bits required in phase shifter. The proposed compact PD with a novel coupler as presented in this paper does not need dedicated chip area and provides 20dB power detection range which can be used to adjust the bias voltages and currents of PAs. Such voltage/current control will in turn control/adapt the output power of each BFIC Tx for different scan angles without compromising on the PAE. The power control not only enables power efficient phased arrays with wide scan angles but also helps to meet emission requirements in terms of side lobes and spurious.

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