Characterization of Differential TMV Vertical Interconnects to 50GHz with Double Side Measurement

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Abstract

Fan-Out Wafer Level Packaging (FOWLP) can be a good candidate for heterogeneous integration of Photonic ICs (PIC) and Electronic ICs (EIC) in the same package to achieve low interconnect loss, low power consumption, and small factor for optical communications requiring high data transmission. The vertical interconnects Through Mold Via (TMV) in FOWLP can be utilized for the RF routing from frontside to backside vertically. The conventional way of characterizing the RF performance of vertical interconnects is to de-embed the vertical section by measuring a back-to-back structure with multiple de-embedding structures. In this paper, differential TMV structures in GSSG configuration are characterized by direct measurement using double-side probing techniques from DC to 50GHz. Three GSSG TMV interconnects with different TMV pitches are measured and compared. The 100Gbps PAM4 eye diagrams of the interconnects are also shown.

Introduction

Optical communication applications demanding higher data transmission rate and bandwidth like hyper-scale data centers, high performance computing, and machine learning have driven the need for integrating the PIC and EIC in the same package to achieve low interconnect loss, low power consumption and small form factor [1-3]. To achieve this, a heterogeneous integrated Optical Engine (OE) in advanced FOWLP was demonstrated in [4-6]. Fig. 1 shows the cross-section of a typical OE package. The PIC is integrated into the molding compound with the EIC flip-chip connected on top of the package. The connections between PIC and EIC are through µBumps and vias. Signals between OE and Application-Specific Integrated Circuit (ASIC) are then routed on the package substrate. For the RF signals to be routed from frontside to backside, vertical interconnects, Through Mold Vias (TMVs), and multi-layer Redistribution Layers (RDLs) are used here. To understand the RF performance and the data transmission capability of the interconnects in OE package, interconnects of GSSG differential configuration as shown in Fig. 2 were designed and fabricated.

The conventional way to characterize vertical interconnects is to measure the back-to-back structures followed by the extraction of the vertical interconnects. In [7], single-ended Through Mold Vias (TMV) performance was extracted using L-2L de-embedding method. In [8], 2-lines de-embedding method was applied to extract the single-ended BGA transitions up to 40GHz. L-2L de-embedding method was also applied for the extraction of differential TSVs to 25GHz in [9]. The de-embedding methods normally require measurements of multiple de-embedding structures and has accuracy and

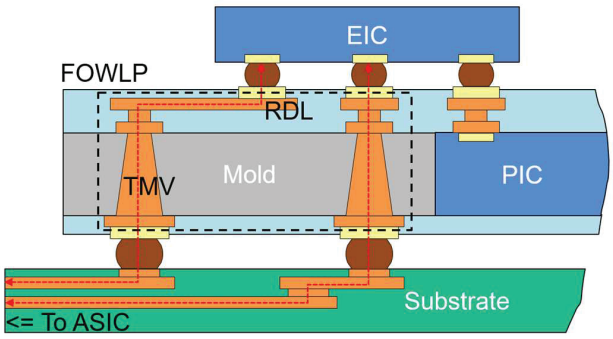

Fig. 1 Cross section view of the heterogeneous integrated OE in FOWLP with TMVs to route the RF signals from frontside to backside.

frequency range limitations. To accurately characterize the vertical interconnects RF performance, double-side probing that directly measures the vertical interconnects can be used. In [10], single-ended vertical interconnects were measured using double-side prober up to 40GHz. TSVs in differential configuration were double-side measured up to 40GHz in [11].

In this work, differential vertical interconnects TMV structures as shown in Fig. 2 were measured up to 50GHz using GSSG probes. The 100Gbps PAM-4 eye diagrams were obtained in Keysight Advanced Design System (ADS) channel simulator with the measured S-parameters imported.

Double-side Probing Setup

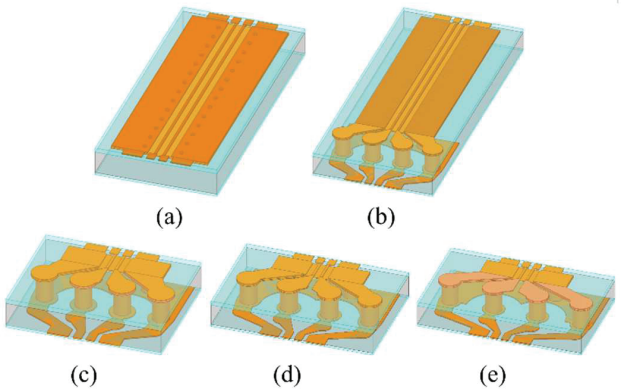

Fig. 2 3D model of the measured structures. (a) 2mm long frontside GSSG CPWG. (b) 2mm CPWG connected with the GSSG TMV interconnect. (c) GSSG TMV with a TMV pitch of 300µm. (d) GSSG TMV with a pitch of 350µm. (e) GSSG TMV with a pitch of 400µm.

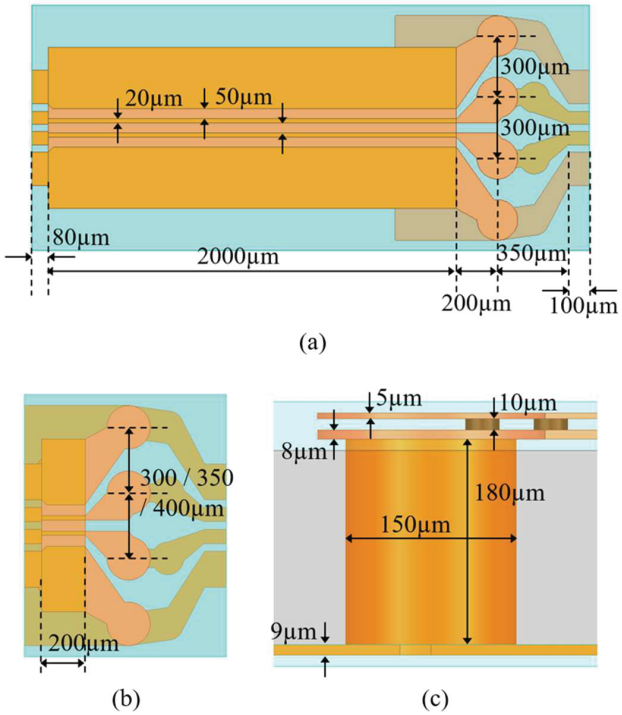

Fig. 3 (a) Dimensions of the RDL with TMV. (b) Dimensions of the TMV vertical interconnects. A 200um long RDL is added at the frontside. (c) Cross-section view of the FOWLP stackup.

Fig. 2 shows the 3D model of the fabricated structures. Fig. 2(a) is a GSSG RDL in CPWG configuration with a length of 2mm on frontside. The CPWG has a signal line width of 20µm with the signal-to-ground gap and signal-to-signal gap of 50µm. The RDL was measured using conventional top-side probing. Fig. 2(b) is the 2mm RDL added with the GSSG TMV to route the signal from frontside to backside. The GSSG TMV has a pitch of 300µm. Fig. 2 (c) to (e) are three GSSG TMVs with a TMV pitch of 300µm, 350µm, and 400µm, respectively. GSSG probes with a pitch of 100µm were used for both top-side and double-side probing. Probing pads and transitions are added at two ends of the interconnects for the probing of 100µm pitch probes as can be seen from Fig. 3 (a) and (b). Fig. 3(c) shows the cross-section view of the FOWLP stackup. The frontside two metal layers have a thickness of 8 and 5µm respectively with a via of 10µm height. The backside metal layer has a thickness of 9µm. The total height of the TMV is 180µm.

Fig. 4 illustrates the setup of the double-side probing. The center of the probe station chuck has a rectangular cavity for the bottom probe to probe on the backside of the vertical interconnects. The probes are connected to VNA with coaxial cables. Short-Open-Load-Reciprocal (SOLR) calibration method was applied to calibrate the probes, cables, and VNA from DC to 50GHz.

Measurement Results and Analysis

Fig. 5 shows the photo of the fabricated structures. Fig. 5(a) to (e) are the frontside photos of the 2mm RDL, 2mm RDL with TMV, and TMVs of different pitches. Fig. 5(f) to (h) are the photos of the backside of the TMV vertical interconnects. Fig. 6 compares the simulated and measured differential return loss

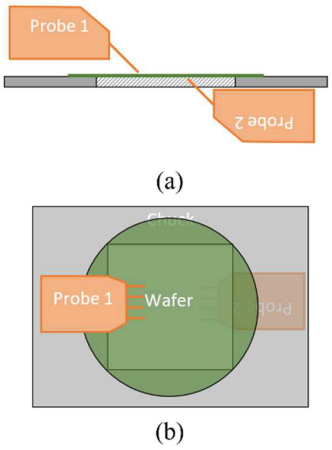

Fig. 4 Double-side probing setup for measurement of vertical interconnects. (a) Side view. (b) Top View. Wafer is placed on the chuck which has a rectangular cavity in the center.

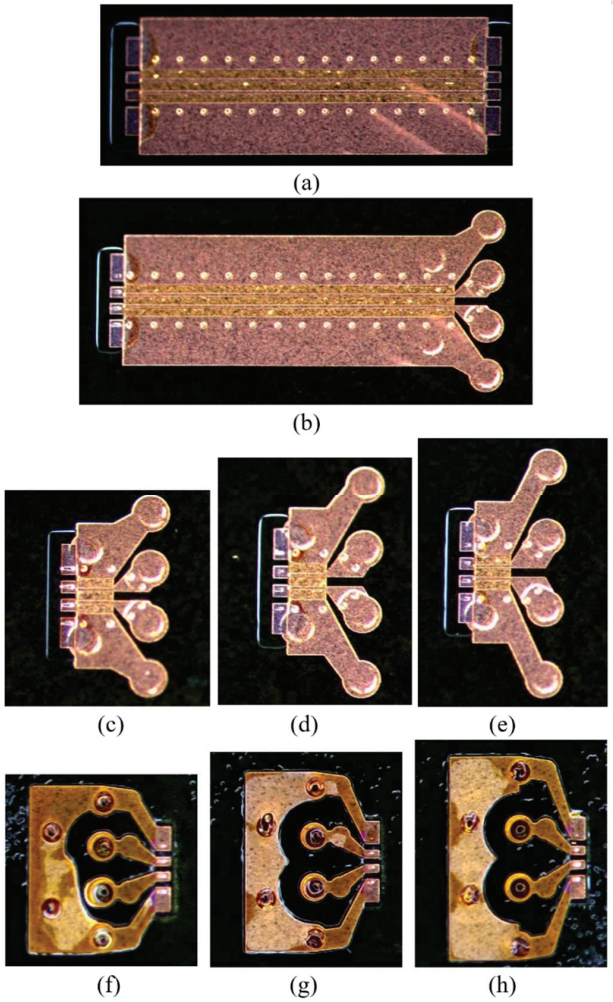

Fig. 5 Photos of the fabricated TMV structures. (a) 2mm long GSSG CPWG on frontside. (b) Frontside of the 2mm RDL with TMV interconnects. (c) to (e) Frontside of the GSSG TMV vertical interconnects with a pitch of 300, 350, and 400µm, respectively. (f) to (h) Backside of the GSSG TMV vertical interconnects.

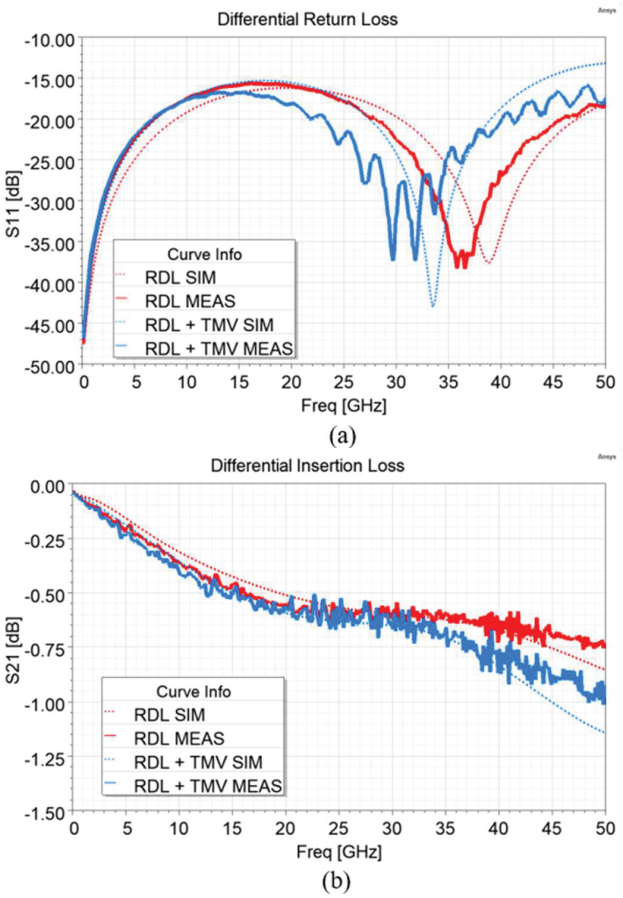

Fig. 8 Simulated and measured S-parameters of the frontside RDL and RDL with vertical TMV interconnects from DC to 50GHz. (a) Differential S11. (b) Differential S21.

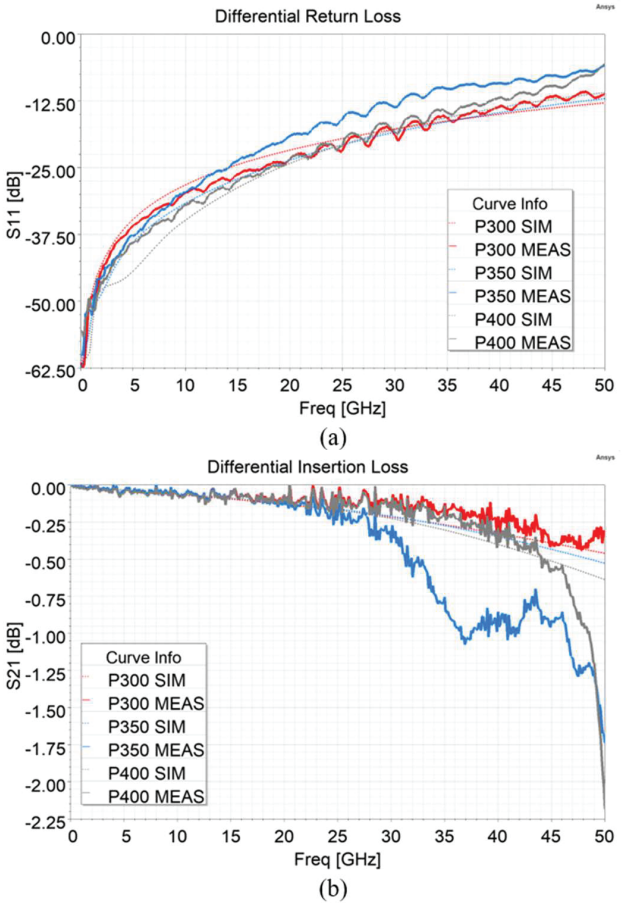

Fig. 6 Simulated and measured S-parameters of three GSSG TMV vertical interconnects with TMV pitch of 300, 350, and 400µm. (a) Differential S11. (b) Differential S21.

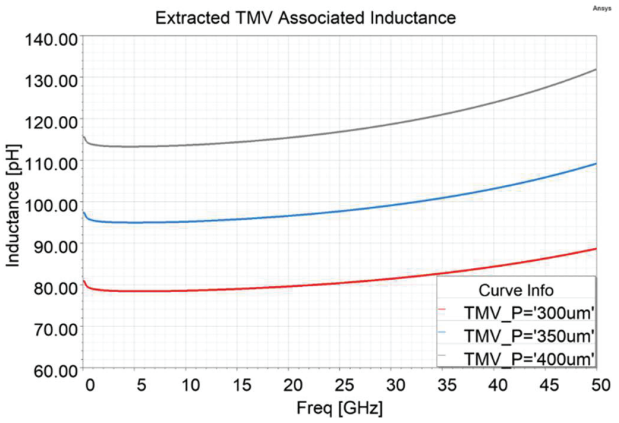

Fig. 7 TMV associated series inductance extracted from simulation model for different TMV pitches of 300, 350, and 400µm.

and insertion loss of the 2mm RDL and 2mm RDL with TMV from DC to 50GHz. Solid lines are the measured results while dashed lines are the simulation results. For both differential S11 and S21, the measured data and simulation model can match well from DC to 50GHz. The red lines are the results of RDL, and the blue lines are RDL with TMV. As can be seen from Fig. 6(a), after adding the vertical TMV to the end of the frontside RDL, the return loss is still maintained below -15dB indicating good impedance matching at the RDL to TMV transition. As shown in Fig. 6(b), an insertion loss of less than -1dB is achieved for both RDL and RDL with TMV from DC to 50GHz. At 28GHz, the 2mm RDL has a differential insertion loss of -0.59dB which is equivalent to about -0.3dB/mm loss at 28GHz. The RDL with TMV has a differential insertion loss of -0.65dB at 28GHz indicating an increase of 0.06dB loss by the vertical TMV.

Fig. 7 compares the S-parameter performances of three GSSG TMV vertical interconnects with different TMV pitch from DC to 50GHz. Solid lines are the measured results while dashed lines are the simulated results. GSSG TMV with a pitch of 300µm has a better impedance matching to 100Ω as can be seen in the red lines in Fig. 7(a) which has a differential return loss better than -10dB from DC to 50GHz comparing to GSSG TMV interconnects with a pitch of 350 or 400µm. For the differential insertion loss as shown in Fig. 7(b), similar insertion loss can be observed for three TMV interconnects at low frequencies since all three interconnects have the same RDL and transition lengths. As frequency increases, the vertical interconnects with larger TMV pitch have higher insertion loss due to the larger series inductance associated with the vertical TMVs as shown of the extracted TMV inductance from the

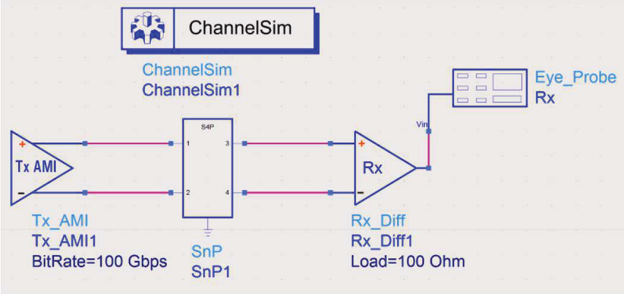

Fig. 9 Channel simulator schematic in ADS to generate 100Gbps PAM4 eye diagrams from the measured 4-port S-parameters.

simulation model in Fig. 8. At 28GHz, GSSG TMV interconnects have a differential loss of -0.14dB, -0.35dB, and -0.21dB for TMV pitch of 300, 350, and 400µm, respectively. The blue solid line in Fig. 7(b) shows an insertion loss drop at around 35GHz which could be a measurement error.

The GSSG RDLs, RDL with vertical interconnects TMV and GSSG TMV vertical interconnects are for the routing and fanout of the RF signals from EIC of the OE for 100Gbps PAM4 signals. Fig. 10 shows the PAM4 eye diagrams of the RDL, RDL with TMV, and TMV interconnect with 300µm pitch. The eye diagrams were obtained by importing the measured 4-port S-parameters into the ADS channel simulator as shown in the schematic in Fig. 9. Clear eye openings can be observed for all three measured structures. Comparing Fig. 10 (a) and (b), after adding a TMV vertical interconnect at the end of the 2mm RDL, the eye width maintains almost the same and the eye height drops by 25mV or 11%, taking the middle eye as an example. The GSSG TMV vertical interconnect with a TMV pitch of 300µm has an average eye height and width of around 260mV and 11.2ps.

Conclusions

This paper presents the measured S-parameters of the vertical interconnects TMV in GSSG configuration from DC to 50GHz. The measurements were done on a double-side prober by directly probing from the frontside and backside of the wafer. A 2mm frontside GSSG RDL with a TMV interconnect was measured to have a differential S21 of -0.65dB at 28GHz. Three TMV GSSG vertical interconnects with different TMV pitch of 300, 350, and 400µm were studied and measured to have a differential S21 of -0.14dB, -0.35dB, and -0.21dB, respectively. The 100Gbps PAM4 eye diagrams of the interconnects were also obtained by importing the measured 4-port S-parameters into the ADS channel simulator. Clear eye openings can be observed for RDL, RDL with TMV, and TMV vertical interconnects.

Acknowledgements

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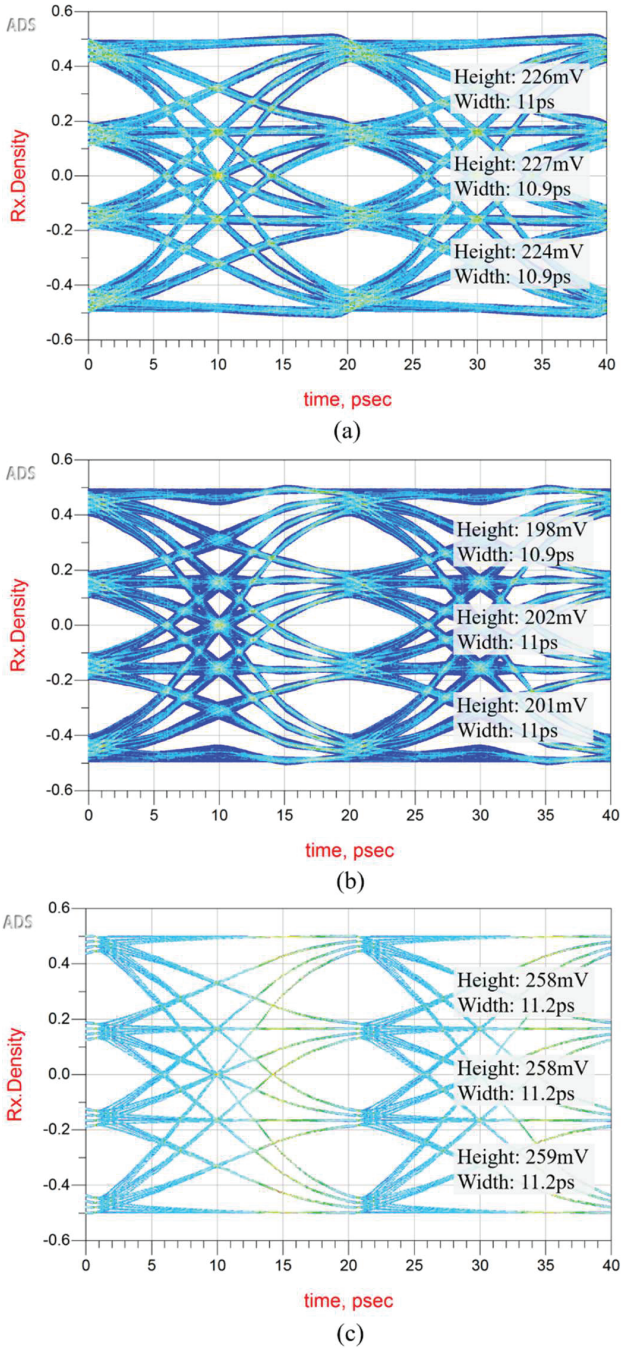

Fig. 10 100Gbps PAM4 eye diagrams generated from ADS channel simulator with measured S-parameters of (a) 2mm frontside RDL, (b) 2mm frontside RDL with TMV interconnects, (c) GSSG TMV interconnects with a TMV pitch of 300µm.

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