Development of Metallization Process for Fine Pitch TSV

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Abstract

Defect-free TSV fabrication process for Cu filling of 1.0µm and 1.5µm diameters with an aspect ratio of 7 and 6 is studied. To improve barrier/seed layer step coverage, TSV profile with scallop free with slight taper was developed, and an electroplating process was for solid TSV Cu filling. Defect-free TSV filling can be achieved for TSV with 1.0µm and 1.5µm diameters.

Introduction

Decreasing the size of TSV to enable high-density interconnection [1] is becoming critical for 3D stacking applications. However, reducing the TSV critical dimension poses immense fabrication challenges to get solid Cu-filled TSV. TSV scaling needs the optimization of liner oxide, the barrier layer and seed layer thicknesses. Liner oxide thicknesses are critical with TSV scaling; too thin is insufficient to ensure electrical insulation and thicker liner oxide lead to a narrow TSV opening, minimizing the plating process windows. Optimum selection of barrier layer and seed layer thicknesses is vital to providing better seeding efficiency during TSV Cu fill. Thin seed layer will cause electrical disconnection during TSV plating and result in no seeding and Cu growth, whereas too thick seed layer will cause PVD overhang in pinch-off defect with a void in TSV after electroplating.

This study demonstrates a defect-free TSV fabrication process for Cu filling of 1.0µm and 1.5µm diameters with an aspect ratio of 7 and 6, respectively. Liner oxide, the barrier layer and seed layer thickness were optimized to improve step coverage of the seed layer. But the increase of seed layer thickness for continuous electrical connection leads to PVD overhang at TSV opening and causes early TSV closure during the electroplating process; this defect is known as a pinch-off. TSV profile with scallop free with a slight taper was developed, and electroplating process was optimized to achieve defect-free Cu filling of fine pitch TSV.

TSV fabrication

Silicon oxide is deposited on a 12inch silicon wafer as a hard mask for Si etch. Since the TSV critical dimension is small, a tri-layer photoresist and SOC are used for fine-pitch TSV patterning, consisting of SiARC, photoresist, and TARC. SoC layer is coated as a hard mask layer for silicon oxide patterning. After SoC etch and silicon oxide etch, and remaining tri-layer mask is stripped using O2 plasma. TSV was then etched using oxide HM anisotropically. The barrier layer and seed layer are deposited prior to TSV Cu filling. The electroplating process is carried out using sulfuric acid-based Cu electrolyte with three additives. Constant current and the stepwise direct current applied for the bottom-up Cu filling.

Results and Discussions

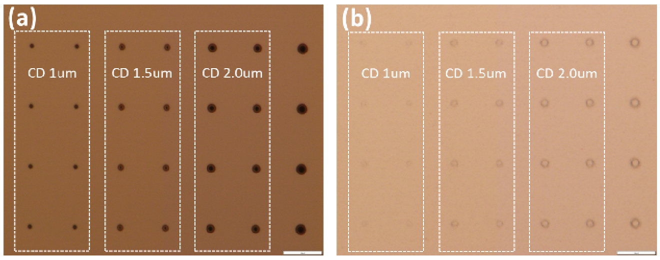

Fig. 1. Microscope images of TSV (a) after barrier/seed layer deposition and (b) after electroplating.

Fig. 1(a-b) are microscope images showing TSV Cu filling behavior before electroplating and after electroplating. Various sizes of TSVs in Fig 1(a) are filled with Cu forming Cu mounds that are due to the accumulated accelerator in TSV (Fig. 1(b)). The microscope is a commonly used method for wafer inspection, but it is hard to detect the defect in TSV because the surface morphology of TSV with and without void defect does not show a significant difference. Due to the small size of TSV, X-ray inspection could not provide a better resolution to TSV defects. Therefore, a cross-sectional FIB analysis was used to inspect the TSV Cu filling defect.

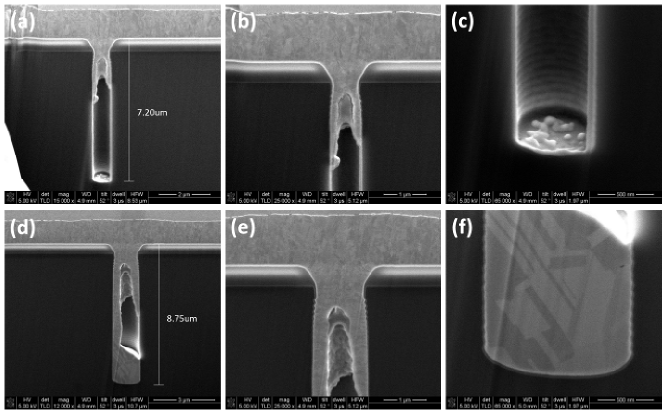

Fig. 2. Cross-sectional FIB/SEM images of (a-c) TSV with 1.0 diameter and (d-f) TSV with 1.5µm diameter after electroplating.

In Fig. 2(a-c), Cu deposit is not grown on the TSV sidewall and TSV bottom for TSV with 1.0µm diameter. The electroplating process needs a conductive layer for metal to be deposited on it, which indicates the Cu seed layer is not deposited on the TSV sidewall and TSV bottom, and there is an electrical disconnection between the TSV top and TSV bottom. For TSV with 1.0μm diameter, the Cu seed layer can reach only 2.6μm from the TSV top. In Fig 2(d-f), TSV with 1.5μm diameter demonstrates bottom-up Cu filling, but discontinuous Cu deposit on TSV sidewall can be seen with large void defect, which could be caused by discontinuous seed layer on TSV sidewall. For TSV with 1.5μm diameter, Cu seed layer on the TSV sidewall has a discontinuous deposit between 4.5μm to 7.0μm from the TSV top. To improve the step coverage of the seed layer, an increase in seed layer thickness is required.

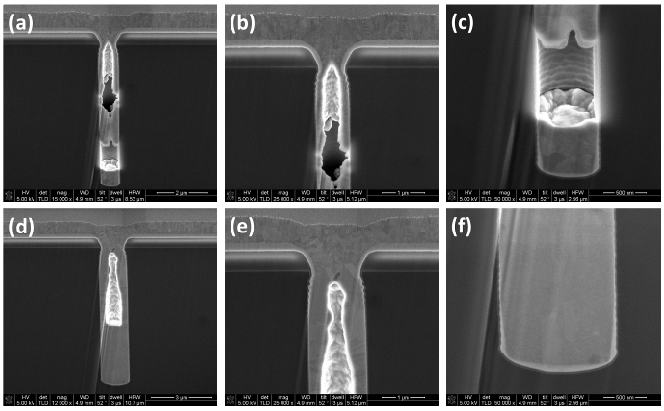

Fig. 3. Cross-sectional FIB/SEM images of (a-c) 1μm CD TSV and (d-f) 1.5μmCD TSV after electroplating.

Compared to Fig 2(a-c), an increase of seed layer thickness improves the step coverage of the seed layer achieving bottom-up Cu filling for TSV with 1.0μm diameter (Fig. 3(a-c)). For TSV with 1.0μm diameter, the Cu seed layer coverage depth increases from 2.6μm to the TSV bottom. But Cu deposit on TSV sidewall still has a discontinuous area between 3.5μm to 6.8μm from TSV top, revealing a discontinuous seed layer on this area. TSV with a 1.5μm diameter shows bottom-up Cu filling and continuous electroplating on the TSV sidewall (Fig. 3(d-f)). It was reported that a thinner Cu seed layer could make a discontinuous seed layer on a sidewall resulting in a defect in metal interconnection after the electroplating process. On the other hand, a thinner Cu seed layer provides a wider process window for the electroplating process because of the bigger top opening of the pattern, while a thicker Cu seed layer can cause early pinch-off defect [2]. And during electroplating, the current density is concentrated at the TSV top resulting in faster electroplating on TSV top compared to TSV bottom. It causes early TSV closure with seam void defect in TSV [3]. Void defect in TSV with 1.5μm diameter is due to increased seed layer thickness and current concentration at TSV top. The electroplating process is modified for solid Cu filling in TSV and applied to TSV with a thicker seed layer.

To evaluate the optimum thickness of the seed layer and check seed layer continuity, cross-sectional FIB/SEM inspection and HF etching test was carried out after barrier/seed layer deposition.

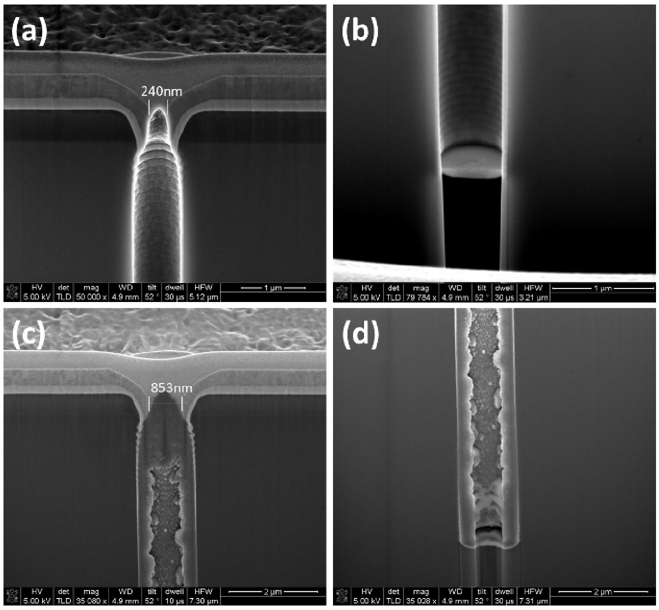

Fig. 4. Cross-sectional FIB/SEM images of (a-b) 1um CD TSV and (c-d) 1.5μm CD TSV after barrier/seed layer deposition.

As shown in Fig. 4(a), TSV with 1.0μm diameter has 240nm TSV opening. To avoid pinch-off defect, while Cu deposit fills 7μm depth TSV from TSV bottom, TSV sidewall needs to be grown only 120nm from each side. TSV with 1.5μm diameter has a relatively wider TSV opening than TSV with 1.0μm diameter (Fig. 4(c)).

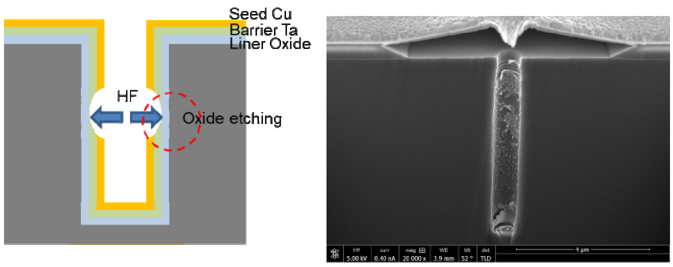

Fig. 5. Cross-sectional FIB/SEM images after HF etching test.

To reveal discontinuity in the barrier/seed layer, a diluted HF test was carried out. When a discontinuous barrier/seed layer is present, diluted HF attacks the Si oxide liner layer, which can be seen by cross-sectional SEM inspection [4].

This study dipped 3cm x 3cm wafer sample in 2% HF solution for several minutes. For TSV with continuous barrier/seed layer, HF solution will not contact with underlying Si oxide layer, while for TSV with discontinuous barrier/seed layer, HF solution will attack underlying Si oxide layer. In Fig. 5, it can be seen that the Si oxide layer in TSV with 1.0μm diameter is etched away by HF solution, and the barrier/seed layer is peeled off. The depth of the remaining barrier/seed layer on the TSV bottom is around 6.5μm from the TSV top, similar to Fig. 3(a).

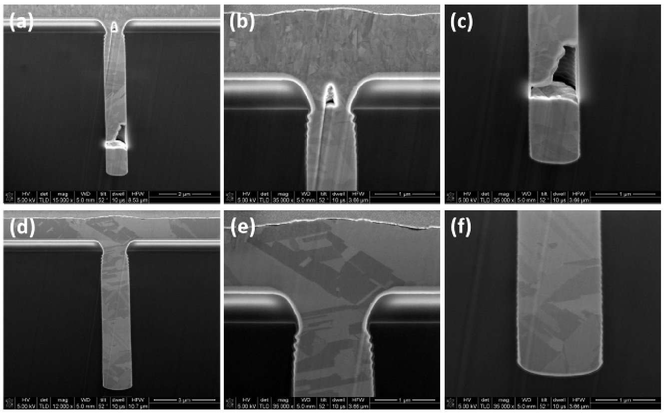

Fig. 6. Cross-sectional FIB/SEM images of (a-c) 1µm CD TSV and (d-f) 1.5µmCD TSV after electroplating.

Cu seed layer thickness is further increased to improve the step coverage of the seed layer on the TSV sidewall. The electroplating process is modified, lowering current density for solid TSV Cu filling. But TSV with 1.0µm diameter still shows discontinuous Cu deposit on TSV sidewall (Fig. 6(a-c)) while solid Cu filling can be achieved for TSV with 1.5µm diameter (Fig. 6(d-f)).

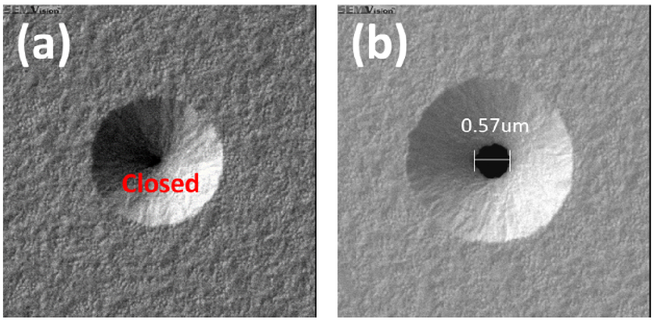

Fig. 7. SEM images of (a) 1µm CD TSV and (b) 1.5µmCD TSV after electroplating.

Further increase of Cu seed layer thickness from Fig. 6 caused the closure of TSV opening for TSV with 1.0µm diameter after barrier/seed layer deposition (Fig. 7). Due to TSV opening closure, electroplating chemicals cannot travel into TSV, and it cannot fill TSV by an electroplating process. Consequently, even though barrier/seed layer thickness increased until the TSV opening is closed, continuous deposit along the TSV sidewall cannot be achieved for TSV with a 1.0µm diameter.

To achieve continuous barrier/seed layer coverage in TSV without TSV opening closure, the TSV etching process is modified to get a smooth scallop and slight taper profile.

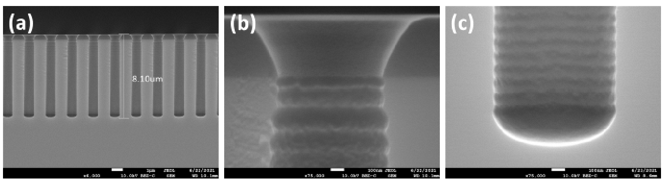

Fig. 8. Cross-sectional SEM images of 1µm CD TSV using baseline TSV etching recipe

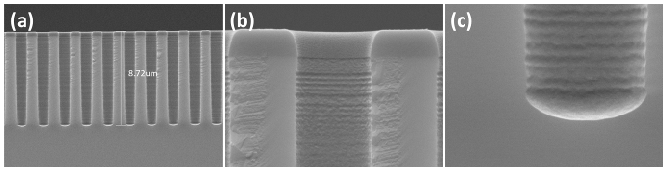

Fig. 9. Cross-sectional SEM images of 1µm CD TSV using TSV etching recipe with scallop free with a slight taper.

Fig. 8 shows the TSV profile using the baseline etching process. TSV has an overhang at TSV top with rough scallop deeper than 40nm, which could cause narrow TSV opening after barrier/seed layer deposition and barrier/seed layer discontinuity along TSV sidewall. After etching process modification, a TSV profile with scallop free with the slight taper is achieved (Fig. 9). Instead of a TSV overhang, a tapered TSV top can be seen with a smooth TSV scallop less than 30nm, which benefits the subsequent electroplating process.

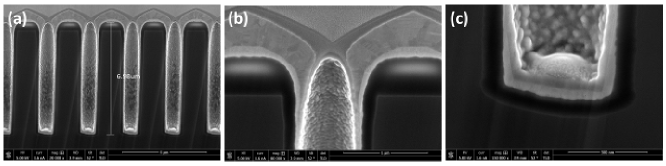

Fig. 10. Cross-sectional FIB/SEM images of 1µm CD TSV after barrier/seed layer deposition.

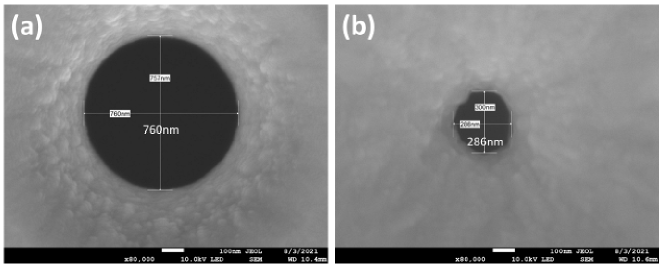

Fig. 11. SEM images of 1µm CD TSV after (a) Ta barrier layer deposition and (b) Cu seed layer deposition.

In Fig. 10, after barrier/seed layer deposition, the TSV overhang is not significant. This is because TSV etching process development is carried out using 5cm x 5cm coupon sample, while the result in Fig.10 is from a wafer-level process. TSV depth in Fig. 10 is 6.98µm, which is shallower than that in Fig. 9 with 8.72µm.

The diameter of TSV top opening for TSV with 1µm diameter is around 760nm after barrier layer deposition (Fig. 11(a)), and after seed layer deposition, top opening diameter is decreased to around 300nm (Fig. 11(b)). To achieve solid TSV Cu filling, while Cu deposit fills 7µm depth TSV from TSV bottom, TSV sidewall needs to be grown 150nm from each side.

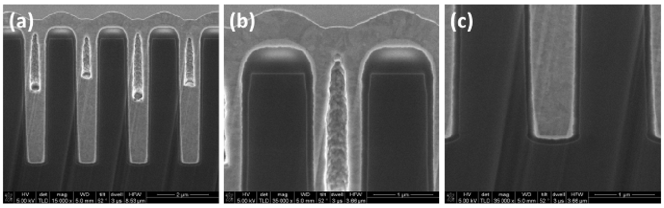

Fig. 12. Cross-sectional FIB/SEM images of 1µm CD TSV with a void defect after electroplating.

Fig. 12 shows TSV Cu filling after constant current electroplating. TSV with 1.0µm diameter can achieve bottom-up Cu filling and continuous electroplating along the TSV sidewall even though pinch-off defect occurs. Due to small TSV opening and current concentration at TSV top, Cu deposition at TSV top makes early closure of TSV opening before Cu growth from TSV bottom completes TSV filling resulting in TSV pinch-off defect.

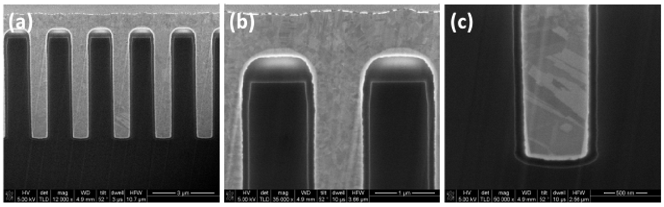

Fig. 13. Cross-sectional FIB/SEM images of defect-free 1µm CD TSV after electroplating

To achieve solid-filled TSV, the electroplating process was optimized by applying stepwise direct current. As shown in Fig. 13, defect-free TSV filling can be achieved for TSV with 1.0µm diameter. Cu overburden on the wafer surface is 0.81µm, and the electroplating process time for solid Cu filling is 30mins. Further study for Cu filling of higher aspect ratio and finer pitch TSV will be carried out.

Conclusions

This study demonstrates a defect-free TSV fabrication process for Cu filling of 1.0µm and 1.5µm diameter with an aspect ratio of 7 and 6, respectively. With baseline etching/electroplating process, continuous deposit along TSV sidewall can not be achieved for TSV with 1.0µm diameter TSV while TSV with 1.5µm diameter shows solid-filled Cu filling. To improve the step coverage of the barrier/seed layer, the TSV profile with scallop free with a slight taper was developed, and then subsequently, the electroplating process was optimized to achieve solid TSV Cu filling. Defect-free TSV filling can be achieved for TSV with 1.0µm diameter and 1.5µm diameter. Cu overburden on the wafer surface is 0.81µm, and the electroplating process time for solid Cu filling is 30mins.

References

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