Process and Reliability of Large Fan-Out Wafer Level Package based Package-on-Package

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Abstract:

This paper presents, the development of large multi-chip fan-out wafer level package (FOWLP) based Package-on-Package (PoP) using mold-First FOLWP integration flow for mobile applications. As part of this development, conventional mold-First FOWLP wafer reconstruction process has been optimized and selected key materials to overcome the challenges such as die shift, die protrusion, warpage. Fine pitch multi-layer RDL of LW/LS of 5µm/5µm fabrication, through mold via (TMV) formation, thin wafer handling for backside RDL and PoP assembly processes were also optimized. TMV process using laser drilling and sidewall plated Cu with polymer filling has been demonstrated. Using these optimized processes multi-chip FOWLP of 15 mm x 15 mm with double side RDL and high I/O count ~1360 I/Os at 400µm pitch was successfully demonstrated. Assembly process flow was optimized for PoP assembly on test boards, and build the PoP samples for reliability testing. FOWLP PoP samples were passed component level tests like MST L1, MST L3, HAST, MST L1+TC and board level tests 500 TCOB cycles and 30 drops of board level drop test. Failure analysis was carried out using CSAM, cross-sectioning and SEM. Reliability tests and failure analysis results will be presented.

Key Words: Fan-Out WLP, Package-on-Package, Fine pitch RDL, Multi-Chip Package, Through Mold Interconnections

I. Introduction

Initially, Fan-Out Wafer Level Packaging (FOWLP) was introduced to overcome the limitation of chip area in Fan-in wafer level chip scale packaging (WLCSP) technology as it can accommodate more I/Os on additional fan-out area around active device [1-2]. FOWLP technology adoption is drastically increased in the recent past due to its performance, form factor and cost. However, this technology was more matured only for limited to single chip packages such as baseband, RF and PMIC, which are used in mobiles applications. Recently, many development activities are in progress to expand the FOWLP technology for other mobile applications and new multi-chip System-in-Package (SiP) for IoT, 5G and automotive applications. Multi-chip SiP can be achieved using FOWLP in formats (i) integrate heterogeneous devices placed laterally side-by-side using RDL interconnections [3] (ii) integrate the multi-chips in Package-on-Package format using FOWLP with vertical (TMVs) interconnections and double side RDL [4]. Die shift, die protrusion, wafer warpage, RDL scaling and reliability of large FOWLP are the main challenges for this conventional FOWLP technology to adopt for complex multi-chip SiPs [5]. Adaptive patterning technology was introduced as advanced litho technique to address die shift issues of laterally placed multi-chip integrations [6]. This technique can address die shift problem with some trade-offs such as longer processing times, but still wafer warpage, RDL scaling and package reliability of large package need to be addressed. FOWLP PoP based 3D SiPs were studied using various vertical interconnection options such as embedded through silicon via (TSV) chips [7], embedded Z line (EZL) interconnection technology [8], PCB bar with plated through holes (PTH) [9]etc. All these reported methods required to fabricate vertical interconnections in separate chip or PCB and embed them adjacent to active device chips during wafer reconstruction process, which leads to die shift related challenges and can be expensive particularly TSV chip fabrication. Laser drilled vertical through mold via (TMV) interconnection is another widely studied technology for vertical interconnection in PoP applications. Laser drilled TMV formation also has its own challenges such as blind via formation to stop front side RDL Cu pad without damaging Cu RDL metal, front-to-back side alignment after molding to drill the via, seed layer deposition on rough side walls of TMVs, Cu plating etc.

This paper presents the mold 1st integration flow, and optimized processes and selection of materials to achieve large multi-chip FOWLP with double side RDL for PoP. Selection of the molding tape and pick & place (P&P) process parameters is critical to minimize the die protrusion. Different molding tapes with different P&P process parameters have been evaluated to selected mold tape and P&P process parameters to achieve die protrusion less than 5µm. Wafer reconstruction process with die-shift compensation method has been established to achieve die shift less than 10µm. Multi-layer RDL fabrication process has been optimized on reconstructed wafer using polymer dielectrics which can be cured at less than 200 degC and Cu RDL plating processes. Thin wafer handling using carrier wafer with laser release layer and temporary adhesive has been optimized and used for the TMV process and backside RDL fabrication. Laser drilling process and seed layer deposition on rough sidewall were optimized, and polymer filling of side wall plated TMVs processes was optimized for PoP application. Board level PoP assembly process was optimized for large FOWLP packages and PoP assembly on test board. These developed packages were subjected to component level reliability tests such as MST L1&L3, HAST and TC, as well as board level reliability tests such as drop test and TCoB. Large FOWLP based PoP samples passed component level MSL, HAST and MSL+TC reliability tests. It also passed board level drop test up to 30 drops without underfill and 500 TC cycles. Failure analysis has been carried out on the failed samples to understand the failure mechanism. The complete details of process development for FOWLP with double side RDL and TMVs, material evaluations, assembly process for large mold 1st FOWLP with double side RDL, reliability & failure analysis results will be presented in the following sections.

II. Test Vehicle Design

To demonstrate FOWLP PoP, a large multi-chip FOWLP of 15mm x 15mm has been designed with two chips placed side-by-side as bottom package. These two chips were integrated using 2 layer fine pitch RDLs of LW/LS of 5µm/5µm and 10µm/10µm respectively and package I/Os of ~1360 at bump pitch of 400µm. Two daisy chain test chips of 9.0mm x 8.0mm and 3.0mm x 2.0mm are designed with square bond pad size/pad opening size/pitches of 70/65/125µm and 40/35/60µm respectively. Daisy chain structures were designed to monitor the process integrity during fabrication such as multi-layer RDL connectivity, TMVs connectivity and package level reliability testing purpose. Test boards for TCoB and drop testing has been designed as per FOWLP daisy chain structures to accommodate the board level monitoring to check the assembly quality and board level connectivity during reliability tests. Test boards for TCoB and drop testing were fabricated using 4 layers FR4 of 1.5mm thickness and 8 layers FR5/TU 768 of 1.0mm thickness respectively. Chips layout in large multi-chip FOWLP package is shown in Figure 1 and cross sectional view of multi-chip FOWLP PoP is shown in Figure 2. Specifications of package and test chips are reported in Table 1 and Table 2 respectively. Wafer Level Chip Scale Package (WLCSP) was used as top package of PoP. WLCSP of 10 x 10 mm^2 was designed with full area array C4 bumps of 250µm at 400µm.

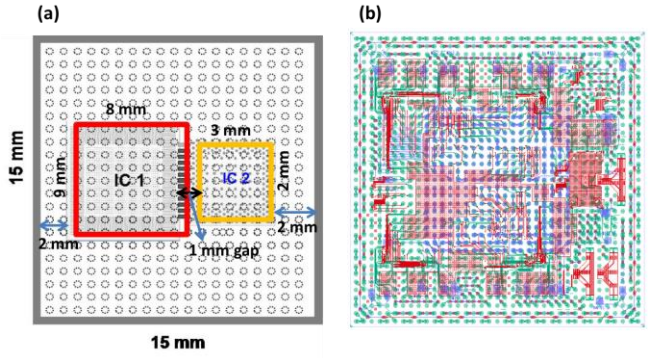

Figure 1: Multi-chip FOWLP layout (a) side-by-side chip layout in package (b) Daisy chain test structures

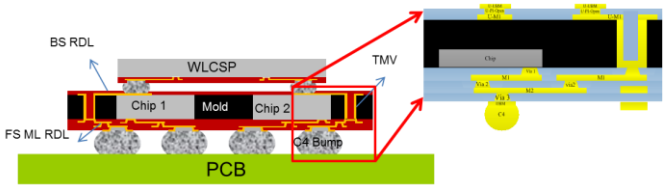

Figure 2: Cross-sectional view of multi-chip Mold-First FOWLP PoP on PCB

Table 1: Specifications of Multi-Chip FOWLP Package

Package Size (mm)	15 x 15 x 0.2
No. of Chips in Package	2
Chip sizes (mm)	IC1: 9x8 and IC2:3x2
No of RDL layer	2 layers on front side & 1 layer on back side
RDL LW/LS (µm)	5/5 and 10/10.
TMV size & pitch (µm)	100 and 300
No. of TMIs	~400 in two rows @package edge
Package level I/O	~1360
C4 bump size & pitch (µm)	250 & 400

Table 2: Specification of test chips

Description	Chip 1	Chip 2
Chip size (mm)	9 x 8	3 x 2
Min Pad pitch (µm)	125	60
Pad size (µm)	70 x 70	40 x 40
Pad Passivation opening size (µm)	65 x 65	35 x 35

III. Mold-First FOWP Integration flow for PoP application

This process integration flow is based on convention FOWLP integration flow, which starts with wafer re-construction process, includes thermal release molding tape lamination on carrier plate followed by device chips pick and place on to the molding tape in face down manner. These chips placed on carrier plates are molded with epoxy material using wafer level compression molding followed by post mold curing (PMC). After PMC, carrier plates are de-bonded from reconstructed epoxy wafers with embedded chips and peel-off the molding tape, and then these reconstructed epoxy wafers with embedded chips are ready for RDL fabrication. Secondly, multi-layer RDLs are built using photo-lithography and Cu electroplating to form the interconnection between two device chips placed side-by-side and re-route the bond pads of device chips on to the epoxy area around the device chips, and UBM formation. Thirdly, FOWLP wafer with front side RDL & UBM is bonded to the glass carrier with laser release material coating using temporary adhesive for thin wafer handling purpose during backside RDL fabrication, flowed by wafer back-grinding & polishing to thin down the reconstructed wafers to required thickness. Fourthly, TMVs are formed using laser drilling of vias through mold on to the front side RDL pads and vias filling process using plating to connect front to back side interconnections for 3D integration, followed by backside RDL & UBM formation. Finally, FOWLP wafer is de-bonded from carrier wafer and cleaned to remove laser release & temporary adhesive material for solder ball attachment on front side UBM, followed by sawing of FOWLP with double sided RDL for PoP assembly. The Mold-First FOWLP integration flow to fabricate the FOWP with double side RDL for PoP is shown in Figure 3.

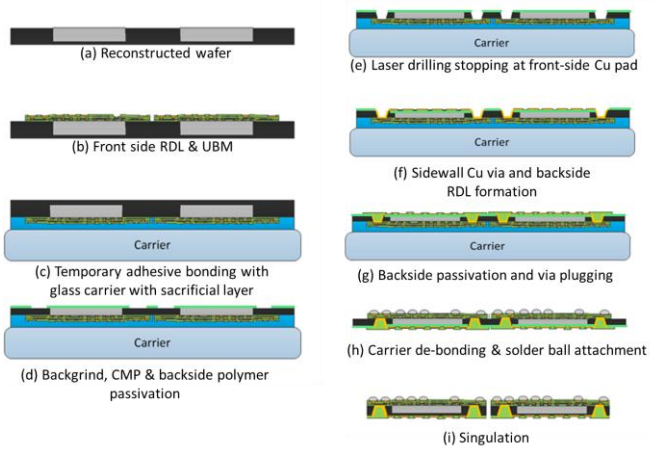

Figure 3: Process Integration flow of Mold-First FOWLP with double side RDL with laser drilled TMVs for PoP

IV. Experiments and Discussion

A. Wafer re-construction process

Die protrusion and die shift are two major challenges of wafer re-construction in mold-first FOWLP integration flow as these two issues limits the multi-chip integration and RDL scaling on re-constructed mold-first FOWLP wafers. Molding tape selection and pick and place process parameters optimization are critical to achieve minimum die protrusion. In this work, two mold compound materials with fine fillers and three molding tape materials are evaluated in terms of die protrusion, die shift & warpage. The schematic of molding tape layers is shown in Figure 4 and details of evaluated mold tape materials are shown in Table 3 & 4 respectively. Wafer level compression molding process is optimized for both mold materials. Die protrusion is measured using contact profiler and microscope to measure die shift after post mold curing of reconstructed wafers. Re-constructed wafer warpage measured as 0.8mm and 1.5-1.9mm using Mold compound material EMC A and EMC B respectively, and Mold tape with thin heat resistance layer showed less die protrusion for all bond forces. Therefore, Mold compound EMC A and mold tape C are selected for further evaluation. DOE matrix experiments are carried out using pick and place bond force between 0.1Kg to 2Kg for two chip sizes of 9mm x 8mm and 3mm x 2mm to select pick & place bond force for minimum die protrusion and die shift. Higher the bond force resulted lower die shift after molding as dies can be more secured on the mold tape when higher bond force applied during pick & Place, but it resulted higher die protrusion as dies are more sink in to the heat resistance layer of molding tape due to higher bond force. The measured die protrusion and die shift results of DOE matrix are analyzed using JMP statistical DOE tool to obtain the optimum bond force, and optimized bond force for 9mm x 8mm and 3mm x 2mm chips to achieve die protrusion <3µm and minimum die shift.

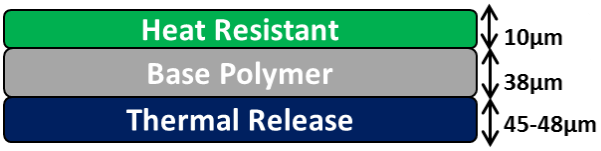

Figure 4: schematic structure of molding tape layers

Table 3: Molding tape and Mold compound materials details

Mold Tape	Release Temp (°C)	Heat Resistant Adhesive thickness (µm)
A	170	10
B	190	10
C	190	6

Table 4: Mold compound material details

EMC Candidate	Mold Type	Tg (°C)	Filler Loading (wt%)	Ave. Filler Size/ Cut Point (µm)	CTE 1/CTE2 (ppm/°C)	Modulus @RT (GPa)
EMC A	Liquid	170	87	8/25*	7/25	18
EMC B	Granular	160	89	5/20*	9/36	24

Die shift is inevitable in mold-first integration and it is mainly due to mold flow during wafer level compression molding and CTE mismatch between carrier plate and mold compound materials. Die shift leads to litho misalignment of passivation via on device chip bond pad after re-construction and it cause to open connection between side by side chips or chip and package. This die shift cannot be eliminated completely, but can reduce the magnitude by doing die shift compensation. Chips are purposefully off-set the location from original desired locations on the final reconstructed wafer, as per the pre-computed X and Y co-ordinates based on the statistical die shift data, during pick and place of chips on carrier with mold tape, so that chips will move to the desired location after molding and PMC. Set of experiments using selected mold tape, mold material and pick and place parameters for two size chips are carried out and generated the die shift data as per the original locations co-ordinates, to understand the die shift behavior and compute the off-set locations to implement the die shift compensation. The chips locations layout on FOWLP wafer for die shift measurements and die shift measurement plots are shown in Figure 5(a) & (b) respectively.

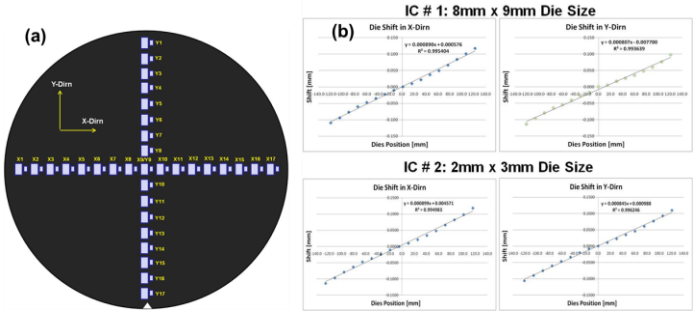

Figure 5: die shift measurements (a) chip location layout on FOWLP for die shift measurements (b) die shift measurement data before die shift compensation

Die shift measurement data shows that chips are shifted outwards from wafer center in linear manner and with consistence magnitude from the original designated location. Initially, Linear die shift compensation method is implemented, in which the compensated gap between the two adjacent chips of same size computed by deducting the die shift calculated using slope linear die shift curve (slope of linear curve x original gap between two adjacent chips of same size) from original gap between adjacent chips of same size. In this linear die shift compensation method, all new chip locations are off-set by same magnitude from their adjacent chips of same size and the results of the die shift measurement data after linear die shift compensation are reported in Figure 6. The results showed that only 90% of chips from the center of the wafer can achieve <10µm die shift using linear die shift compensation method and outer most chips are still shifted >10µm.

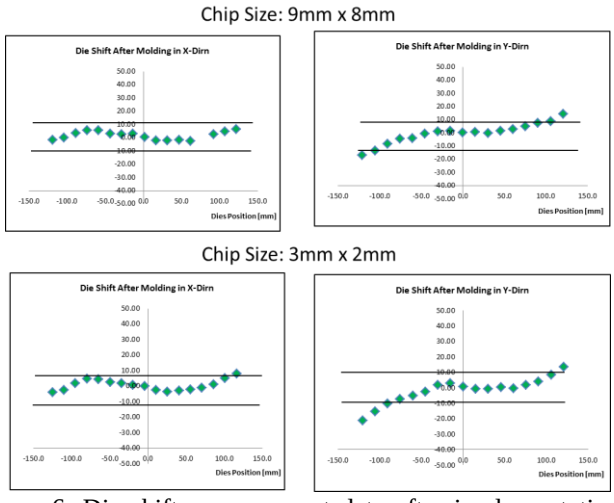

Figure 6: Die shift measurement data after implementation of linear die shift compensation

To improve the die shift further, dynamic die shift compensation method was studied, in which each chip off-sets with unique die shift magnitude by the same magnitude of that measured die shifted from the original location co-ordinates. In this dynamic die shift compensation method, all new chip locations are off-set by different magnitudes from their adjacent chips based on the die shift behavior of chip at that particular location on the 300mm reconstructed wafers. This die shift compensation method achieved overall die shift on the 300mm wafer <10µm as shown in Figure 7 and this method is adopted for the multi-chip large FOWLP test wafers fabrication.

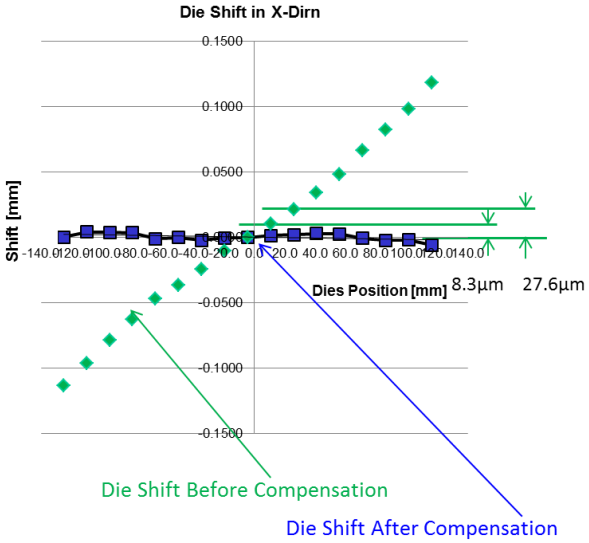

Figure 7: Die shift measurement date after implementation of dynamic die shift compensation

B. Through Mold Via Interconnections for PoP

A nano-second UV laser was used for TMVs formation in mold wafers. Laser drilling process is evaluated by forming the bling TMVs of 100µm diameter in blanket mold wafers fabricated using EMC materials with max filler size of 75µm and 20µm to study the effect of filler size on TMV sidewall profile. TMVs formed in mold wafer with fine filler size material is smooth via profile with less sidewall roughness compared to the coarse filler size material as shown in Figure 8 (a) and (b). TMV sidewall roughness in wafer with coarse filler material is attributed to the filler particle dislodgement from the surrounding epoxy resin material during laser drilling process as laser source cannot cut through the filler particle material. For PoP application, laser drilled vias need to be landed on front side metal pad without damaging Cu RDL pad. Therefore, different front side Cu RDL thicknesses 3µm, 5µm, 7µm and 9µm are evaluated to identify the minimum Cu thickness requirement to form the TMV of 100µm diameter in 200µm thick mold wafers with good connectivity. TMV laser drilling process is optimized using two step drilling method, high laser power for bulk mold material removal and then switched to lower laser power for slower ablation of mold when it reach nearer to front side RDL, to stop on front side Cu layer without any damage to Cu RDL pad and results showed that there is no significant damage to Cu RDL pad of 3µm and 9µm thicknesses as shown in Figure 8 (c) and (d). Electroless Cu seed deposition and Ti/Cu PVD seed layer deposition methods are evaluated for continuous seed layer deposition on rough TMV sidewalls. Thin Cu electroless seed can deposit continuous layer even on very rough TMV side walls, but it has weak adhesion quality as shown in Figure 8(e). In case of PVD seed layer, thick Cu layer deposition is required to form the continuous layer on smooth sidewall TMVs formed in mold wafers with fine filler material as shown in Figure 8(f), and cannot form the continuous PVD seed layer on TMV side with coarse filler materials due to the shadow effect of side wall roughness. Thick PVD seed layer deposition leads to high wafer warpage after PVD seed layer deposition. Step PVD process was optimized to achieve continuous seed deposition on TMV sidewalls with minimum wafer warpage. TMV wafers with seed layer are further electroplated to confirm the good connectivity of TMVs.

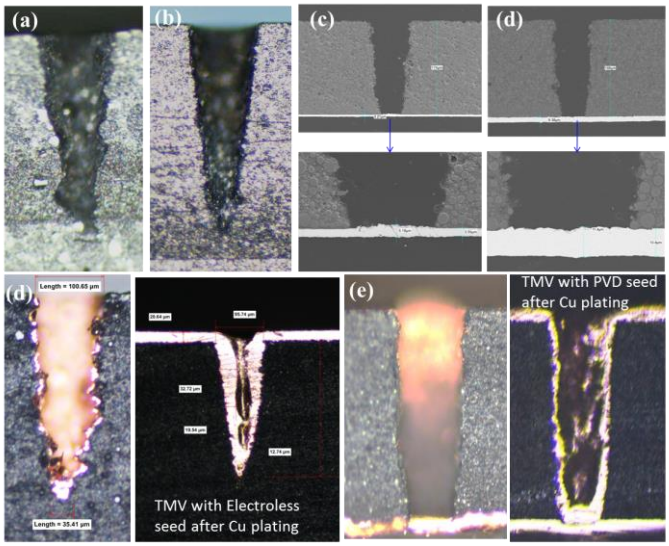

Figure 8: Cross-section of laser drilled TMVs (a) TMV profile in mold wafer with coarse filler material (b) TMV profile in mold wafer with coarse filler material (c) TMV stopped on 3µm thick front side RDL (d) TMV stopped on9 µm thick front side RDL (e) TMV with electroless Cu seed (f) TMVs with PVD seed layer deposition followed by Cu electroplated.

TMVs with partially plated Cu on the sidewalls are filled with polymer dielectric material to plug the blind TMVs for further backside RDL fabrication. Two polymer dielectric material filling methods (i) spin coat and vacuum soft bake of liquid polymer dielectric (ii) vacuum lamination of dielectric film over laser drilled TMVs are studied to achieve void free polymer plugging. Spin coating of liquid polymer dielectric material over the mold wafer with partially plated blind TMVs forms lot of voids in the TMVs and soft backing process is carried out under vacuum to remove voids from the dielectric material in TMVs. However, non-uniform filling of dielectric in TMVs over wafer and dielectric dishing of 40-100µm at the center of TMVs are observed as shown in Figure 9 (a) & (b), and this may be due to the in-sufficient dielectric material around the highly dense TMVs area to reflow into the vias during soft back and curing. Vacuum lamination of dielectric film over mold wafer with partially plated TMVs using optimized process parameters achieved very good TMV plugging with uniform thick film formation on mold wafer surface as showing Figure 9 (c) and it can be used as backside RDL passivation in the integration.

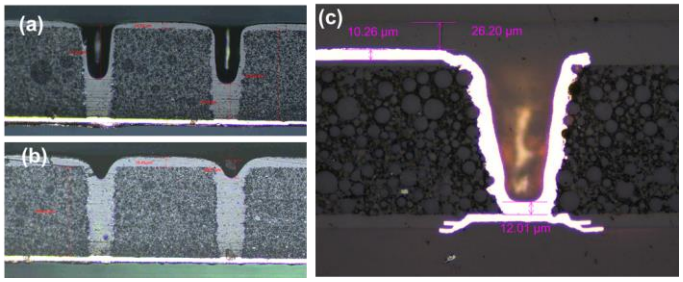

Figure 9: Cross-section of laser drilled through Mold Via with polymer plugging (a&b) polymer plugging using spin coated dielectric with vacuum baking (c) polymer plugging using vacuum lamination dielectric film

C. Fine Pitch RDL on Mold First FOWLP Wafer

Two low cure temperature dielectric materials were evaluated as inter metal dielectric layer and litho processes coating, backing, exposer, post exposer bake and developing processes were optimized to achieve 5µm via patterning in 7-8µm thick dielectric layer for fine pitch RDL processing on reconstructed wafers. Both dielectric materials were cured at 200^0C temperature for 1 hour. Die shift magnitude and bond pad size on device chip will decide the fine pitch RDL alignment on chips in reconstructed wafer as large die shift of chips with small size bond pads leads open connections due to miss-alignment of passivation opening on re-constructed chip bond pads. Therefore, litho experiments are carried out using mask with 5µm size passivation via on optimized reconstructed wafer with different bonds sizes of 10µm -70µm on test chip to define the minimum bond pads size on device chips to achieve good connectivity. The minimum bond pad size for 5µm passivation via on the reconstructed wafer with 10µm die shift should be 30µm to achieve good alignment and connectivity, good alignment of passivation via is observed even on 20µm pad size at the center of reconstructed wafer where die shift is <5µm as shown in Figure 10(a). Bond pad size of 30µm x 30µm has been used to design the daisy chain test chips for the development of large multi-chip FOWLP. Photoresist litho, plating and seed layer etching processes are optimized for fine pitch RDL of LW/LS of 5µm/5µm on reconstructed wafers and achieved good coverage over chip edges without any RDL damage as showing in Figure 10(b).

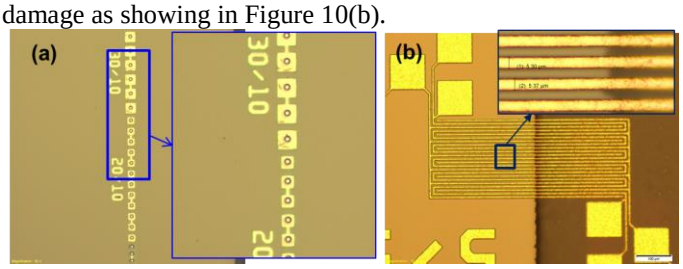

Figure 10: Optical images (a) passivation alignment with bond pads of chip on reconstructed wafer (b) fine pitch RDL of LW/LS of 5µm/5µm over embedded chip edge.

Fabricated fine pitch RDL of 5µm/5µm was characterized using meander structures and 5 point measured I-V curve of the meander structures was nearly horizontal with leakage current of less than 1pA as shown in Figure 11, and it shows no leakage between adjacent fine RDL lines and micro cracks in fine pitch RDL. Daisy chain structures were designed by connecting 50 and 100 number of vias to confirm the process uniformity and connectivity of small passivation via opening of 5µm between two metal layers. I-V characterization results of daisy chains showed linear cure with average resistance of 3.2 and 4.5 ohms respectively as showing in Figure 12 and it shows good connectivity of inter metal vias of 5µm.

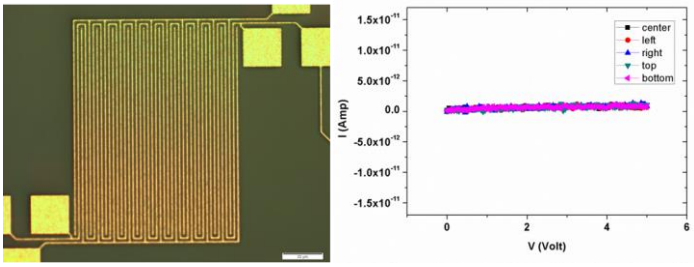

Figure 11: Meander structure with RDL LW/LS of 5µm/5µm and I-V curve of meander structure.

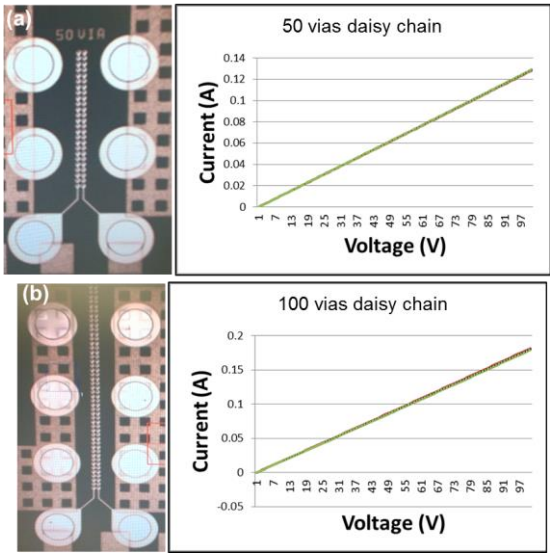

Figure 12: Daisy chain structures and I-V curve of daisy chains (a) daisy chain structure connects 50 passivation vias (b) daisy chain structure connects 100 passivation vias.

D. Process Integration of Mold-First Fan-out WLP with double side RDL and TMVs

Test vehicles fabrication for reliability testing was carried out using optimized wafer reconstruction processes and selected materials explained in the earlier sessions to arrange two daisy chain test chips side-by-side with die protrusion <3µm and die shift <10µm. Front side redistribution layers (RDLs) fabrication starts with passivation opening of 5µm vias on daisy chain test chips of reconstructed wafer, followed by formation of multi-layer fine pitch RDL layers of LW/LS of 5µm/5µm and 10µm/10µm were fabricated using optimized process parameter to integrate two test chips in single package. Cu/Ni/Au UBM of 5µm/3µm/0.1µm was formed using electroplating process for C4 bumping. Front side multi-layer RDL process results at various stages was shown in Figure 13.

Thin wafer handling is critical to thin down the FOWLP wafer with front side RDL layers to required thickness and process the back side RDL for package-on-package application. Glass carrier with sacrificial laser release layer coating was used as support wafer and bonded to front side of FOWLP wafer using temporary adhesive material as shown in Figure 14(a). FOWLP wafer was thin down to 200µm and exposed the test chips at back side, and front side and backside of FOWLP wafer after thinning was shown in Figure 14(b) & (c). Laser drilling of TMVs require alignment marks at the back side to

stop the TMV on front side metal pads as laser drilling tool do not have IR alignment feature to see through the Si chip. Therefore, dielectric layer was coated on the back grinded surface of bonded FOWLP wafer and Front to back side alignment was carried out using dual side IR alignment process as shown in Figure 14(d) to pattern the alignment marks at the backside of the FOWLP wafers. The alignment mark was not able to recognize clearly through the rough surface of the back grinded Si surface by litho tool as shown in Figure 14(e) as grinding marks adversely affect the quality of the image. This was resolved by introducing the polishing process step after back grinding to remove the grinding marks and stepper can recognize the alignment mark clearly as shown in Figure 14(f). This dielectric layer at the backside will serve two purposes (i) provide the alignment mark for laser TMV drilling alignment to the front side bond pad (ii) protect the mold surface from laser burn marks which will degrade the adhesion of subsequent RDL layers on backside of the FOWLP wafer.

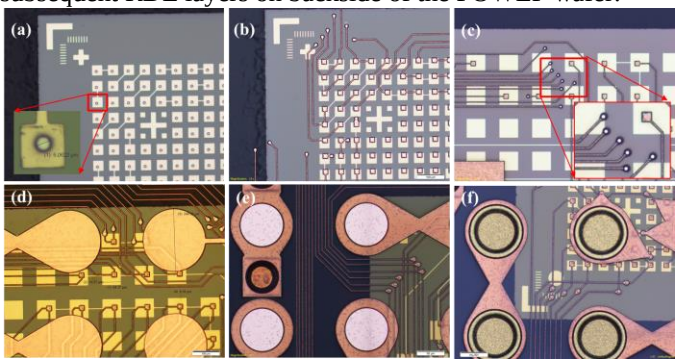

Figure 13: Mold first FOWLP front side RDL fabrication processes results (a) first passivation opening on bond pads of test chip (b) 1st RDL metal routing (c) 2nd passivation opening on 1st RDL pads (d) 2nd RDL metal routing (e) 3rd passivation opening on 2nd RDL pads (f) UBM formation for C4 bumping

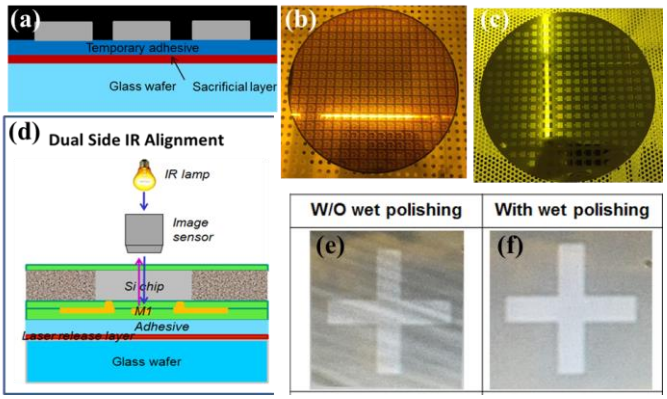

Figure 14: Thin wafer handling for back side RDL processing (a) Schematic of carrier wafer bonding (b) front side RDL through bonded glass carrier (c) FOWLP wafer back side after thinning (d) front to backside alignment procedure (e)&(f) Alignment mark reorganization on back grinded FOWLP wafer surface without & with polishing respectively

TMV vertical interconnection formation was carried out on the backside of bonded wafer using optimized laser drilling to stop on the front side Cu pad as shown in Figure 15(a), followed by Ti/Cu seed layer deposition using step PVD process. Backside RDL and TMV side wall metallization was carried out in single litho and plating process step using dry film patterning on FOWLP wafer with seed layer deposited TMVs as shown in Figure 15(b). After TMV side wall and RDL plating, dielectric film was laminated under vacuum to plug the partially plated TMVs as Shown in Figure 15 (c)& (d), followed by patterning of same dielectric layer to open RDL metal for bond pads of top package assembly as shown in Figure 15(f). After completion of backside RDL and UBM processes, glass carrier wafer was de-bonded using laser exposer followed by plasma cleaning of sacrificial layer residue. De-bonded FOWLP wafer mounted on dicing frame with dicing tape and temporary adhesive layer cleaned from the front side of the FOWLP wafer using cleaning solvent. C4 bond pads on front side is clean from residue and wafer is ready for dicing and bumping. FOWLP test samples were fabricated using two low cure temperature dielectric materials for reliability testing evaluation.

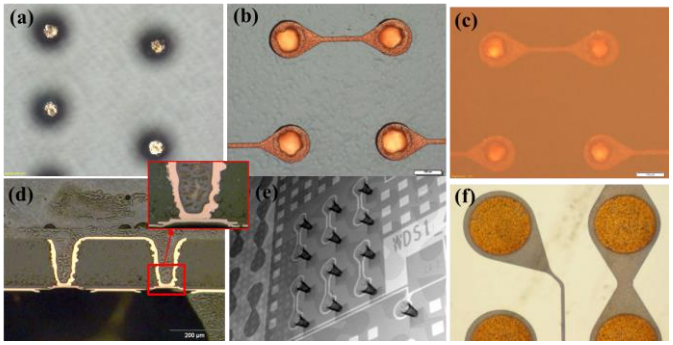

Figure 15: Backside RDL fabrication processes results (a) Laser drilled TMVs stopped on front side RDL pads (b) backside RDL and partially plated TMVs (c)-(e) polymer plugged TMVs (f) Backside RDL patterning for PoP assembly.

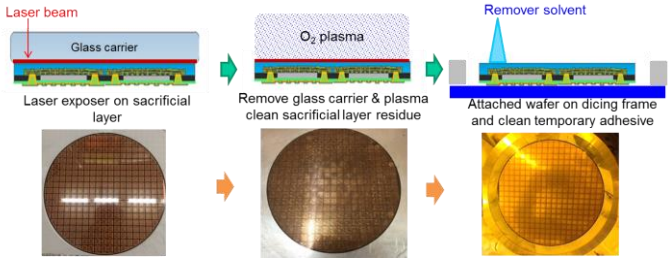

Figure 16: Glass carrier de-bonding and cleaning process flow

V. Package Assembly

Large multi-chip FOWLP of 15mm x 15mm x 0.2mm with double side RDL and TMVs observed less warpage after dicing. C4 bumping on front side UBM of 200µm size and WL CSP UBMs was carried out at package level using flux and solder ball attachment jigs. Bump reflow process was optimized to control the warpage of large FOWLP after C4 bumping. C4 bump quality on mold-first FOWLP samples fabricated using two different dielectric materials was verified using bump shear testing and results obtained met the bump shear requirement of >2.5g/mil^2 as per the JEDEC standard. The large (15 mm x 15 mm) multi-chip mold-first FOWLP package and WLCSP with bumping are shown in Figure 17. Board level assembly processes for large FOWLP with 250µm size C4 bumps at 400µm pitch and PoP assembly on TCoB and drop test boards has been optimized using tacking and reflow method. In case of PoP assembly, bottom FOWLP package first tacked on to PCB using flux and low temperature thermal compression bonding, then top WL CSP tacking on bottom FOWLP package using flux followed by reflow process to form the solder joint interconnections between bottom FOWLP and PCB, FOWLP and top WLCSP simultaneously as shown in Figure 18.

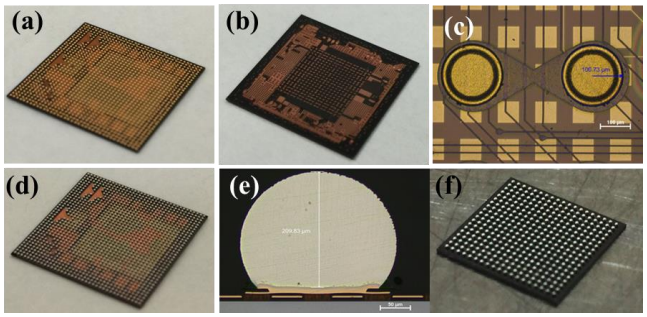

Figure 17: Mold-First FOWLP (a) Package with front side RDL (b) Package with backside RDL (c) UBM pad after de-bonding & adhesive cleaning (d) C4 bumped package (e) X-section of C4 bump on FOWLP (f) WLCSP with C4 bumping.

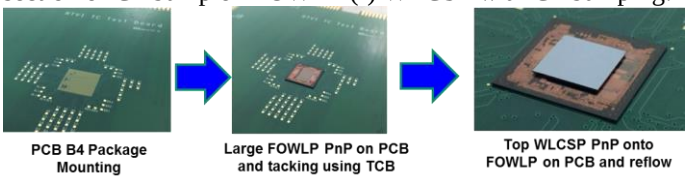

Figure 18: Assembly process flow for PoP bonding on PCB

Warpage of large FOWLP was measured at each assembly process steps and maximum package warpage observed during PoP assembly using optimized assembly flow was 56µm as shown in Figure 19. Daisy chain resistance was measured on PCB to confirm the connectivity of C4 bump interconnection at various levels and TMVs. The measured resistance valves of various daisy chains connecting C4 solder joints between FOWLP & WLCSP through TMVs, FOWLP and PCB, vertical TMVs alone, etc are consistent and repeatable. The integrity of assembled PoP was also confirmed by cross-sectioning the assembled PoP. Cross-section analysis showed good solder joint formation between two packages and FOWLP & PCB, and TMVs integrity with top & bottom RDL layers was also confirmed as shown in Figure 20.

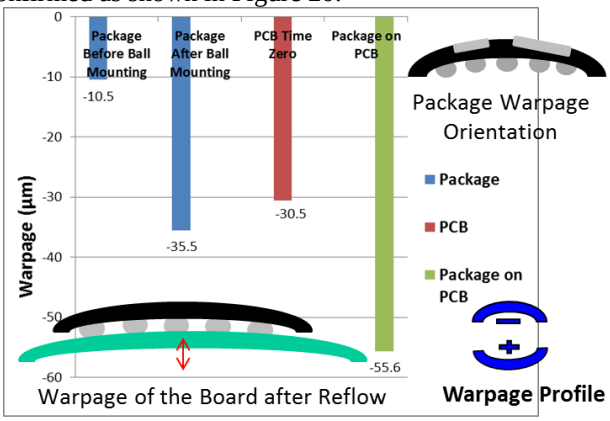

Figure 19: Warpage of mold-first FOWLP at various stages of PoP assembly

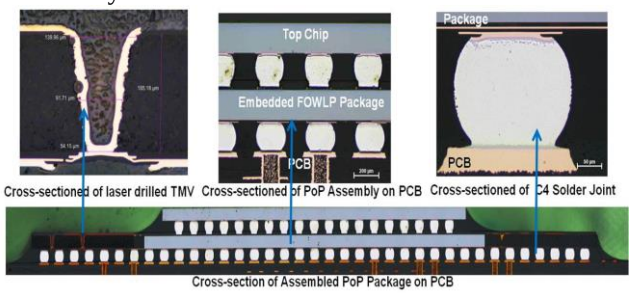

Figure 20: Cross-section of FOWLP PoP on PCB

VI. Reliability Test Results

Large multi-chip FOWLP PoP samples fabricated using two dielectric materials (material A & material B) were subjected to component level and board level reliability tests to confirm the package integrity and structural performance. Test conditions of component and board level reliability tests are shown in table 5. CSAM/Thru-scan analysis and daisy chain resistance measurements were performed before and after reliability tests to verify the package integrity. The change in daisy chain resistance by 20% and open chains are considered as ET test failure. The reliability test performance results of FOWLP PoP samples are tabulated in Table 6. FOWLP PoP samples with dielectric material A showed better performance in component level and board level reliability tests compared to the POP samples with Dielectric material B. FOWLP PoP samples with material A passed component level tests MST L1 and L3, HAST and MST L1 + TC 1000 cycles without any failure. Most of the PoP samples with dielectric material A were also passed board level drop test (without underfill) up to 30 drops and 500 TCoB cycles.

Table 5: Reliability test conditions

Test	Test condition
MST L1 (Component)	85°C/85% RH for 168hours + 3x Reflow, 260°C
MST L3 (Component)	30°C/60%RH for 192hours + 3x Reflow, 260°C
HAST (Component)	JESD22-A110A 130° C/ 85% 96 hours
Thermal Cycling (Component)	Thermal Cycling , - 55°C to +125°C, 15 min. dwell, 1000 cycles.
Drop impact (Board level)	JESD22-B111 0.5 ms half-sine with peak acceleration of 1500 G, 30 drops
TCOB (Board level)	Thermal Cycling , - 40°C to +125°C, 15 min. dwell, 1000 cycles.

Table 6: Reliability test results

Reliability test	Dielectric A (#samples failed/Total Samples)	Dielectric B (#samples failed/Total Samples)
MST L1 (Component)	0/22	4/22
MST L3 (Component)	0/22	0/22
HAST (Component)	0/15	9/15
MST L1 + TC 1000 cycles	0/21	17/21
TCoB (Board Level)	0/15 @250 cycles 2/15 @500 cycles 13/15 @ 750 cycles 15/15 @1000 cycles	15/15 @250 cycles
Board Level Drop test (30 drops)	3/22	9/22

Failed samples were analyzed using CSAM and cross-sectioning to identify the failure modes. The failure analysis of failed component reliability test samples with dielectric material B revealed that the most of the failures occurred due to dielectric layer delamination from reconstructed mold wafer surface as showing Figure 21. This may be due to the poor adhesion of dielectric material with mold surface and it can be improved by introducing the mold surface cleaning before dielectric coating. Cross-section analysis of failed TCoB samples revealed that dielectric cracks are initiated around C4 bump UBM at fan-out mold area of the FOWLP and propagated through RDL metal trace as shown in Figure 22(a). This failure mode was also confirmed on the surface of the failed FOWLP package after detaching from the PCB as shown in Figure 22(b). TCoB test results can be improved by using hybrid dielectric films, dielectric material fine via resolution as first layer for fine pitch RDL and dielectric layer with high modulus as final passivation layer below C4 bump UMB. Drop test failures are also occurred mainly due to the dielectric layer peeling from front or backside of the reconstructed mold wafer surface. Drop test performance can be improved by improving the dielectric materials adhesion on mold surface and applying underfill for C4 bumps on PCB.

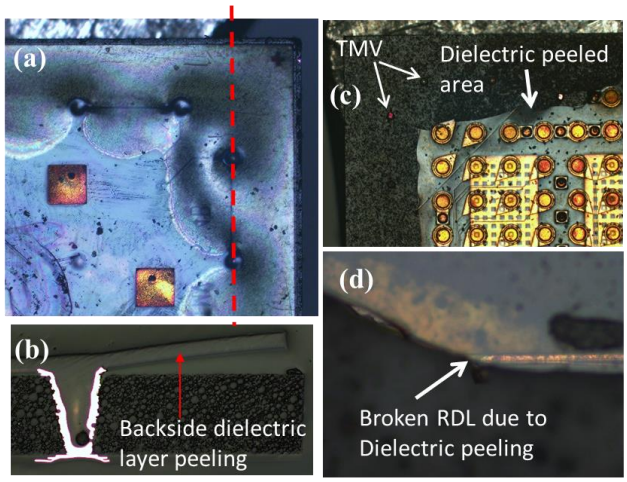

Figure 21: Images of failure modes (a & b) backside dielectric layer peeling from mold surface (c & d) front side dielectric layer peeling and RDL cracking due to dielectric peeling respectively.

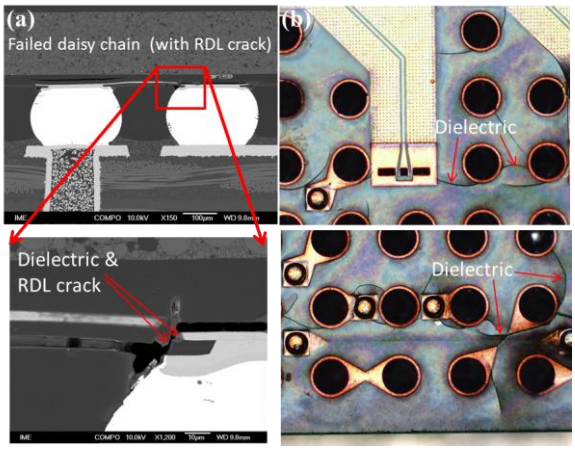

Figure 22: Failure mode images of TCoB samples (a) Cross-section of cracked Dielectric layer and RDL trace (b) top view of the failed FOWLP surface after detached from PCB.

VII. Conclusions

Mold-first FOWLP integration flow was successfully demonstrated for large multi-chip package of 15mm x 15mm with fine pitch multi-layer RDL of L/S of 5µm/5µm, double side RDL & laser drilled vertical TMVs, and package I/Os ~1360 for mobile application. Wafer re-construction processes were demonstrated to achieve die protrusion ≤3µm using optimized pick & place process and molding tape with thin thermal adhesive, and die shift ≤10µm using dynamic compensation method. Fine pitch RDL process was established using selected PRs and dielectric materials, and successfully fabricated 2 layer fine pitch RDL of 5µm/5µm on reconstructed FOWLP wafer to integrate 2 test chips. Laser drilled TMV processes was optimized to stop on the front side RDL pad and fabricated through mold vertical interconnections using optimized laser drilling, PVD seed deposition on rough TMV side walls, partial plating of TMVs along with backside RDL and polymer plugging of TMVs processes for PoP application. Thin wafer handling process was established using glass carrier wafers with laser release layer coating and temporary adhesive for TMV and backside RDL processing. Processes for carrier wafer de-bonding, cleaning of laser release material residue and adhesive material were optimized. Successfully fabricated Mold-first FOWLP wafers with double side RDL using two different dielectric materials for reliability assessment. C4 solder bumping and bonding processes were optimized for large FOWLP PoP assembly on PCB. PoP samples with dielectric material A showed better performance than the samples with dielectric material B. FOWLP PoP samples with dielectric material A passed component level reliability tests MST level 1& 3, HAST and MST L1 + TC 1000 cycles, and also passed board level tests 30 drops as per the JEDEC drop test without underfill and TCoB 500 cycles. The main failure mode observed on the component TC test and TCoB failed test samples was dielectric delamination from mold surface and dielectric crack in dielectric layer at the corner of C4 bump UBM respectively, and it can be improved by using hybrid dielectric layers to improve the TCoB further.

Acknowledgement

This work is the result of a project initiated by High Density Fan-Out Wafer Level Packaging (HD-FOWLP) Consortium. The authors greatly appreciate the members' participation in discussions and encouragement throughout the course of the project which makes this research possible. Authors would like special thanks to AMAT, Orbotech and Kingyoup Optronics teams for their support in PVD process, TMV laser drilling and laser release material coating & laser de-bonding processes respectively.

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