Reliability Assessment of 2.5D Module using Chip to Wafer Hybrid Bonding

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Abstract

Wafer to wafer hybrid bonding has been established to form fine pitch interconnections for high density I/O applications [1, 2]. However, this approach has limitation that demands same interconnects layout and same chip sizes for both wafers. In addition, yield of the bonded wafer is affected severely from the individual yield of the wafer and the location of the chip with good yield. Chip to Wafer hybrid bonding is an attractive approach to mitigate the yield issue and the different design aspect from the chip and the wafer. However, it is not an easy approach as it demands absolute cleanliness of bonding surfaces for both chip and the wafer throughout the assembly processes. This article demonstrates reliability assessment of chip to wafer bonding approach. A good yield of chip to wafer hybrid bonding was obtained and the bonding interface remained intact throughout the thermal cycling tests and moisture sensitive test.

Introduction

Chip to wafer hybrid bonding is getting more and more adopted by the industry in handling devices with ultra-fine pitch below 10 µm. Challenges such as oxide planarization, surface activation impact on surface roughness and contact angle, copper oxide's thickness, and high bonding accuracy In addition, bonder's cleanliness, compatibility of the assembly material such as dicing tape in the surface activation process, stringent Cu dishing magnitude and uniformity impact the yield of the Hybrid bonding. Dicing induced particles are encountered for mechanical blade dicing approach and need to be mitigated in the hybrid bonding process [3, 4, 5].

Successful hybrid bonding requires controlling the Cu dishing in angstrom level by Chemical Mechanical Polishing (CMP). Wafer needs to be coated with protective layer before dicing process to eliminate dicing debris sticking on the bonding surfaces Surface activation including de-ionised (DI) water rinsing to generate hydroxyl (-OH) group on the bonding surfaces, optimum Cu oxide thickness as it will be difficult to induce Cu grain growth if the oxide is too thick. Bonder bonding's accuracy should be 0.1 to 0.25 times the pad diameter to enable good Cu-Cu interfacing area, and area around the bonding process should be ISO 3 specifications to minimize particles landing between the bonding interface.

In this work, we developed CMP process to achieve Cu dishing ~4nm, Oxide roughness ~0.3nm; dicing with protective layer; surface activation, room temperature tacking process and annealing process. The wafer with bonded units passed Moisture Sensitivity Level 3 and 1000 Temperature cycling.

Information of Test Vehicle

High Temperature TEOS oxide is deposited at 350ºC on both the chip and the bottom wafer. The size of the chip is 6mm x 6mm x 0.2mm and the size of the package is 8mm x 15mm. Thickness of the bottom wafer is 0.775mm. Cu pad is 5µm at pitch of 10µm. Table 1 showed the information of the chip and bottom wafer. Figure 1 showed the schematic layout of the bonded unit.

CMP was carried out on both the chip and bottom wafer to achieved ~0.3nm oxide roughness and ~4nm Cu dishing. Figure 2 showed the Atomic-Force Microscopy (AFM) results on the surface of the chip after CMP process. Cu dishing is closely related to the annealing temperature. Lower annealing temperature for successful Cu-Cu joints formation will require lower Cu dishing as lower annealing temperature can generate limited expansion of the Cu material.

Table 1: Test Vehicle's Information

Item	Information
Chip Size	6x6x0.2mm
Package size	8x15mm
Bottom Wafer	300mm diameter with 0.775mm thickness
Pad Size and Pitch	5µm pad diameter at 10µm pitch
Passivation Type	High Temperature TEOS Oxide
No of HB Pads	352,366

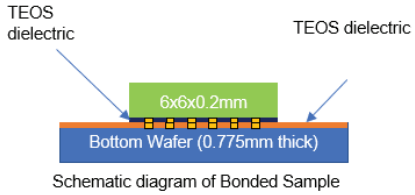


Figure 1: Schematic diagram of the bonded sample

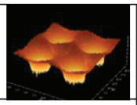
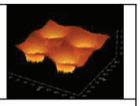
3D View		
Cu roughness Average (nm); 1x1µm	0.177	0.170
Oxide Roughness Average (nm); 2x2µm	0.161	0.170
Step height (nm)	-3.377	-3.279

Figure 2: AFM results on the chip after CMP Process

Two sets of daisy chain structures with 10k pads are monitored immediately after annealing process. Moisture Sensitivity Level (MSL) 3 with 3x reflow process and 1000 T/C. One set of daisy chains was located on top left corner and the other set located at bottom right corner of the chip as shown in Figure 3. Both sets consist of pad diameter of 5µm at pitch of 10µm.

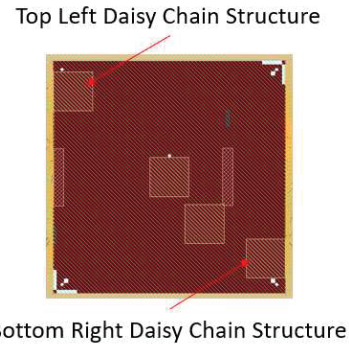


Fig 3: Daisy Chain Groups on the test vehicle

Plasma Process Optimization

10x10mm chip with blanket High Temperature TEOS passivation is treated with plasma parameters and subjected to contact angle and surface roughness measurement. Environmental plasma system is used to treat the surface before bonding. Nitrogen gas is used in the plasma process. Different plasma parameters such as flowrate, power, gap and scan speed were tested out as tabulated in Table 2.

The results of contact angle and surface roughness were input into JMP software. Target responses are low contact angle and low surface roughness. The software indicated that the response is significant, and gap is the most significant factor as shown in Figure 4 & 5.

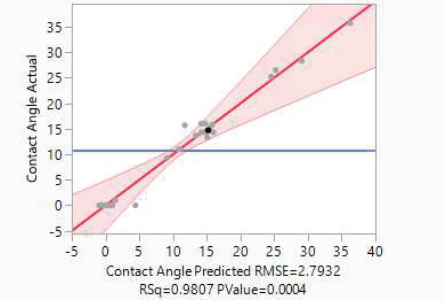


Figure 4: Response Surface Analysis

Table 2: Plasma Parameters

Test ID	N2 (slpm)	Power (W)	Gap (mm)	Speed (mm/s)
1	0.3	80	1	1
2	0.3	180	1	1
3	0.15	130	1	2.5
4	0.3	80	4	4
5	0.15	130	2.5	2.5
6	0.3	180	4	1
7	0.3	130	2.5	2.5
8	0.15	130	2.5	2.5
9	0.3	180	4	4
10	0.3	80	4	1
11	0.15	130	2.5	2.5
12	0.15	130	2.5	4
13	0.15	130	4	2.5
14	0.15	130	2.5	1
15	0.3	80	1	4
16	0.15	80	2.5	2.5
17	0.15	130	2.5	2.5
18	0.15	180	2.5	2.5
19	0.3	180	1	4

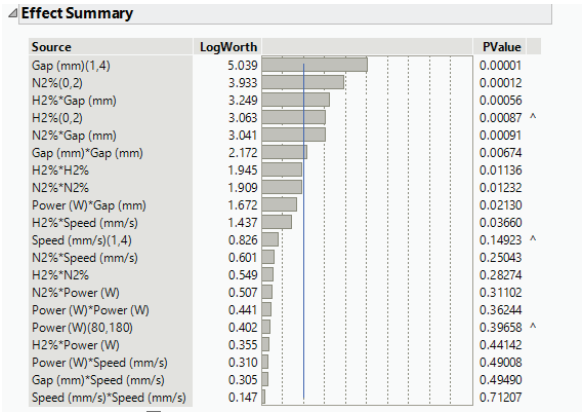


Figure 5: Effect of various factors indicated Gap is the most significant factor

The surface response curve indicated the optimum plasma parameters for low contact angle and roughness are 0.15slpm, 80W, 4mm gap & 4mm/sec scanning speed as shown in Figure 6. Prefer to have low contact angle and low surface roughness to enable good Cu-Cu diffusion bond.

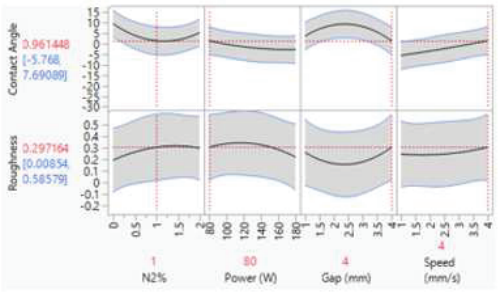


Figure 6: Surface Curve Response

Evaluation of chip to wafer bonding with different Cu dishing and different annealing parameters

Chip & bottom wafer with different Cu dishing are subjected to different annealing parameters to see any impact to the yield related to daisy chain formation. Chip and bottom wafer were CMP to produce ~4nm Cu dishing and ~8nm Cu dishing as shown in Figure 7.

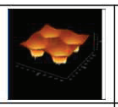
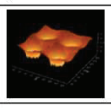
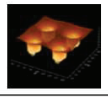
	Cu Dishing ~4nm		Cu Dishing ~8nm	
3D View				
Cu roughness Average (nm); 1x1µm	0.177	0.233	0.176	0.125
Oxide Roughness Average (nm); 2x2µm	0.161	0.170	0.104	0.097
Step height (nm)	-3.377	-3.279	-8.137	-7.799

Figure 7: Wafer with 4nm and 8nm Cu dishing

The chips with different Cu dishing are tacked on the bottom wafer with similar Cu dishing. The tacking parameters are 20N for 3sec at room temperature. The wafer with tacked chips were subjected to annealing temperature of 350ºC or 400ºC and either 3hr or 5hr annealing duration. The wafer with the bonded chips were subjected to daisy chain (with 10k pads) measurement after the annealing process.

Results on the evaluations

Table 3 tabulated the daisy chain yield for the wafers prepared with different Cu dishing and annealing parameters. Yield is relatively the same regardless of Cu dishing and annealing parameters. The results indicated that good daisy chain connection can be achieved with lower annealing temperature of 350ºC and shorter duration of 3hr with Cu dishing range from 4 to 8nm. Figure 8 showed the yield map comparing with 4nm and 8nm Cu dishing.

Table 3: 10k pads Daisy chain Results

No	CMP	Annealing Parameters	Yield % (10k pads)
1	~ 4nm Cu dishing; ~ 0.3nm oxide roughness	150ºC/1hr & 400ºC for 5hr	~ 90%
2	~ 4nm Cu dishing; ~ 0.3nm oxide roughness	150ºC/1hr & 400ºC for 3hr	~ 98%
3	~ 4nm Cu dishing; ~ 0.3nm oxide roughness	150ºC/1hr & 350ºC for 5hr	~ 95%
4	~ 4nm Cu dishing; ~ 0.3nm oxide roughness	150ºC/1hr & 350ºC for 3hr	~ 97%
5	~ 8nm Cu dishing; ~ 0.3nm oxide roughness	150ºC/1hr & 400ºC for 5hr	~ 97%

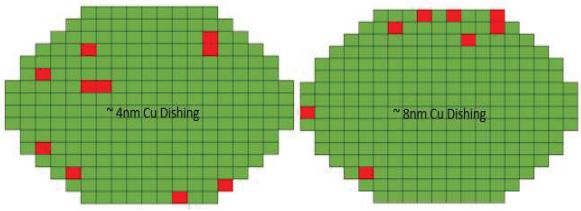


Figure 8: Daisy Yield Map for wafer with 4nm and 8nm Cu dishing (red indicate failed/opened unit)

X-sectioning was done on bonded unit that had daisy chain reading and another unit that had no daisy chain reading. Voids are observed between the Cu-Cu interface but no gross gap between the Cu-Cu interface for both passed and failed unit as shown in Figure 9.

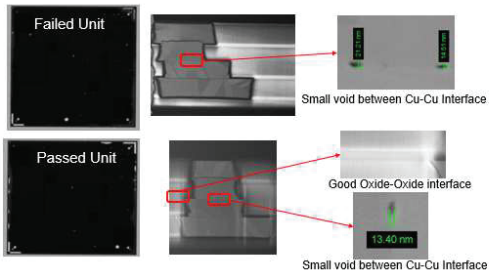


Figure 9: X section analysis for failed and passed unit

Reliability Assessment

Chips were tacked on wafer at 20N for 3sec after surface activation. The bonded units were subjected to MSL 3 with 3x reflow process and 1000TC after annealing process at 400ºC for 5 hrs. Figure 10 showed the wafer populated with chips.

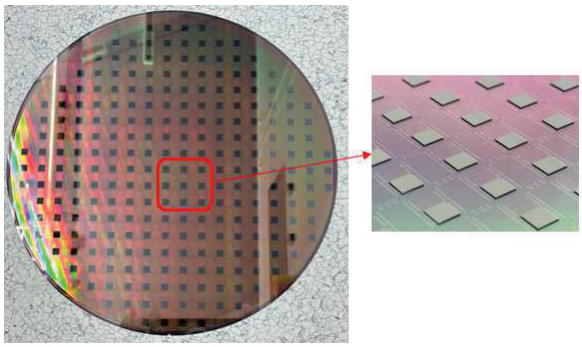


Figure 10: Wafer tacked with chips after annealing process

10k pads daisy chain results indicated no significant deviation before and after MSL 3 as shown in Figure 11a & 11b respectively. CSAM images as shown in Figure 12 indicated no significant delamination observed between the bonding interface. The bonded chips passed MSL 3 with 3x reflow. The wafer with bonded chips was subjected to temperature cycling of -40ºC/+125ºC.

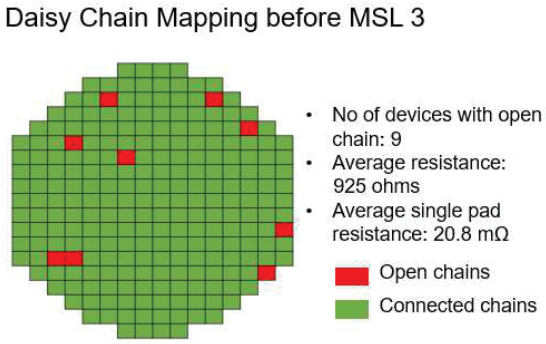


Figure 11a: Daisy Chain mapping before MSL 3

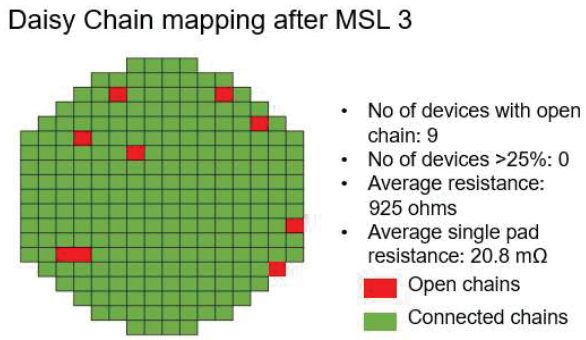


Figure 11b: Daisy Chain mapping after MSL 3

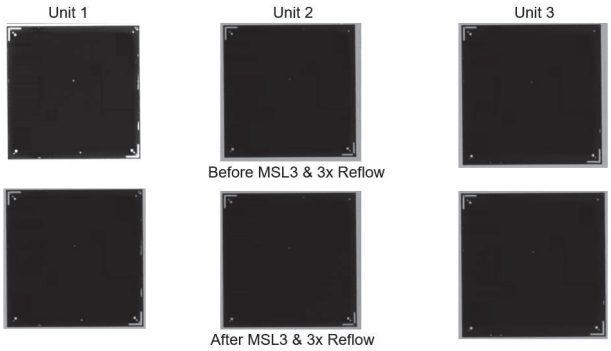


Figure 12: CSAM images before and after MSL 3 with 3x reflow

The daisy chain results after 1000 TC cycles indicated no further increased in units with open reading. However, there are total of 75 devices having resistance increased at least 25% above the reading at time zero. The daisy chain mapping after 1000 TC cycles is shown in Figure 13. CSAM images as shown in Figure 14 indicated intact bonding interface after 1000 TC cycles.

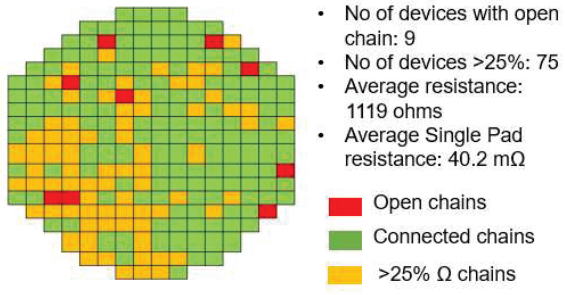


Figure 13: Daisy Chain mapping after 1000 TC cycles

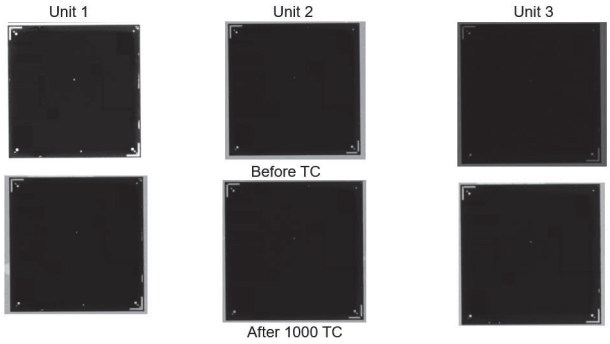


Figure 14: CSAM images before and after 1000 TC Cycles

Failure analysis was conducted on unit that had 25% increased in resistance values. The x section images as shown in Figure 15 indicated there are mini-voids between Cu-Cu interface. The voids maybe the reason why the resistance had increased. No severe delamination was observed in the bonding interface.

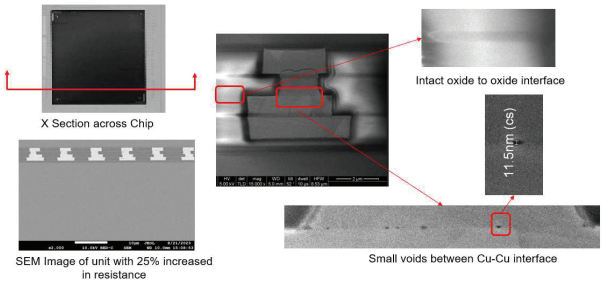


Figure 15: CSAM and X section images for unit with high resistance value

X section images of good unit indicated intact oxide to oxide interface and mini-voids between Cu-Cu interface as shown in Figure 16. No severe delamination oberved in the bonding interface.

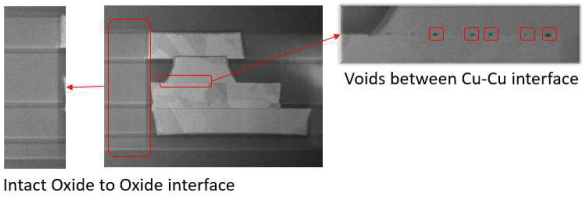


Figure 16: X section images of good unit

Conclusions

Reliability Assessment of 2.5D Module using Chip to Wafer Hybrid Bonding is carry-out with the following findings:

(a) Plasma treatment is optimized to achieve low contact angle and low surface roughness

(b) Cu dishing 4 to 8nm and oxide roughness ~0.3nm are essential for good Cu-Cu interconnects

(c) Good daisy chains yield can be achieved with lower annealing temperature of 350°C and shorter duration of 3hr with Cu dishing as high as 8nm
(d) Established chip to wafer hybrid bonding process passed both MSL 3 with 3x reflow and 1000 TC cycles

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