Process Challenges in Thin Wafers Fabrication with Double Side Hybrid Bond Pads for Chip Stacking

Mishra Dileep Kumar
*Institute of Microelectronics (IME), Agency for Science, Technology and Research (A*STAR) , 2 Fusionopolis Way, Innovis #08-02, Singapore 138634, Republic of Singapore*
mishra_dileep@ime.a-star.edu.sg

Vasarla Nagendra Sekhar
*Institute of Microelectronics (IME), Agency for Science, Technology and Research (A*STAR) , 2 Fusionopolis Way, Innovis #08-02, Singapore 138634, Republic of Singapore*
vasarla_nagendra_sekhar@ime.a-star.edu.sg

B.S.S. Chandra Rao
*Institute of Microelectronics (IME), Agency for Science, Technology and Research (A*STAR) , 2 Fusionopolis Way, Innovis #08-02, Singapore 138634, Republic of Singapore*
bhesetti_chandra_rao@ime.a-star.edu.sg

Ser Choong Chong
*Institute of Microelectronics (IME), Agency for Science, Technology and Research (A*STAR) , 2 Fusionopolis Way, Innovis #08-02, Singapore 138634, Republic of Singapore*
chongsc@ime.a-star.edu.sg

Vempati Srinivasa Rao
*Institute of Microelectronics (IME), Agency for Science, Technology and Research (A*STAR) , 2 Fusionopolis Way, Innovis #08-02, Singapore 138634, Republic of Singapore*
vempati@ime.a-star.edu.sg

***Abstract*—3D packaging with stacked dies is widely explored as a future advanced packaging technology for applications involving high-performance computing and High Bandwidth Memory (HBM) devices. In this direction, chip-to-wafer (C2W) hybrid bonding is an emerging technology that offers high I/O and heterogeneous integration of chips. For HBM stacking, the hybrid bond pads need to be fabricated on both sides. The backside process involves the wafer going through a temporary bonding and debonding (TBDB) process, and thus, the thermal budget of the fabrication processes is limited up to 200 °C. Therefore, a low-temperature PECVD-deposited SiCN was evaluated as the dielectric material for backside fabrication. This article focuses on the process challenges and mitigation plans in thin Wafers fabrication on 300 mm silicon wafer using the revised integration flows to enable four to eight memory chip stacking.**

Keywords—Hybrid bonding, Memory chip stacking, SiCN dielectric, TBDB, CMP optimization

I. INTRODUCTION

With the advancement in communication devices and artificial intelligence (AI), increasing performance with higher speed and lower form factor is critical [1-3]. The data-centric future demands have put increasing demands for advanced logics such as CPU, GPU, memory story system and high bandwidth memory (HBM). Chiplets and Heterogeneous Integration (HI) technologies are expected to drive performance and efficiency enhancement of semiconductor modules while Si scaling is slowing down. High-speed memory storage capacity is becoming necessary to meet the ever-increasing demand for Artificial intelligence (AI) and data centers. In this regard, there is need to increase the interconnect or I/O density at the backend-of-the-line (BEOL) using advanced packaging methods. Conventional bump-based technologies such as C4 microbump using underfill can support the interconnect pitch down to 20 µm. In this regard, advanced packaging technology, such as hybrid bonding technology for chip stacking is explored for HBM devices with pitch < 10 µm. Hybrid bonding is a key enabler trend of more than Moore. Several semiconductor industry players are developing the hybrid bonding method by reducing the feature size and pitch to further increase the I/O density.

There are several approaches for hybrid bonding such as Wafer-to-wafer (W2W), Chip-to-wafer (C2W), and Chip-to-chip (C2C) bonding. Hybrid bonding using W2W approach has been well established for NAND stacking, CMOS BSI and is in production for a few years while C2W and C2C hybrid bonding is still in the early stage before it is ready for production. C2W hybrid bonding is a key technology in fine-pitch packaging, offering heterogeneous integration of dies for various applications. Moreover, C2W hybrid bonding has a relatively better yield due to the selection of known good dies (KGD) as compared to W2W hybrid bonding.

The hybrid bonding requires stringent chemical mechanical planarization (CMP) process control for roughness and dishing to obtain a good bonding interface. During the hybrid bonding process, the surface of the substrate and chip component is subjected to plasma activation, followed by DI water rinse to form a silanol group. The silanol group promotes hydrogen bonding during tacking, and subsequent annealing forms a covalent bond (Si-O-Si) [4-5]. Subsequently, a high-temperature post-bond anneal step is done to develop Cu-Cu joint by thermal diffusion [6].

Multi-chip stacking and bonding require fabricating a hybrid bond pads on both sides of the wafer. The device wafer frontside fabrication is performed using a standard single copper damascene process flow for the RDL and hybrid bond pad layer. Afterwards the wafer is subjected to temporary bonding with a carrier wafer. Then, the device wafer is backgrinded to the required chip thickness. The backside fabrication is to be carried out on temporary bonded wafers,

which are non-standard wafers. This article discusses the different process challenges encountered during backside damascene flow on 300 mm silicon wafers and its mitigation plans. Later, C2W hybrid bonding evaluation was performed, and four-chip stacked module was demonstrated.

II. TEST VEHICLE DESIGN

The memory test vehicle chip was designed to have TSVs, RDL Cu metallization, and a hybrid bond layer on the front-side and a hybrid bond pad layer on the backside. For the frontside, single damascene flow was implemented using high temperature dielectrics while the backside flow was implemented using low temperature SiCN on the TBDB wafer. A schematic of the four-memory chip stacked on the bottom substrate is shown in Fig. 1.

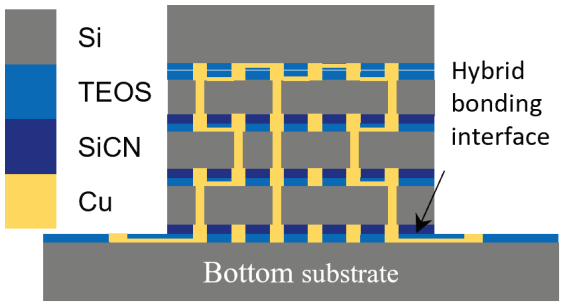


Fig. 1 Schematic of four-chip stacked on the bottom substrate.

The test vehicle also had daisy chain structure for continuity check between memory chip and bottom substrate. The number of hybrid bond pads was > 750,000 on each side of the wafer. The daisy chain structure was designed such that individual memory chips form a daisy chain connection through the bottom substrate, allowing electronical measurements across all four memory chips. The comb/meander structures were designed for leakage measurement, and the Kelvin via structure was designed for contact resistance measurement of single hybrid bond pads. The specific details about the memory chip size, critical dimensions, and pitch are listed in Table 1. Memory chips #1 to #3 had TSVs and were fabricated on the same wafer, while the memory chip #4 was fabricated separately without TSV.

TABLE I. TEST VEHICLE DESIGN PARAMETERS

Parameters	Values
Chip size	13 x 6 mm
Minimum trace width/space	2µm/2 µm
TSV size	4.5 x 50 µm
Chip frontside RDL Cu pad	Ø6 µm
Chip frontside hybrid bonding pad	Ø5 µm
Chip backside hybrid bonding pad	Ø5 µm
Hybrid bond pad pitch	10 µm

III. PROCESS CHALLENGES DURING BACKSIDE HYBRID BOND PAD FABRICATION

During the fabrication of the hybrid bond pads on the backside of the 300 mm silicon wafers, different process challenges have been encountered. The process challenges include a selection of a suitable dielectric material and unit process optimization, chip-level warpage control, Cu patches at the wafer edges, and front-side wafer surface roughness impact by the TBDB glue material. These challenges are addressed by adopting new process integration methods, as discussed in the following sections.

A. Selection of the backside dielectric material

Due to the thermal budget of the glue material, the temporary bonded wafer cannot be processed at temperatures exceeding 200 °C. The available choices of low temperature dielectrics include polymer, tetraethyl orthosilicate (TEOS), and Silicon carbon nitride (SiCN). As reported in the literature, polymer dielectric material has the outgassing issues during post-bond annealing [7-9]. Whereas use of low-temperature deposited TEOS dielectric results in non-bondable chips and void formation due to poor film quality. The SiCN had a higher number of dangling bonds and hydroxyl groups formed than TEOS [10-12]. SiCN film known for higher bond energy at lower deposition and annealing temperatures [13]. Thus, in the present work, SiCN was explored as a dielectric material to fabricate hybrid bond pads on the device's backside.

The SiCN deposition at lower temperatures results in higher non-uniformity of film thickness and lower density, which are significant concerns for hybrid bonding. Therefore, the low-temperature CVD process requires optimization to improve the density to reduce the outgassing issues and film thickness uniformity. Additional densification steps may be included in the post-CVD process to reduce the film porosity.

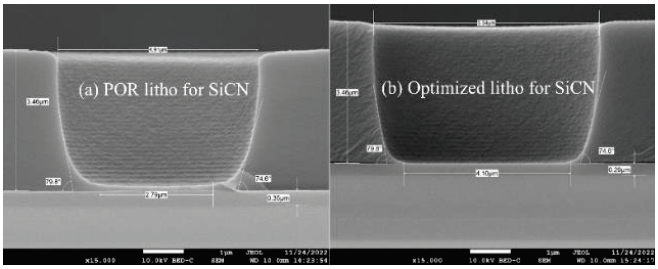


Fig. 2 SiCN lithography: (a) Using POR recipe and (b) Using optimized recipe.

Generally standard TEOS film needs lithography exposure dose < 100 mJ/cm^2 to open the required critical dimension (CD) in the positive tone photoresist. Compared to the TEOS, the refractive index of the SiCN dielectric is different and needs lithography recipe optimization. Fig. 2(a) shows an XSEM image with a lower bottom critical dimension (CD) after development using the process of record (POR) recipe. Therefore, a photoresist focus exposure matrix (FEM) was performed, and the lithography recipe was optimized to get the

desired CD using a lithography exposure dose > 130 mJ/cm^2 (Fig. 2(b)). After this, the etching rate of SiCN film also needs to be tuned due to difference in the etch rate compared to standard TEOS dielectric. Different gases and flow rates were explored to reach an optimized etch recipe.

In addition, the CMP recipe for SiCN needs to be redeveloped due to differences in mechanical properties such as hardness, density when compared to standard dielectrics. In general, the hardness and density of the dielectric film deposited at higher temperature is more than the film deposited at lower temperature [14]. The hardness of the TEOS and SiCN films also varies when deposited at same lower temperature i.e. < 200 °C. The film hardness values were measured using nano indentation test and it was found that that the low temperature TEOS hardness was approximately three times higher than SiCN film. During the CMP process the rate of removal is related to the film hardness and CMP recipe needs modifications as per the dielectric material. Generally, the CMP process is performed in two steps i.e. Cu and dielectric CMP. The Cu CMP is performed in two sequence which includes the bulk Cu removal by applying higher pressure across the different zones. The maximum Cu removal happens during the bulk Cu CMP step. After this, the remaining Cu is removed in the Cu clearance step in which a lower pressure is applied across the wafer. The complete removal of the Cu is ensured by the end point trace method. Finally, the wafer is subjected to dielectric/barrier CMP to polish away the seed layer and small amount of dielectric material. The SiCN CMP recipe was optimized in all these steps to get hybrid bonding compatible surface topography, i.e., dielectric roughness < 0.3 nm and Cu dishing < 5nm across the wafer, as shown in Fig. 3.

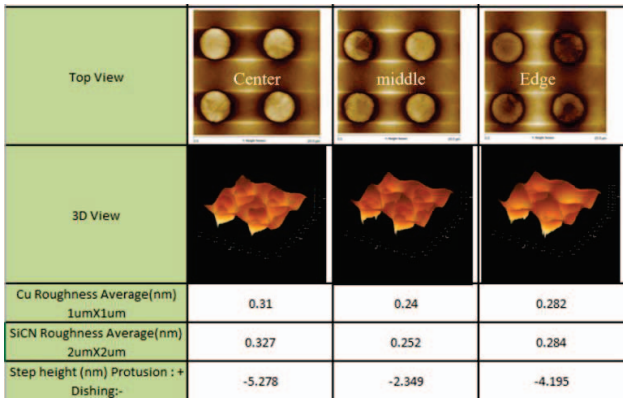


Fig. 3 AFM results for SiCN dielectric using optimized CMP recipe across three locations on the wafer.

B. Cu patch at the wafer edges on the temporary bonded device wafer

The backside fabrication of the hybrid bond pad was performed on a TBDB wafer. After the Temporary bonding, the device wafer was thinned down to 50 µm using the backgrinding process. The device wafer total thickness variation (TTV) was observed to be < 2 µm after the backgrinding process. Then the wafer was flowed down for the backside hybrid bond pad fabrication using the SiCN dielectric. During the CMP process, Cu patches mostly concentrated at the wafer edges were observed using the POR recipe, as shown in Fig. 4(a). The presence of Cu patches results in particle contamination during the dicing process and lowers the yield.

The Cu patch is not observed when CMP is performed on non-TBDB wafers. Therefore, we speculate that there can be several reasons for the occurrence of Cu patch. For example, it may be caused by the formation of edge bead during the TBDB process. Cu patches on the temporarily bonded wafer after the CMP process also might be the resultant effect of glue material TTV and backgrinding process. Therefore, the Cu patch issue mitigation should be a co-optimization effort across various process modules.

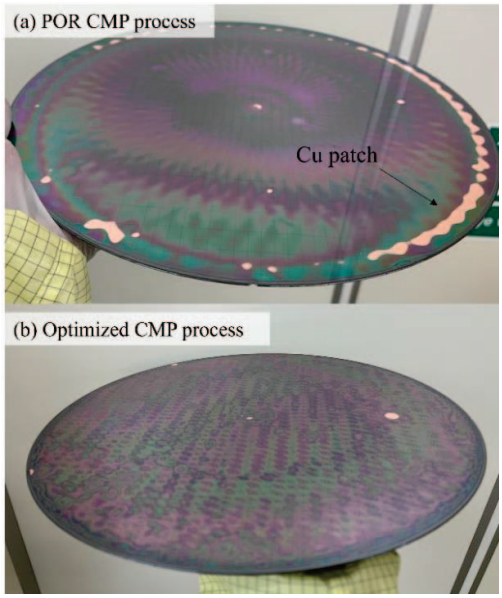


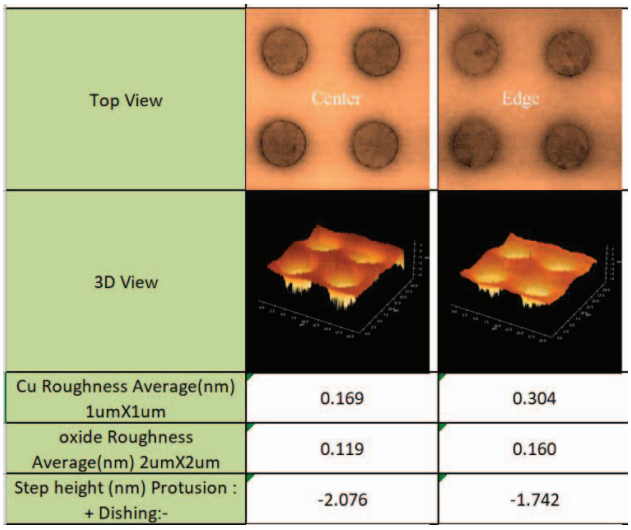
Fig. 4 Wafer level Cu patch on TBDB wafer after CMP process: (a) high Cu patch at wafer edge using POR CMP recipe and (b) low Cu patch using optimized CMP recipe.

Currently, most of the TDBD glue materials used is more suitable for TSV revealing flows where the glue thickness is ~ 80-100 µm. The exact TBDB flow used for TSV cannot be adopted for the thin memory wafer handling specially for hybrid bonding applications. The glue coating thickness plays a crucial role in lowering the overall TTV and edge bead formation. Therefore, there is a need to lower the glue thickness and edge bead formation. In the CMP point of view, different slurries and zonal pressure modifications were evaluated during the CMP process to minimize the Cu patches. Zonal pressure modifications to reduce the Cu patch is quite challenging as there is a risk of wafer slipping due to zonal pressure imbalance.

Fig. 4(b) shows the wafer image with a lower Cu patch obtained using an optimized CMP recipe. The Cu patch was reduced substantially, however, few Cu patch was still observed. It will require more optimization in the process flow and CMP process to eliminate the Cu patch on TBDB bonded device wafer.

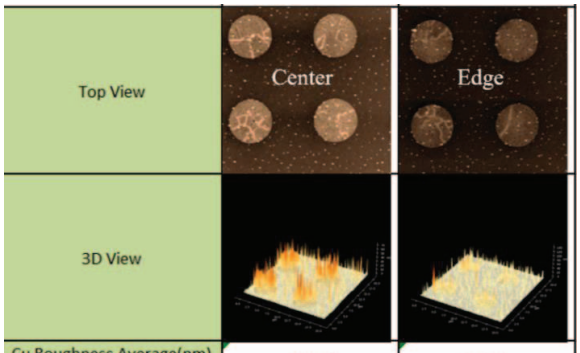
C. Frontside Surface modification by the TDBD glue material

Frontside surface quality preservation is another challenge for thin wafer fabrication using temporary bonding flow. After the backside hybrid bond pads were fabricated, the device wafer was debonded from the carrier wafer. Fig. 5 shows AFM results after the CMP process, i.e., before the temporary bonding process where front-side the TEOS dielectric surface topography was within specifications. The dielectric roughness was < 0.3 nm and Cu dishing was < 5 nm across the wafer.



Cu Roughness Average(nm) 1umX1um	0.169	0.304
oxide Roughness Average(nm) 2umX2um	0.119	0.160
Step height (nm) Protusion : + Dishing:-	-2.076	-1.742

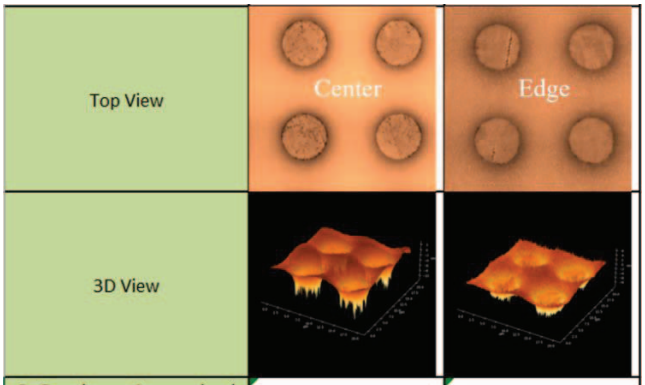
Fig. 5 AFM results on the frontside hybrid bond pad, i.e., TEOS surface before temporary bonding.



Cu Roughness Average(nm) 1umX1um	6.573	5.425
Oxide Roughness Average(nm) 2umX2um	1.458	2.164
Step height (nm) Protusion : + Dishing:-	20.563	17.461

Fig. 6 AFM results on frontside hybrid bond pad, i.e., TEOS surface after temporary debonding using POR integration flow.

However, after the debonding process, the frontside surface topography was severely altered. This alteration happened due to the interaction of the TBDB glue material with the dielectric material and the Cu pads. The dielectric surface i.e., TEOS roughness increased to > 2 nm, and the Cu dishing increased to ~17 to 20 nm across the wafer, as shown in Fig. 6. The altered dielectric surface badly affects the subsequent hybrid bonding process. This high roughness of the dielectric makes the chips non-bondable during the hybrid bonding process, and it needs to be mitigated.



Cu Roughness Average(nm) 1umX1um	0.451	0.298
Oxide Roughness Average(nm) 2umX2um	0.161	0.242
Step height (nm) Protusion : + Dishing:-	-2.179	-2.532

Fig. 7 AFM results on frontside TEOS surface after temporary debonding using modified integration flow.

To mitigate the glue residue and dielectric interaction, there are several methods reported in literatures. An additional protection layer such as monolayer protection, thin metal capping can be used before the TBDB process to protect the underneath dielectric and Cu layer [15]. The selection of TBDB material itself is critical to minimize the surface modification. In this regard, few TBDB materials were evaluated that are generally used for TSV revealing flow. Most of the TDBD glue materials were observed to be attacking the dielectric and Cu material and nanometric change in the surface topography was obtained. Another way to overcome this issue is modification in the integration flow to recondition the wafer back to desired roughness. Fig. 7 shows the AFM results after the debonding process using the new integration flow involving reconditioning CMP process to restore surface topography. On the wafer's front-side, the TEOS roughness restored back to pre TBDB surface condition i.e., dielectric roughness < 0.3 nm, and Cu dishing < 5 nm across the wafer.

D. Chip level warpage

During C2W tacking and bonding process, chip-level warpage plays a vital role in achieving successful hybrid bonds. Minimal chip warpage promotes good tacking. High chip warpage can result in non-tacking of the chips, which leads to

chip corner delamination, or chip drop-off during subsequent plasma treatment and DI water clean. Therefore, a modification in the fabrication process flow was evaluated to mitigate the chip-level warpage issues. Initially the chip warpage was found to be very high > 150 µm using standard fabrication flow for the SiCN film at the backside as shown in Fig 8. The chips were non-bondable to the bottom substrate wafer.

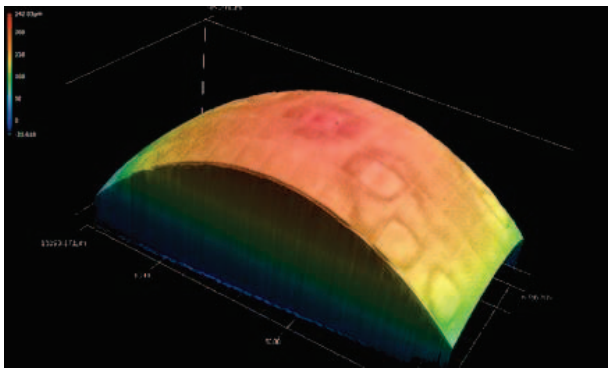


Fig. 8 chip warpage > 150 µm with SiCN facing up.

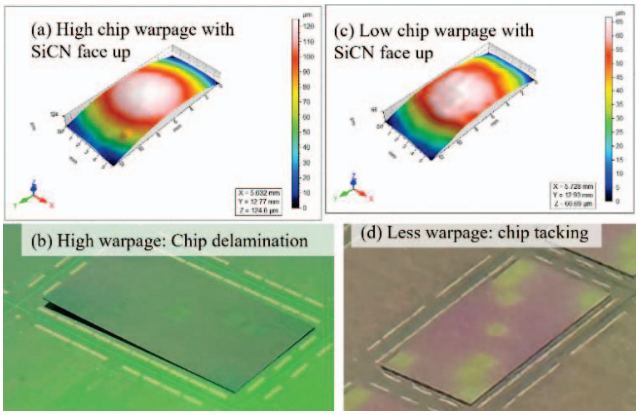


Fig. 9 Images showing the effect of the chip warpage: (a, b) Higher chip warpage resulting in chip delamination, (c, d) Lower chip warpage resulting in successful chip tacking.

After the modification in the fabrication process to manage the stresses, the chip warpage was reduced. The results with slightly lower warpage > 120 µm where the chips were bondable with corner delamination is shown in Fig. 9(a, b). After the chip tacking process in hybrid bonding, the dielectric interface bonding happens by the weaker hydrogen bonding and it is during the post-bond annealing, a stronger co-valent bond is formed. Thus, chips with high warpage, the corner starts delaminating within few hours. Therefore, it is needed to reduce the chip warpage further to promote chip tacking without any delamination. The chip warpage was reduced to the desired level < 70 µm using similar approach of stress reduction, and the chips were successfully tacked, as shown in Fig. 9(c, d).

IV. C2W HYBRID BONDING AND E-TEST

After mitigating the above process challenges, the thin memory test wafer with hybrid bond pads on both sides was fabricated using the optimized unit steps and fabrication flow. Later, the wafer was singulated and plasma treated. Back-to-face flip chip bonding approach was used for memory chip stacking. The first three memory chips had a thickness of 50 µm, while the top capping chip was 100 µm. Four-chip stacking of the memory chips was established using a bond force of 100 N for 30 seconds.

The XSEM image of a memory chip with properly aligned and void-free TSVs, RDL, and bond pads on both sides is shown in Fig. 10(a). The optical images showing subsequent tacking of the chips are shown in Fig. 10(b). No chip delamination and tacking voids were observed. The optical image for four-chip memory stacked on the bottom substrate wafer clearly showing the chip edges is shown in Fig. 10(c, d). After the chip stacking, post-bond annealing was performed to promote copper diffusion and form Cu-Cu joint.

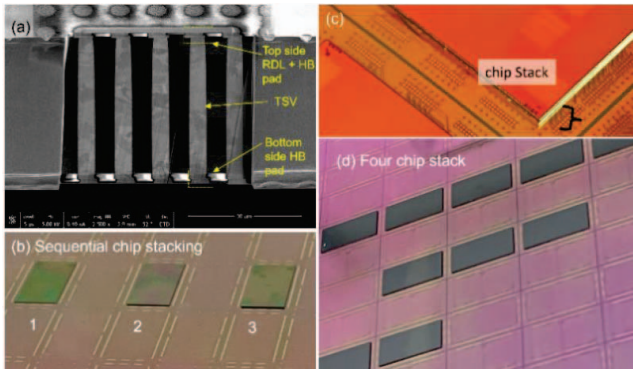


Fig. 10 Images showing: (a) XSEM of a single 50 µm thin memory chip with bond pads on both sides, (b, c) Sequential stacking of memory chips, and (d) Four chip stack module.

The XSEM images of the top chip, i.e., chip #4 with chip#3 having TSVs, are shown in Fig. 11. A good and void-free dielectric-dielectric bond interface has been demonstrated. Cu-Cu diffusion was achieved, and Cu merging was observed across the hybrid bond interface. Later, electrical testing was performed for the hybrid bonded four-chip stack module, and the daisy chain connection was measured successfully between memory chips and the bottom substrate with resistance values in the range of 17-19 ohms for ten daisy chain with hybrid bond pad connections. Further optimization in the unit fabrication steps, stacking and bonding methodology is in progress to increase the overall electrical test yield.

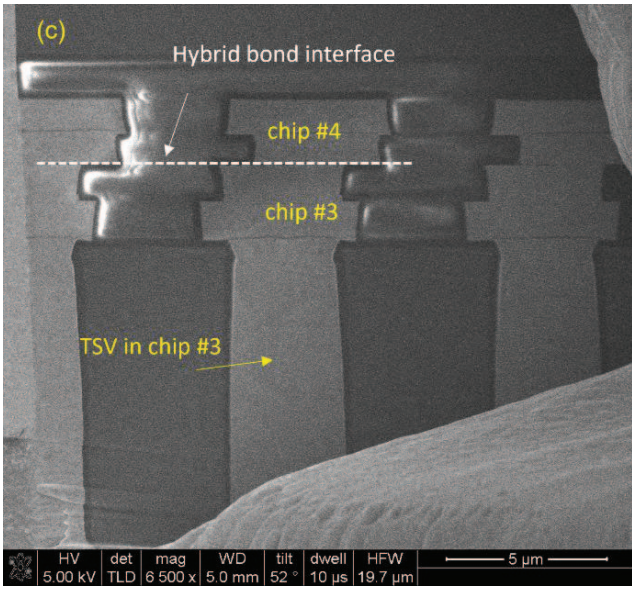


Fig. 11 XSEM analysis of hybrid bond pad interface.

V. CONCLUSIONS

The present article discussed the different process challenges encountered while fabricating thin memory test wafer with hybrid bond pads on both sides. The challenges were mitigated by optimizing the unit step process on 300 mm silicon wafers and modifying the integration flow. Finally, a four-chip memory stack module was demonstrated using a back-to-face hybrid bonding approach. A hybrid bonding interface with good dielectric-dielectric and Cu-Cu joints was demonstrated. Daisy chain connections for a four-chip stack were established with low-temperature SiCN and high-temperature TEOS dielectric.

ACKNOWLEDGMENT

This research was supported by the C2W hybrid bonding consortium project and the Agency for Science, Technology, and Research (A*STAR) under the Centre of Excellence in Advanced Packaging 3.0 (Grant No I2101E0008).

REFERENCES

[1] Zhou, W., Kwon, M., Chiu, Y., Guo, H., Bhushan, B., Street, B., Parekh, K. and Singh, A., "Critical Challenges with Copper Hybrid Bonding for Chip-to-Wafer Memory Stacking," 73rd Electronic Components and Technology Conference (ECTC), IEEE. May, 2023, pp. 336-341.

[2] Sekhar, V.N., Mishra, D.K., Choong, C.S. and Rao, V.S., "Thin Memory Chip Fabrication for Multi-stack Hybrid Bonding Applications", 24th Electronics Packaging Technology Conference (EPTC), IEEE. December, 2022, pp. 589-593.

[3] Choong, C.S., Jason Au Keng Yuen, Sekhar, V.N., Ismael Cereno Daniel Mishra, D.K., and Rao, V.S., "Reliability Assessment of 2.5D Module using Chip to Wafer Hybrid Bonding", 25th Electronics Packaging Technology Conference (EPTC), IEEE. December, 2023, (in press).

[4] Furuse, S., Fujii, N., Kotoo, K., Ogawa, N., Saito, S., Yamada, T., Hirano, T., Hagimoto, Y. and Iwamoto, H., "Behavior of Bonding Strength on Wafer-to-Wafer Cu-Cu Hybrid Bonding", *72nd Electronic Components and Technology Conference (ECTC), IEEE*. May, 2022, pp. 591-594.

[5] Mishra, D.K., Sekhar, V.N., Choong, C.S., Chandra Rao B.S.S., Chui, K.J., and Rao, V.S., "Evaluation of Low Temperature Inorganic Dielectric Materials for Hybrid Bonding Applications", 25th Electronics Packaging Technology Conference (EPTC), IEEE. December, 2023,(in press).

[6] Lau, J.H., "Recent Advances and Trends in Cu-Cu Hybrid Bonding", *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 13, No. 3 (2023), pp. 399-425.

[7] Sekhar, V.N., Takenori, Fujiwara, Hitoshi, Araki, Yu, Shoji, Masaya, Jukei, Kota, Nomura, Mishra, D.K., Choong, C.S., and Rao, V.S., "Polymer Dielectric Materials Evaluation for Hybrid Bonding Applications", 25th Electronics Packaging Technology Conference (EPTC), IEEE. December, 2023, (in press).

[8] Mishra, D.K., Sekhar, V.N., Choong, C.S. and Rao, V.S., "Evaluation of Polymer Materials for Hybrid Bonding Application", *24th Electronics Packaging Technology Conference (EPTC), IEEE*. December, 2022, pp. 357-360.

[9] Sekhar, V.N., Kumar, M.D., Lianto, P., Chong, S.C. and Rao, V.S., "Cu Damascene Process on Temporary Bonded Wafers for Thin Chip Stacking using Cu-Cu Hybrid Bonding", *73rd Electronic Components and Technology Conference (ECTC), IEEE*. May, 2023, pp. 564-570.

[10] Kim, S.W., Fodor, F., Heylen, N., Iacovo, S., De Vos, J., Miller, A., Beyer, G. and Beyne, E., "Novel Cu/SiCN surface topography control for 1 µm pitch hybrid wafer-to-wafer bonding" *70th Electronic Components and Technology Conference (ECTC), IEEE*. June, 2020, pp. 216-222.

[11] Peng, L., Kim, S.W., Iacovo, S., Inoue, F., Phommahaxay, A., Sleeckx, E., De Vos, J., Miller, A., Beyer, G., Beyne, E. and Zinner, D., "Advances in SiCN-SiCN bonding with high accuracy wafer-to-wafer (W2W) stacking technology", *International Interconnect Technology Conference (IITC), IEEE*. June, 2018, pp. 179-181.

[12] Rim, D., Lee, B., Park, J., Cho, C., Kang, J. and Jin, I., "The wafer bonding yield improvement through control of SiCN Film composition and Cu pad shape" *72nd Electronic Components and Technology Conference (ECTC), IEEE*. May, 2022, pp. 674-678.

[13] Brun, X.F., Hasan, M.M., Yang, Y., Carazzetti, P., Drechsel, C. and Strolz, E., "Characterization of 300 mm Low Temperature SiCN PVD Films for Hybrid Bonding application", *73rd Electronic Components and Technology Conference (ECTC), IEEE*. May, 2023, pp. 548-555.

[14] Nagano F, Iacovo S, Phommahaxay A, Inoue F, Sleeckx E, Beyer G, Beyne E, Gendt SD. Film characterization of low-temperature silicon carbon nitride for direct bonding applications. ECS Journal of Solid State Science and Technology. 2020 Dec 23;9(12), pp 123011.

[15] Hong ZJ, Liu D, Hu HW, Cho CI, Weng MW, Liu JH, Chen KN. Investigation of bonding mechanism for low-temperature CuCu bonding with passivation layer. Applied Surface Science. 2022 Aug 1;592, pp 153243.