150 Gbps THz Chipscale Topological Photonic Diplexer

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Abstract

Photonic diplexers are being widely investigated for high data transfer rates in on-chip communication. However, dividing the available spectrum into non-overlapping multicarrier frequency sub-bands has remained a challenge in designing frequency-selective time-invariant channels. Here, we report an on-chip topological diplexer exhibiting terahertz frequency band filtering through Klein tunnelling of topological edge modes. The silicon topological diplexer chip facilitates two high-speed channels with quadrature amplitude modulation (QAM) over a broad bandwidth of 12.5 GHz each. These channels operate at carrier frequencies of 305 GHz and 321.6 GHz, achieving a combined diplexer capacity of 150 Gbit/s. To ensure minimal interference between adjacent channels, a guard band is implemented. Topologically protected edge modes suppress the frequency selective fading of the broadband signals and hold promise for diverse integrated photonic applications spanning terahertz and telecommunication realms, including the design of lossless

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topological multiplexers, interconnects, antennas, and modulators for the sixth to X generation (6G to XG) wireless.

Introduction:

The emergence of global digitalization, massive internet of things (IoT), cloud and edge computing(*1*), and artificial intelligence-based applications(*2*, *3*) has directed the attention towards terabits per second (Tbps) communication links, one of the key visions of sixth-generation (6G) communication(*4*). Terahertz (THz) frequency band, the last frontier of radio frequency (RF) spectrum (1 Hz to 3000 GHz as per *ITU standard*) is envisioned as the key enabler to meet Tbps requirement of 6G communication links(*5*, *6*). The availability of large bandwidths along with high-resolution sensing capabilities of THz waves will herald the era of convergence of the imaging, computing, mobility and sensing domains to enable smart and energy efficient 6G networks(*7*). Emerging data-intensive applications rely on broadband THz devices, which include waveguides(*8*, *9*), filters(*10*), modulators(*11*, *12*), high-speed switches(*13*, *14*), phase shifters(*15*), power splitters(*16*), antennas(*17*) and interconnects(*18*–*21*). To leverage the bandwidth and aggregate data capacity of the THz band, frequency division multiplexer (Mux) and demultiplexer (Demux) need to be developed to enhance the spectral efficiency and to support advanced functionalities such as frequency-division duplexing (FDD)(*22*). In communication architecture, diplexer is a device that serves the purpose of multiplexing and demultiplexing of two non-interfering frequency bands. It could support two incoming, outgoing or both signals simultaneously(*23*). A diplexer is an integral part of a communication network operating at RF(*22*, *24*) and optical frequencies(*25*, *26*). However, at THz frequencies development of diplexer is still at an early stage. For instance, the first THz leaky waveguide diplexer showed an aggregate data speed of 50 Gbit/s for free space communication(*27*). Alternatively, dielectric slab waveguide (*28*, *29*), or photonic crystal (PC)(*30*) waveguide were utilized to achieve on-chip diplexers. Later, cavity-based silicon micromachined hollow waveguide diplexer was demonstrated, which involve complex fabrication and lack on-chip compatibility(*31*). Moreover, on-chip devices face significant challenges, including susceptibility to reflection or scattering losses, substantial bending loss, and inadequate channel isolation. Channel isolation is a critical requirement in frequency division multiplexing and demultiplexing operations. The existing Mux and Demux demonstrations are based on evanescently coupled waveguides(*32*), where channel bandwidth and crosstalk are extremely sensitive to changes in the coupling environment. In addition, the frequencies overlap between the adjacent bands in the coupled waveguides could result in adjacent channel interference (ACI)(*33*, *34*) therefore, on-chip filtering is required to separate two frequency bands to avoid signal distortions in each channel. To eliminate the reflection and scattering losses, recently, an on-chip demultiplexer is demonstrated in a topological waveguide-cavity device(*35*). However, the extremely narrow linewidth of the topological cavity limits the bandwidth (few hundreds of MHz) of the demultiplexed channel. Another state-of-art on-chip demonstration includes plasmonic circuit based add-drop multiplexer(*36*), where huge insertion loss due to Y-splitters before add-drop multiplexing operation limits device capability in realizing high-speed data transmission. Recently, a triplexer device was demonstrated using topological waveguides composed of

zigzag and bearded interface, which is again based on coupled waveguides approach (*37*). Therefore, novel design principles are required to address these challenges. Additionally, on-chip frequency band filtering techniques need to be developed for THz topological photonic integrated circuits (T^2PIC) for the future generations of on-chip high data-rate interconnect and wireless communication(*38*).

Here, we demonstrate a THz topological silicon (Si) based on-chip diplexer that supports FDM of two broadband channels. The topological diplexer chip is designed using valley photonic crystal (VPC)(*39*–*42*) that exhibits Dirac-like conical photonic band structure. Recently, there has been an open discussion on topological protection against backscattering due to structural defects.(*43*, *44*) We want to highlight that the fabrication process used in realizing the diplexer chip has a resolution of up to 0.5 µm, which is very small compared to the propagating wavelength (~ 300 µm @ 310 GHz) in the silicon slab. Therefore, topological protection at THz frequencies remains unaffected by minor fabrication tolerances. To achieve the FDM in the topological diplexer chip, photonic heterostructure is constructed with VPC unit cells having different bandgaps and Dirac frequencies. The shift in Dirac frequency of photonic band structure is equivalent to the 'potential shift', resulting a 'potential-barrier' for the topological edge modes while traversing across the topological diplexer chip. The Dirac-like dispersion ensures the unimpeded transport of topological edge modes through the potential barrier. This unique transport of the topological edge mode in the topological diplexer is attributed to '*Klein tunnelling*'(*45*), a relativistic quantum mechanical phenomenon that refers to near unity transmission of waves through a potential-barrier.(*46*) Leveraging the advantage of Klein tunnelling, our topological diplexer device operates through frequency band filtering rather than evanescent coupling, and demonstrate enhanced channel bandwidth with excellent isolation.

The essential feature of our demonstration includes: (i) Unravelling the underlying physics of "Klein tunnelling" that supports the topological transport of edge states through photonic heterostructures made of different bandgap unit cells. (ii) Silicon-compatible chip with dual channel multiplexing and demultiplexing capability. (iii) Bidirectional communication with highest aggregate data speed of 150 Gbit/s into two independent high-speed (75 Gbit/s) channels at the 300 GHz band. (iv) On-chip topologically protected THz spectrum filtering. (v) On-chip guard band feature to suppress ACI. Table I shows comparison between state-of-art diplexer demonstration to clearly highlight the novelty of our work in terms of channel filtering, group delay, coupling length, guard band feature, and underline principle involved in waveguiding mechanism.

Table I: New physics and performance comparison of our topological chip with the state of the art.

Diplexer Type	**Channel filtering**	**On-Chip compatibility**	**Channel group delay**	**Guard band**	**Coupling length**	**Waveguiding mechanism**	**Aggregate Data speed**
Micro-machined Waveguide diplexer (Ref. [31])	Coupled resonator	x	Dispersive	x	~3.3 λ	Index guiding	Not available
Photonic-crystal Diplexer (Ref. [30])	Coupled waveguide	✓	Dispersive	x	~λ	Photonic bandgap	~6 Gbit/s

							Mux + Demux
Dielectric waveguide diplexer (Ref. [28])	Coupled waveguide	✓	Dispersive	x	~5λ	Index guiding	~25 Gbit/s (Mux)
VPC waveguide diplexer (this work)	Bandwidth tailoring	✓	Non-dispersive	✓	~ 0.25* λ	**Klein tunneling**	**~150 Gbit/s** Mux + Demux

**λ: wavelength corresponding to the central frequency*

The topological diplexer design is based on Valley Photonic Crystal (VPC), composed of a honeycomb lattice of triangular holes. Fig. 1a shows the schematic of topological diplexer chip, composed of a honeycomb lattice of triangular holes. The rhombus shaped unit cell of VPC comprises of two equilateral triangular holes with side lengths l_1 and l_2 as shown in Fig 1. For a symmetric photonic crystal (i.e, $l_1 - l_2$) there exists a pair of Dirac points at K and K' valleys protected by lattice and time-reversal symmetric. Unlike PC, where the bandgap arises due to Bragg reflections(*47–50*), breaking the inversion symmetry of VPC by introducing $l_1 \neq l_2$, lifts the degeneracy of Dirac points and opens a photonic bandgap (additional detail in Supplementary Information Section S1).The sign of asymmetry, defined as $\Delta l = l_1 - l_2$, characterizes the topological properties of the VPC. For instance, the VPC with opposite signed Δl possesses opposite signed Berry curvature and valley-Chern numbers(*51–55*). Interfacing the VPCs with opposite signed valley-Chern number construct the domain wall that supports valley polarized edge states.

The edge states provide robust transport of THz signals through sharp bends, which is essential for device miniaturization. In addition, the linear dispersion of topological edge states yields constant group velocity across the entire bandgap, which is experimentally confirmed. The flat group velocity effectively allows the complete bandwidth to be used for on-chip communication for high throughput. To design the edge states in the desired frequency band, the central frequency of the bandgap is tuned by changing the VPC unit cell dimensions (including the periodicity), as discussed in Supplementary Information Section S2. The phase-linearity and time-invariant response (constant group velocity) of the edge states enables THz spectrum filtering through different topological VPC interfaces without introducing additional frequency-dependent time delay to the propagating broadband signal. Such time-invariant signature of the edge states is experimentally captured as group delay of the carrier signals in the communication channel, where group delay flatness is important to maintain the fidelity of the signal flowing through the chip. Preserving the nature of the VPC domain wall (interface of bigger triangular holes), irrespective of the unit cell periodicity, does not change the edge state's electromagnetic mode profile (additional detail in Supplementary Information Section S1). Another striking feature that topological protection offers is the reflection management of data transport in our topological diplexer chip. The valley selective transport of topological edge states plays an important role by routing the reflected signal to auxiliary port (Port 4 in Fig. 1c), that minimize the impact of reflection on channel bandwidth. In addition, the guard band feature in topological diplexer allows to separate two broadband frequency channels to ensure that both can transmit simultaneously without ACI. The topological VPC diplexer chip enables essential functionalities such as on-demand channel

filtering and full-duplex data transmission, which paves the path for developing high-density on-chip communication channels for 6G communication devices.

Our on-chip diplexer chip contains various domain walls made of photonic heterostructures with different bandgap regions. For example, type-*A* domain wall is constructed by VPC unit cells with bandgap ranging from 295-325 GHz. Similarly, type-*B* and type-*C* domain walls are composed of VPC unit cells having bandgap ranging from 285-307 GHz and 310-340 GHz, respectively (as shown in Fig. 1 and supplementary information Section S2). Data signal traversing through type-*A* to type-*B* domain walls is assigned as channel 1 (CH1), while type-*A* to type-*C* domain walls is labelled as channel 2 (CH2). Notably, the topological protection of edge states ensures robust and reflectionless transport of data signal even at the presence of large potential-barrier (i.e., across different types of domain walls) in the topological diplexer chip. The unimpeded penetration of topological edge states through the photonic potential barrier is because of 'Klein tunneling',(*45*), which arises in VPC owing to Dirac-like photonic band dispersion. The signature of Klein tunnelling results in the enhanced transmission at the lower frequency window for *AB* and *AC* domain walls as compared to the pristine domain wall, which could be explained from the conservation of valley pseudo spin in the topological diplexer chip (see details in Supplementary Information, Section S5).

Discussion:

Fig. 1a shows the schematic of the THz topological diplexer chip with Mux (2 x 1) and Demux (1 x 2) functionalities. The THz topological diplexer chip is made of high-resistive silicon (HR-Si) (see method section for fabrication details). The HR-Si offers low absorption loss, large non-dispersive refractive index (~3.42) and CMOS compatibility. Here, CMOS refers to the standard fabrication processes (photolithography, oxide deposition, reactive ion etching (RIE)) used by the semiconductor industry to fabricate integrated circuits. The ports (Port 1, Port 2, Port 3) associated with each VPC domain wall (grey, green, blue) selectively, supports one or both channel bandwidth centred around the carrier frequency (f_{c1}, f_{c2}). The schematic in Fig. 1a shows the aggregated data speed of 150 Gbit/s at the Mux Port 1, whereas a data speed of 75 Gbit/s is individually supported by the two Demux ports (Port 2 and Port 3). The image of rhombus-shaped unit cell at the bottom left of Fig. 1a highlights the periodicity (p), side length of equilateral triangular holes (l_1, l_2) and thickness (t) of the silicon (Si) slab. The methodology adopted in designing an on-chip diplexer device lies in the bandgap engineering of each topological bandgap region, as depicted in Fig. 2b. The waveguiding interface facing larger triangular air holes in each topological region is the zigzag arrangement of unit cells, which forms the domain wall (*A, B,* and *C*). The unit cells in each region have identical thickness but different periodicity (p_a, p_b, p_c) and air holes dimensions. The geometrical parameters allow to tailor the propagation bandwidth with broadband (domain wall *A*), and narrowband (domain wall *B, C*) waveguiding regions with a guard band to prevent interference between the two narrow bands. In our experimental configuration, we have used two narrow bands as independent communication channels (CH1, CH2) with carrier frequencies at 305 GHz and 321.6 GHz, respectively. Fig. 1c shows the optical image of the fabricated topological diplexer chip, where waveguiding domain wall of types *A, B*, and *C* have been highlighted (details of sample area with *A*, *B*, and *C* VPC region in Supplementary Information Section S3). The left portion (*A*-type) of the topological

diplexer chip contains a 50:50 power splitter to direct the entire bandwidth along Port 2 and Port 3 waveguiding regions. The top and bottom portions of the chip on the right-hand side act as low-pass and high-pass filters, respectively, to allow narrow bandwidth availability at Port 2 and Port 3. The extra frequency bands of type *A* domain wall reflect from *AB* and *AC* interfaces is guided back to the Port 4 due to the valley selective nature of edge states (Fig. S7 in supplementary information), which minimizes the impact of reflection on CH1 and CH2 bandwidth. This type of reflection management is unique and only occur in topological diplexer chip, resulting as enhanced performance metric such as high data rates (see Table I), and excellent channel isolation characterized by jitter analysis (see Table II) of the digital signal. The multiple bends along the waveguiding path showcases the resilience of data signals, attributed to the nontrivial topology of VPC. The experimentally recorded constellation plot on the right side of Fig. 1c further showcases the chip capability as a diplexer, where simultaneous injection of independent QAM-32 signals with different carrier frequencies at Port 1 is successfully retrieved from Port 2 and Port 3, respectively.

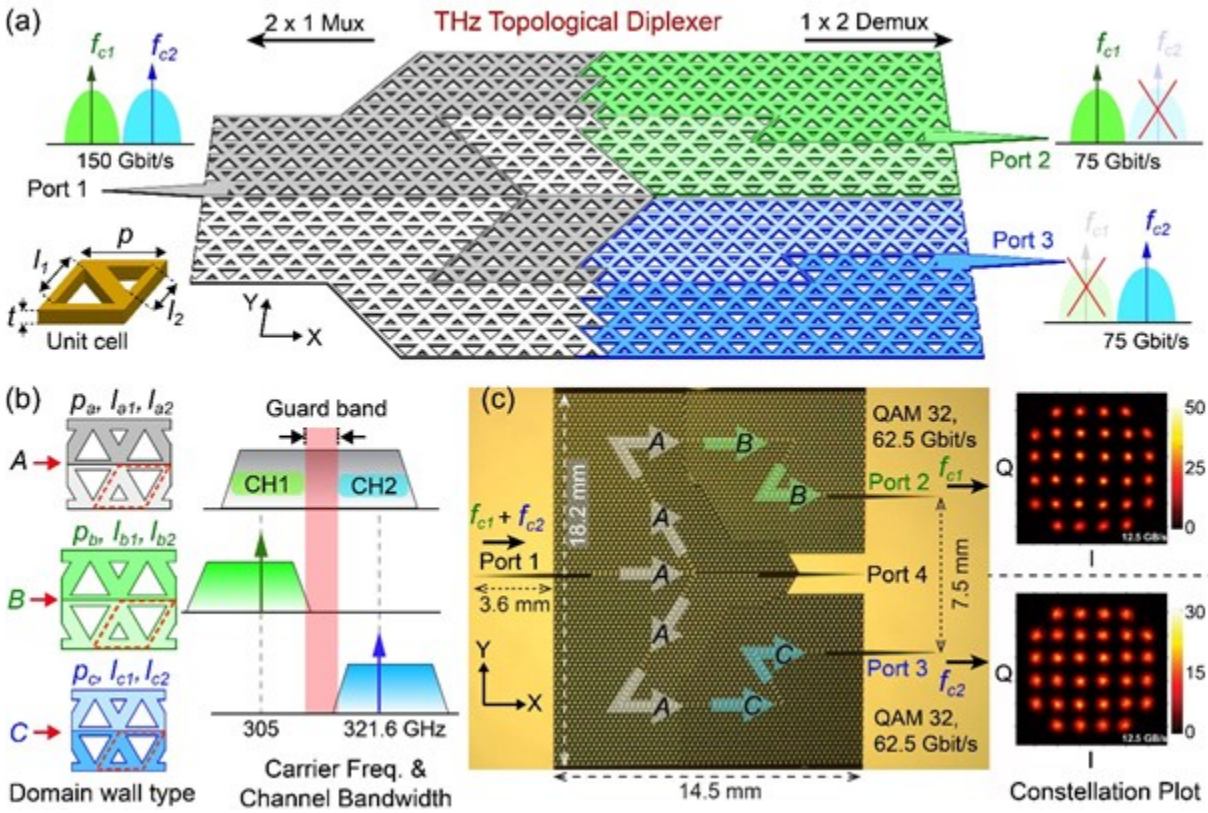

Fig. 1: THz topological diplexer chip for 6G communication. a) Schematic of topological diplexer chip for multiplexing/demultiplexing [Mux (Port 1) ↔ Demux (Port 2 + Port 3)] of the two 75 Gbit/s channels (green, blue) operating at two different carrier frequencies (f_{c1}, f_{c2}) to have an aggregate data speed of 150 Gbit/s. The coloured regions with triangular holes in the schematic represent three distinct topological VPC regions (grey green, blue). The bottom left image shows unit cell labelling (p: periodicity, t: thickness, l_1 & l_2: side length of triangular holes) to identify dimensional features of the dissimilar unit cell in each topological region. b) Unit cell arrangement on left with dimensions for *A* (p_a=258, l_{a1}=175, l_{a2}=85), *B* (p_b=262, l_{b1}=159, l_{b2}=92), and *C* (p_c=249, l_{c1}=175.5, l_{c2}=99.6) type domain wall for three distinct VPC regions (grey, green, blue). All dimensions are in microns (μm). The schematic on the right shows carrier frequency and channel bandwidth supported by each domain wall. The unused bandwidth between CH1 and CH2 is shown as the guard band highlighted by red shaded region. c) Optical image of the fabricated diplexer chip with wave

propagation path along *A, B,* and *C* type domain wall. Constellation plot on the right shows demultiplexed QAM-32 modulation signal (data speed of 62.5 Gbit/s) measured at Port 2 and Port 3, respectively.

The conservation of linear dispersion and modal profile of the topological edge states along *AB* and *AC* interfaces is vital for the lossless transfer of the propagating mode from one topological VPC region to another. Since the topological diplexer chip already contains a power splitter, minimum reflection losses at the interface (*AB* or *AC*) would reduce the power-penalty for error-free data communication. Fig. 2a shows the simulated projected band diagram for all three (*A, B, C*) zigzag interfaced supercells (additional details in Supplementary Information Section S1). The bulk bands (non-existence of edge states) at the top and bottom is represented by grey colour, while the topological edge modes corresponding to type *A*, *B* and *C* domain walls are indicated by coloured lines (green, grey, and blue) within the bandgap region. The topological edge states exhibit linear dispersion in the vicinity of the Dirac point (K or K'). The group velocities of the topological edge states for all three domain wall types are nearly identical, which ensures dispersion free transition of data signals while traversing from *A* to *B* (or *C*) domain walls. The overlap in the bandgap region (green background) between *A* and *B* forms the first narrow band channel (CH1), while the overlapping region between *A* and *C* (blue background) makes the second channel (CH2). The guard band region (red background) falls outside the bandgap region of the type-*B* and type-*C* domain walls. Fig. 2b shows the experimentally measured S-parameters when the THz waves is coupled to the diplexer chip at Port 1 and received at Port 2 and Port 3 (see method section for experimental setup details). The presence of bulk bands is the source of channel crosstalk in our diplexer device. In the lower frequency band (CH1) the channel isolation values lie in the range of 12 dB to 30 dB, while in the upper frequency band (CH2) the channel isolation values are in the range of 11 dB to 28 dB. The reflection measurements (S11, S22, and S33) at Mux and Demux ports are provided in Section S8 of supplementary information. The measured reflection coefficient S22 for CH1 and S33 for CH2 is slightly higher for some frequencies than S11 but still close to the -10 dB level. This mismatch could be due to the misalignment of tapered couplers with the WR-3.4 metallic hollow waveguides, an experimental limitation contributing to the reflection losses. The maximum value of transmission coefficient (S21 and S31) for CH1 and CH2 is -5 dB and -6.5 dB, respectively as shown in Fig. 2b. Since our device acts as an ideal power splitter, both S21 and S31 should be -3 dB. The tapered Si coupler for coupling the waves to the VPC domain wall(*56*) contributes additional insertion loss in both the channels (2 dB for CH1 and 3.5 dB for CH2, additional information in Supplementary Information Section S2 and S12). In addition to insertion loss induced by couplers, the additional losses in S21 and S31 are coming from the *AB* and *AC* interface. To quantify the losses between CH1 and CH2, we performed the reflection coefficient analysis presented in Fig. S4c of supplementary information. Fig S4c shows that the *AC* interface has a relatively higher reflection coefficient than the AB interface, which results in different levels of S21 and S31. The shaded green and blue regions in the S-parameter plot (Fig. 2b) represent the -3 dB bandwidth of CH1 and CH2, respectively. Both *AB* and *AC* interface reflect the frequency band corresponding to channel CH2 and CH1, respectively. This could introduce fluctuation in transmission bandwidth of diplexer chip when both *AB* and *AC* interface are present. Numerically calculated voltage standing wave ratio (VSWR) values in Fig. S4d of supplementary information, confirms the strong presence of out-of-band standing waves due to reflection from *AB* interface, which coincides with the CH2 bandwidth. This confirms that standing

waves are formed due to reflection from *AB* interface, which introduces large fluctuation in S31. The standing wave signature is also measured at Port 4 (S41 data in Fig. S7 supplementary information), where strong fluctuation is observed in frequency band associated with CH2 bandwidth. The S41 data also confirms that the guard band frequencies not supported by *B* and *C type* domain wall are dominantly reflected from *AB* and *AC* interface compared to CH1 and CH2 and guided back to Port 4 of the diplexer chip. The guard band is selected to be ~ 5 GHz to avoid any channel interference. Similar trends are observed when the diplexer chip is excited from Port 2 and Port 3, which are consistent with the simulation and experimental results (additional information in Supplementary Information Section S6). The same transmission coefficients for the back-and-forth port excitation confirm that the chip behaves as a passive on-chip diplexer. Fig. 2c shows the experimentally measured group delay for different frequency components at Port 2 and Port 3. The group delay measured at Port 2 and Port 3 are nearly 0.6 ns and remains flat for entire channel bandwidth at Port 2 and Port 3 owing to linear dispersion and topological protections of the edge states. The flatness in group delay ensures the utilization of the entire channel bandwidth for transmitting large bandwidth complex signals without any distortion. Due to measurement constraints, we have designed a large area chip.

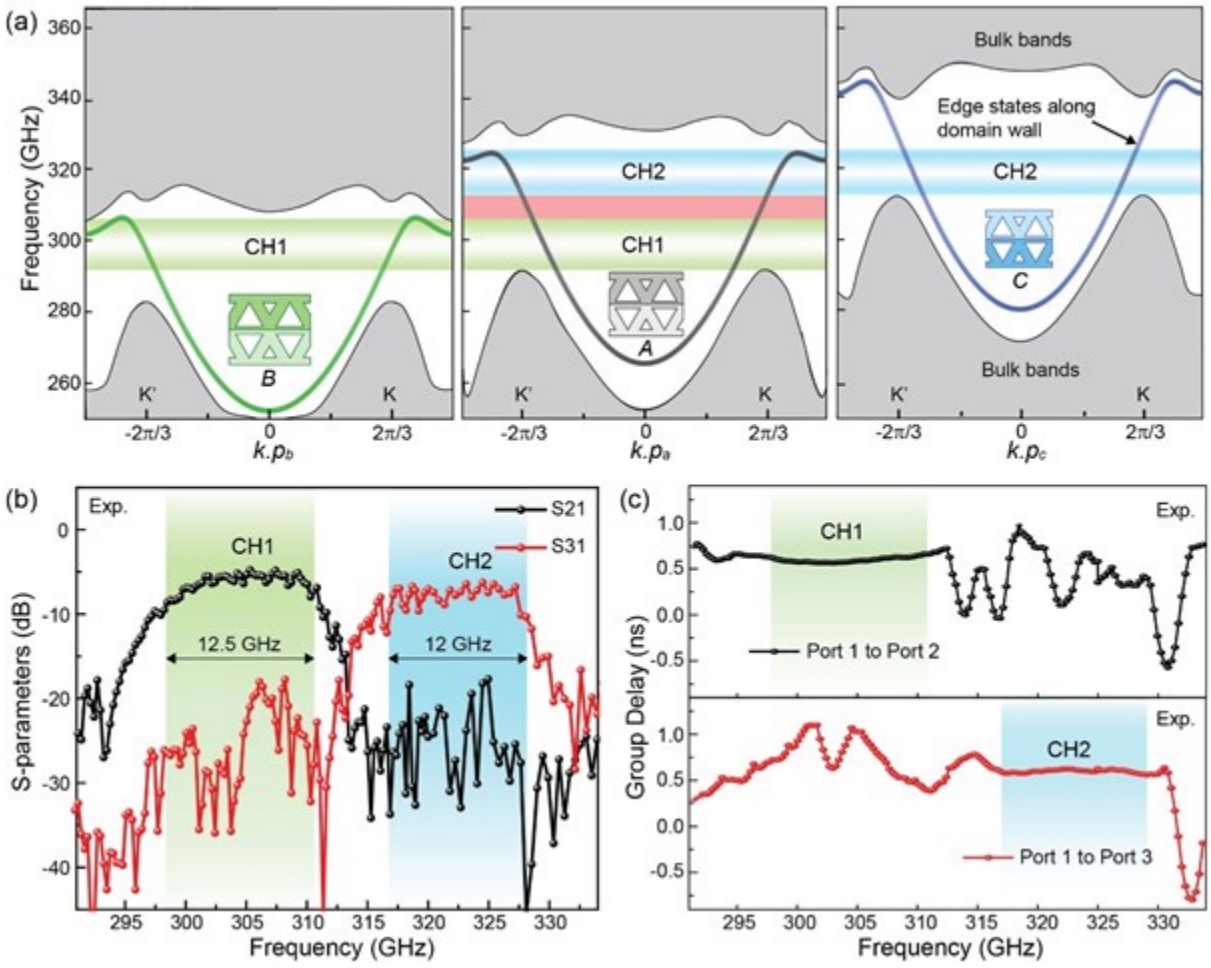

Fig. 2: Time-invariant topological diplexer with perfect channel isolation and flat group delay. a) Numerically calculated projected band diagram of zigzag interfaced domain wall of type A, B and C. Grey region represents bulk bands, while green, black, and blue curve represents edge states for domain wall of type A, B and C, respectively. The shaded green, blue, and red region represents the frequency band for

CH1, CH2 and the guard band, respectively. b) Experimentally measured transmission coefficient (S-parameters) from Port 1 to Port 2 (S21) and Port 1 to Port 3 (S31). The corresponding green and blue regions represent -3 dB bandwidth of CH1 and CH2, respectively. c) Experimentally measured group delay for various frequency components from Port 1 to Port 2 and from Port 1 to Port 3. Green and blue regions highlight the frequency band for CH1 and CH2, respectively.

We further demonstrated the performance of the topological diplexer chip in demultiplexing operation, using two independent transmitting channels carrying QAM-32 modulation signal centred around carrier frequencies f_{c1} (305 GHz) and f_{c2} (321.6 GHz). The two channels were simultaneously multiplexed (2 x 1 Mux) to WR 3.4 rectangular hollow waveguide by waveguide combiner, as shown in Fig. 3a, and coupled to Port 1 of the topological diplexer chip. The demultiplexed channels corresponding to CH1 (f_{c1} = 305 GHz) and CH2 (f_{c2} = 321.6 GHz) were individually recovered at Port 2 and Port 3 (chip and WR 3.4 waveguide images are shown in Fig. 3a). The recovered signal is down-converted to a baseband signal with a sub-harmonic mixer (SHM) and local oscillator (LO), which is analyzed by the real-time oscilloscope (RTO) for performance analysis (detailed experimental information in Supplementary Information Section S9). Fig. 3b shows the measured absolute spectral power (black solid curve) of 12.5 GBaud signals centred around the carrier frequencies (f_{c1} and f_{c2}) in both the channels (CH1 and CH2) at Port 1, to evaluate the modulated signals bandwidths. Each channel lies within the frequency band (red solid line with green and blue shaded region) supported by Port 2 and Port 3, respectively. We tested the device for maximum data transmission capability, where an aggregated data speed of 125 Gbit/s is demultiplexed into two channels, CH1 and CH2, of equal capacity. Each channel with 12.5 GBaud QAM-32 signal supports a data speed of 62.5 Gbit/s. Fig. 3c shows the Reference signal (at Port 1) and Demuxed signal (at Port 2 and Port 3) IQ constellation diagram corresponding to 62.5 Gbit/s measured from RTO at both ports. However, it is worth noting that the relative spread of IQ points at higher carrier frequency (f_{c2}= 321.6 GHz) for the Reference and Demuxed channel are larger in comparison to channel with lower carrier frequency (f_{c1}=305 GHz). This arises due to the additional high-frequency RF losses for CH2 from the measurement setup itself, rather than the diplexer chip. Furthermore, to quantify the signal transmission quality through the diplexer chip, we performed error vector magnitude (EVM) analysis at Port 1 and Demuxed port (Port 2 and Port 3) for the available transmitted power relative to Port 1, as shown in Fig. 3d. The linear dependence of EVM with relative transmitted power confirms that no additional signal distortion is observed due to propagation of THz carrier signals through the topological diplexer chip. It is evident that increasing the relative transmitted power improves the signal-to-noise ratio (SNR), thus reducing the EVM for both channels at the output ports of the diplexer chip. We also estimated the power penalty when the THz carrier signals propagate through the topological diplexer chip. Power penalty provides an estimated value of additional transmission power required to maintain channel performance (constant EVM) when measured with the diplexer chip inserted within the overall transmission system. The topological diplexer chip introduces a power penalty of 3 dB and 5 dB at Port 2 and Port 3, respectively, accounting for the additional losses measured for CH2 (Fig. 2c). The corresponding bit-error-rate (BER) texted in Fig. 3d at different EVM values with and without diplexer chip decreases with increase in received signal power. The topological diplexer chip is also tested for two channels multiplexing (MUXED) operation. To characterize the MUXED operation, we used QAM-16, QAM-32, and QAM-64 modulated signals at carrier frequencies

of 305 GHz and 321 GHz. The aggregate data rate corresponding to QAM 16, QAM 32 and QAM 64 are 100 Gbit/s, 125 Gbit/s, and 150 Gbit/s, respectively (additional detail in Supplementary Information Section S10). The strategy of power splitting and frequency band filtering via VPC domain wall could be further extended to realize multichannel FDM (see Section S13 in Supplementary Information).

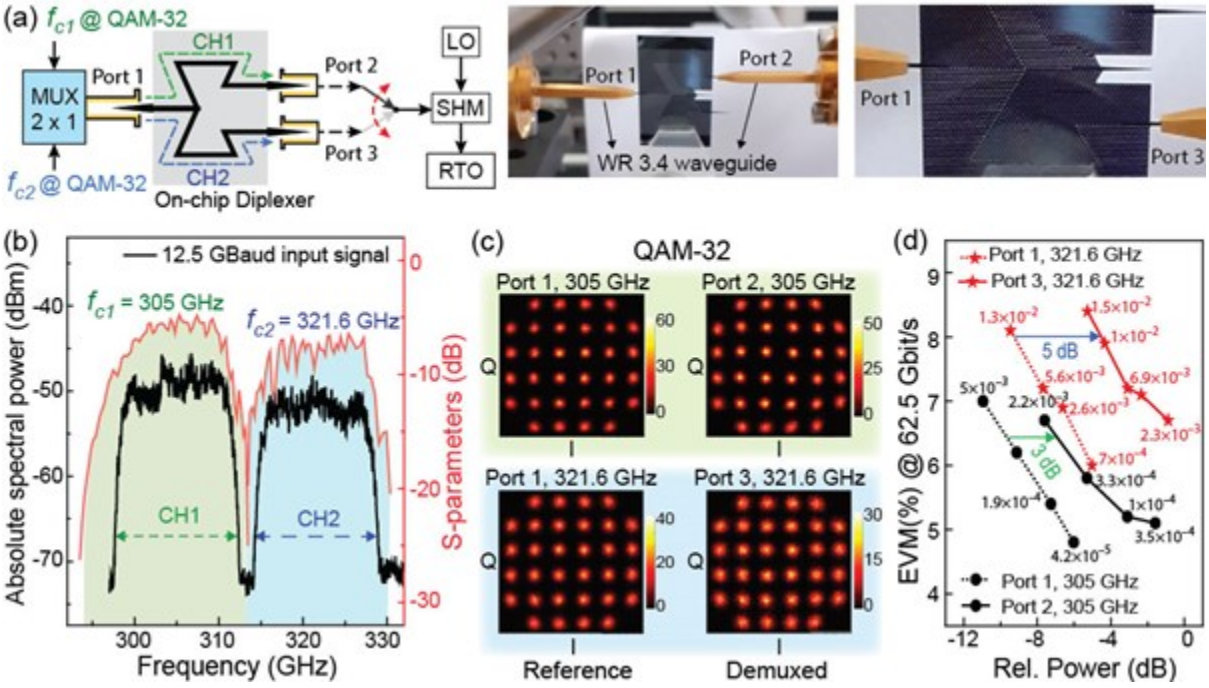

Fig. 3: Demultiplexing of two THz channels by topological diplexer chip. a) Schematic shows the basic configuration of measurement setup for the topological diplexer chip to capture QAM-32 modulated signal at carrier frequencies f_{c1} and f_{c2}. Images on the right shows the fabricated chip with waveguide ports arrangement in the experiment setup. b) Measured absolute spectral power (solid black curve) of the 12.5 GBaud input signal in two channels (CH1, CH2) centred around carrier frequencies f_{c1} (305 GHz) and f_{c2} (321.6 GHz). The red curve in the background shows S-parameters for signal transmission at Port 2 and Port 3, with the green and blue shaded regions for CH1 and CH2, respectively. c) QAM-32 IQ constellation diagram at Reference (without chip) and after channel demultiplexing (Demuxed) at Port 2, Port 3. d) EVM versus relative transmission power without (dotted line for Port 1 at 305 GHz and 321.6 GHz) and with (black solid line for Port 2 at 305 GHz, red solid line for Port 3 at 321.6 GHz) Demux operation. Graphs also shows the experimentally measured BER values at each point. 3 dB and 5 dB are the power penalty at the respective ports in demultiplexing operation by the diplexer chip.

We also recorded the eye pattern for THz carrier-mediated digital signal transmission with the lowest BER values. The eye diagram at specific BER values shown in Fig. 4 displays the variation in 'I' or 'Q' component of 12.5 GBaud QAM-32 signal with time, as triggered by the symbol clock. The eye diagrams retrieved before (Ref.: Port 1) and after the Demux operation (Port 2 & Port 3) through carrier demodulation shows the comparison between the received signal quality with and without the topological diplexer chip in a high-speed signalling environment. Nearly similar eye amplitude for the reference and Demux showcases the diplexer chip's robustness in maintaining the communication channel's signal integrity. The eye-opening for digital transmission at 321.6 GHz is lower than 305 GHz due to additional high-frequency RF losses for CH2. Table II shows the jitter analysis based on

the eye diagram shown in Fig. 4. The random jitter (RJ) is related to the noise in the communication channel, while the deterministic jitter (DJ) is associated with channel crosstalk and ACI in device. The measurement setup shows identical DJ value for both channels without the diplexer chip. S31 exhibits larger fluctuations than S21 in amplitude (Fig.2.b), but a slightly higher group delay dispersion (Fig.2.c). This induced a lower DJ value increase for CH2 than for CH1 in channel demultiplexing operation via the topological diplexer chip. The total jitter (TJ) is calculated by the summation of RJ and DJ, confirming the expected impact of the group delay dispersion.

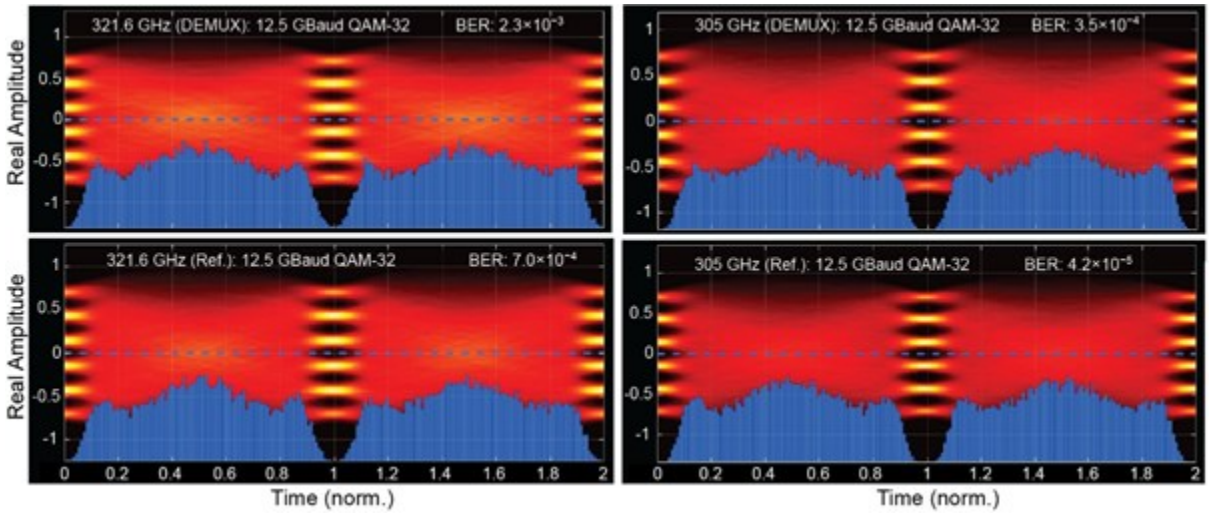

Fig. 4: Eye diagram of digital signal received through THz channels. Eye pattern of the demodulated 12.5 GBaud QAM-32 signal at Port 1 (Ref.) and after the channel demultiplexing (Demuxed) at carrier frequencies 321.6 GHz and 305 GHz. The dark blue graph in each eye diagram window represents the spread of points all around the time as digital signal makes transition from one voltage level to another ($t_0 \rightarrow t_1, t_1 \rightarrow t_2$).

Table II: Jitter calculation for 12.5 GBaud QAM-32 signal retrieved after the demodulation of THz carriers.

Carrier freq.	Meas. config.	BER	Symbol rate (GBaud)	Ts (ps)	Deterministic (DJ in ps)	Random (RJ in ps)	Total (TJ in ps)
305 GHz (CH1)	Ref.	4.2×10^{-5}	12.5	80	50.4	39.2	89.6
	Demux	3.5×10^{-4}	12.5	80	59.2	41.6	100.8
321.6 GHz (CH2)	Ref.	7.0×10^{-4}	12.5	80	50.4	42.4	92.8
	Demux	2.3×10^{-3}	12.5	80	54.4	41.6	96

**Ts: Interval per symbol, DJ: Deterministic jitter, RJ: Random jitter, TJ: Total jitter, ps: picosecond*

Conclusion:

In conclusion, we have experimentally demonstrated a chip-scale broadband THz topological diplexer for future 6G to XG wireless communication. The topological diplexer chip consists of photonic heterostructures (type A, B and C domain walls) constructed with VPC unit cells of different bandgap regions. The robust transport of data signal through the composite structures of the topological diplexer chip is supported by Klein tunnelling of the topological edge modes. Our devised topological diplexer chip preserves the topological features enabling time-invariant FDM of data signals with negligible crosstalk. The photonic diplexer chip supports two independent, well-isolated communication channels of 12.5 GHz bandwidth with nearly flat group delay. The average values of channel isolation for CH1 and CH2 in lower and upper frequency bands are 19 dB and 17.5 dB, respectively. We have achieved a maximum data speed of 75 Gbit/s per channel (and aggregated data rate of 150 Gbit/s) using higher order QAM-64 modulation format. Dual channel multiplexing and demultiplexing operating with an aggregate data speed of 150 Gbit/s in on-chip configuration will significantly contribute to the technological development of compact and low-loss THz integrated photonic devices. The diplexer chip architecture also provides design flexibility for single-chip full-duplex transceiver channels, which could play a key role in the chip-to-chip communication with high data rates through photonic devices. For emerging T^2PIC applications., the Klein tunnelling mediated transport of electromagnetic waves provide unprecedented way to control the flow of data signals, in particular, for on-chip isolators, filtering and wave-division multiplexing by harnessing the pseudo spin or valley degree of freedom.

Methods:

Diplexer chip fabrication:

The Si VPC diplexer chip was fabricated on 8-inch diameter HR-Si wafer (resistivity (ρ) > 10 kΩ·cm). The Si wafer was thoroughly cleaned, and 4 μm thick silicon-di-oxide (SiO_2) layer was deposited. Photolithography was used to define the triangular etch holes. SiO_2 was selectively etched away, exposing the Si surface. Deep reactive ion etching of Si was carried out to etch >200 μm of Si. The photoresist and SiO_2 layers were then completely removed. Back grinding of Si wafer was carried out for thinning down the wafer to 200 μm.

Numerical simulation:

The band structure calculations were performed using a numerical frequency domain solver (COMSOL Multiphysics). A rhombus-shaped unit cell composed of two equilateral triangular holes was designed with periodicity '*p*' (p_a=258 μm, p_b=262 μm, p_c=249 μm) and thickness '*t*' (200 μm). Floquet boundary conditions were employed in the VPC unit cell along both the x and y directions. In the eigenvalue solver analysis, we performed a parametric sweep of the *k*-vector such that it traces the point from Γ to M, M to K and K to Γ to cover the irreducible Brillouin zone. The detailed simulation results are discussed in Supplementary Information Section S1.

Experimental Section:

i) Vector-Network Analyzer (VNA) based THz characterization setup:

The fabricated diplexer chip is characterized using a set of vector network analyzer (VNA) based THz frequency extenders modules in the 220-325 GHz and 325-500 GHz ranges. In each frequency bands, the testing system is composed of a pair of frequency extenders (Z-325 and Z-500 type) driven by a ZVA-24 from Rodhe&Schwarz, with rectangular waveguide ports. The system was the first waveguide calibrated using a TRM (Thru, Reflect, Match) waveguide calibration procedure as per WR-3.4 or WR2.2 waveguide standards. After calibration, WR-3.4 is used to couple the input signal to Port 1 and collect the output signal from Port 2 and Port 3, respectively. The transmission curves as well as group delay measurements in Fig. 2b and Fig. 2c are the relative transmission measurement through the Si-VPC diplexer chip, ie the reference measurement is obtained by direct rectangular waveguide coupling at VNA ports in each band.

ii) THz communication experiment setup:

The testbed used for QAM-32 modulation experiment is composed of optically-modulated and fixed tunable laser lines at 1.55 µm, where the frequency difference fixes the operating carrier frequency in the optical to THz converters used. In all the tests, the 12.5 GBaud QAM-32 data signal generated by fast (64 GS/s) arbitrary waveform generator (AWG) is used to drive the optical modulator. One of three laser lines used is fixed (193.678 THz) and modulated using I/Q Mach Zehnder modulator. To generate the dual frequency THz test signal, a set of two photonics-driven THz sources (uni-travelling carrier photodiode, UTC-PD(*57*)) is used to generate the two THz carriers independently, before injection in the diplexer. The first THz source is established by mixing the 193.678 THz modulated laser with a fixed laser at 193.373 THz (leading to f_{CH1}=305 GHz), while the second is using a fixed laser line at 194 THz combined with the 193.678 THz line, leading to f_{CH2} = 321.6 GHz. Before each UTC-PD, an erbium-doped fiber amplifier (EDFA) is used to set the optical power that feeds each UTC-PD. The two THz carriers are then simultaneously injected within the diplexer Port 1, thanks to waveguide combiners operating in the WR3.4 band. Then the same WR3.4 injection waveguide is used to couple the data-flow into the diplexer. At the output Port 2 and Port 3 of the diplexer chip, the same WR3.4 waveguide is used to feed the THz receiver. This receiver comprises a sub-harmonic mixer (SHM, GaAs Schottky diodes technology) featuring 8–10 dB conversion losses in the operation band. An electronic multiplication chain pumps this SHM to down-convert the signal into an intermediate frequency (IF). The IF signal at SHM output is further amplified by a wideband 30 dB gain stage (SHF810) before detection using a fast real-time oscilloscope (RTO) with 70 GHz bandwidth. I/Q maps and EVM are computed using the VSA software and MATLAB routines. The detailed block diagram of the THz communication setup is presented in Supplementary Information Section S9.

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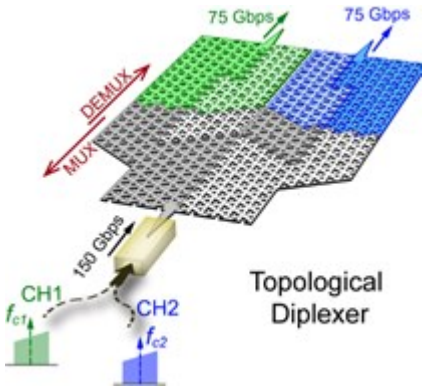

The on-chip photonic diplexer for 6G to XG communication works on the principle of power splitting and terahertz spectrum filtering. The topological nature of the silicon chip facilitates in simultaneous multiplexing (MUX) and demultiplexing (DEMUX) of two broadband 12.5 GHz channels (CH1 & CH2) to support an aggregated data speed of 150 Gbps.