# RF Performance Study of Through-Mold-Via (TMV) using L-2L De-Embedding Method

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**Abstract**

In advanced packaging, vertical interconnects enable the frontside to backside connections. This work presents a method to extract the RF characteristics of Through-Mold Via (TMV) using L-2L de-embedding method. Detailed equations and de-embedding procedures are demonstrated in this paper. Simulations and measurements of 3 TMV structures with different pitch are presented to validate the method up to 50GHz.

**Introduction**

In Fan-Out Wafer Level Packaging (FOWLP) with chips embedded in the molding compound, vertical interconnect Through-Mold Via (TMV) can be used to route signals directly between frontside and backside Redistribution Layers (RDLs) through the molding compound as shown in Fig. 1. With TMV and both sides RDLs, 3D integration and Package-On-Package (PoP) are possible [1]. It is important that the RF performance of vertical interconnections like Through-Silicon Via (TSV), µBump, and TMV is characterized for precise RF signal routing design and simulation. However, direct two-side measurement of vertical interconnect structures is hard to achieve.

To extract the RF characteristic of vertical interconnects, various modeling and extraction methods were demonstrated. In [2], Through-Reflect-Line (TRL) method was used to de-embed a co-axial TSV transition. Two TSV transitions were cascaded in a front-to-front configuration connected with two frontside CPW lines and one backside CPW line. TRL calibration was applied to a set of thru, open and different lengths of CPWs for both frontside and backside transmission lines to extract the CPW lines. With the scattering matrixes of both sides CPW sections and front-to-front cascaded structure known, the S-parameters of TSV transition can be derived. The extracted TSV transition shows good performance up to 30GHz. The TRL calibration method is well established and the de-embedding procedure is straightforward. However, sets of structures need to be fabricated and measured.

In [3], two-port S-parameters extraction of Sn/Ag bumps as the vertical interconnects bonding a CMOS chip to a glass substrate in flip-chip technology was demonstrated. Two sets of GSG bump transitions connecting a CPW transmission line on chip were divided into three cascaded elements as bump-TL-bump. With the T-matrixes of cascaded structure and TL known, the S-parameters of vertical bump transition can be derived. To obtain the characteristics of cascaded structure and TL, on-wafer testing of the structures with extended probing pads were performed. Sets of de-embedding structures were also measured to calibrate out the pads. The measurement and extraction were done up to 20GHz, and good consistence and validity of the proposed vertical bump transition de-embedding method are shown.

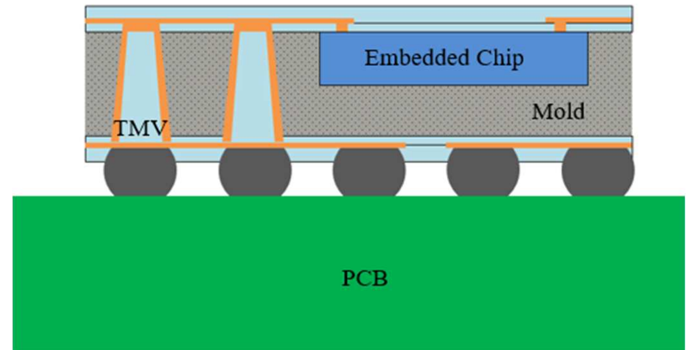



Fig. 1. Through-Mold Via (TMV) in Fan-Out Wafer Level Packaging (FOWLP) with chip embedded in molding compound.

The de-embedding methods in [2] and [3] both extract the vertical transition from a cascaded network. To de-embed out the cascaded elements, the characteristics of the cascaded elements need to be obtained first by other calibration methods. Additional de-embedding structures and measurements would be required. The RF characteristics extraction of the vertical transition therefore would also depends on the accuracy of the measurements and de-embedding of the cascaded elements.

L-2L (double-delay) de-embedding method [4] uses two transmission lines with the same width but one has twice the length of the other one as shown in Fig. 2 (a) and (b). Structure A and B are considered as cascade of multiple two-port networks, i.e. [A] = [PAD][FL][PAD] and [B] = [PAD][FL][FL][PAD]. ABCD-matrix of FL and PAD, [FL] and [PAD] can then be solved by equations (5) and (6). In [5], with two more structures of TLs at backside connecting to DUT which consists of two single TSVs connected by a frontside meander line, an extended L-2L de-embedding method was first demonstrated to extract the resistance, inductance and capacitance of the a single TSV up to 50GHz. In [6], L-2L de-embedding method was also applied for the de-embedding and characterization of CMOS transistor.

In this work, the S-parameters of three GSG TMV transitions with a pitch distance of 200 µm, 250 µm, and 300 µm are extracted using extended L-2L de-embedding method. The following sections show the de-embedding structures and methodology of the proposed method. The extracted S-parameters of fabricated TMV transitions up to 50GHz will be shown.

**L-2L De-Embedding Methodology**

The de-embedding structures are shown in Fig. 2. Structures (a) and (b) are the CPW TL at the front side with a TL length of FL and 2FL respectively. Structures (c) and (d) have two TSV transitions connecting the frontside CPW TLs and a backside CPW TL. In structure (c), the backside CPW has a length of BL while the backside CPW of structure (d) has a

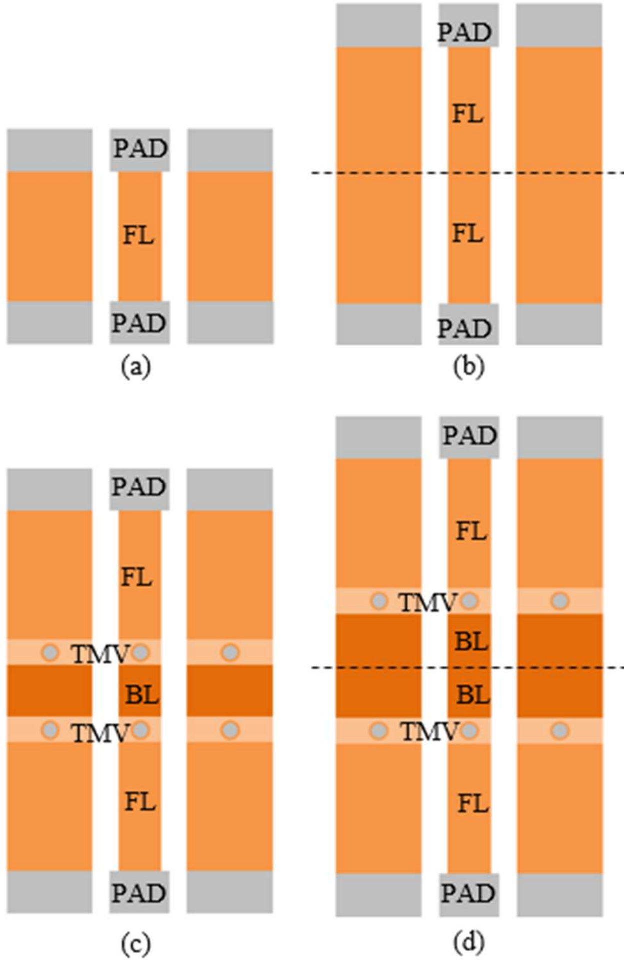



Fig. 2. Structures for extended L-2L de-embedding method. (a) Frontside CPW TL with a TL length of FL. (b) Frontside CPW TL with a TL length of 2FL. (c) TMV transition from frontside to backside with a backside TL length of BL. (d) TMV transition from frontside to backside with a backside TL length of 2BL.

length of 2BL. All structures including probing pads, TLs, and TMV transitions are symmetrical. The structures can be analyzed as a cascade of multiple two-port networks and each network is represented by an ABCD-matrix and expressed as Equations (1) to (4) as follows:

$$[A] = [PAD][FL][PAD] \tag{1}$$

$$[B] = [PAD][FL][FL][PAD] \tag{2}$$

$$[C] = [PAD][FL][TMV][BL][TMV][FL][PAD] \tag{3}$$

$$[D] = [PAD][FL][TMV][BL][BL][TMV][FL][PAD] \tag{4}$$

The ABCD-matrixes of [FL] and [PAD] can be derived from (1) and (2) as:

$$[PAD] = ([A]^{-1}[B][A]^{-1})^{1/2} \tag{5}$$

$$[FL] = [PAD]^{-1}[A][PAD]^{-1} \tag{6}$$

From (3) and (4), ABCD-matrix of TMV transition can then be derived as:

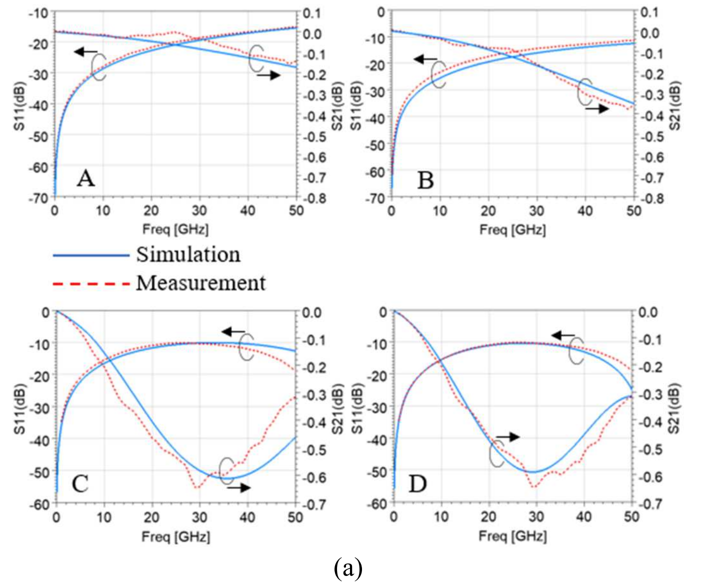
$$[TMV] = \left( \begin{matrix} [PAD]^{-1}[FL]^{-1}([C]^{-1}[D][C]^{-1})^{-1}[FL]^{-1} \\ [PAD]^{-1} \end{matrix} \right)^{1/2} \tag{7}$$

With both [PAD] and [FL] known, ABCD-matrix of TMV transition can be extracted and converted to S-parameters. The extraction algorithm is implemented using Keysight ADS 2020.

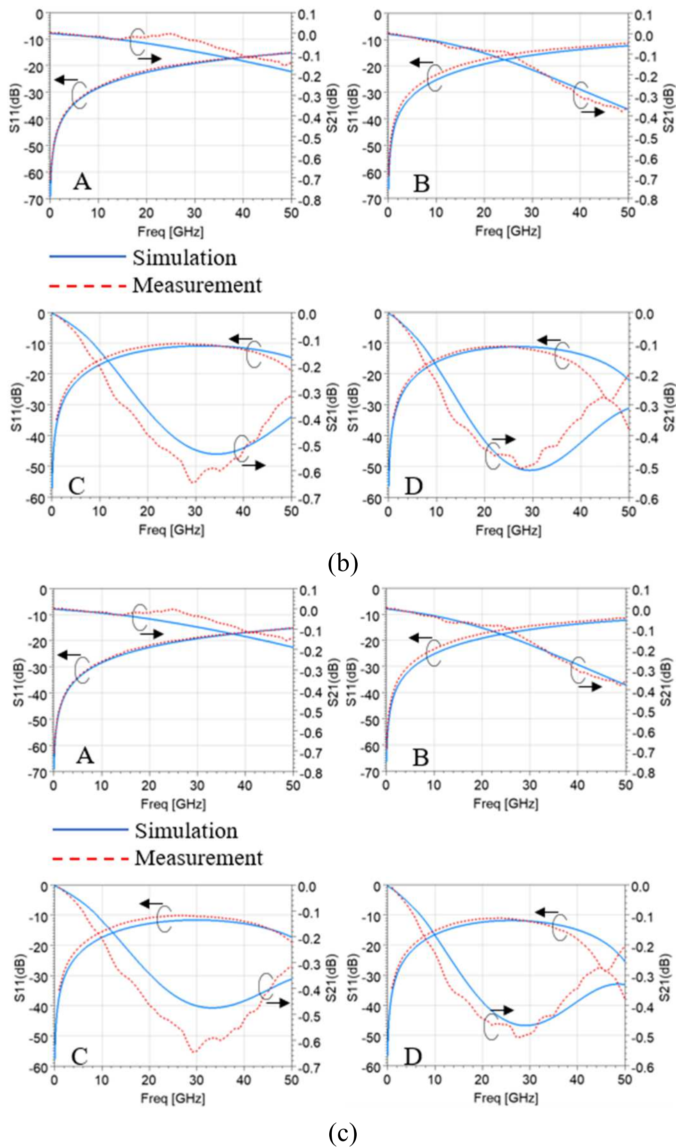
**Measurement Results**

Three sets of de-embedding structures with TMV pitch of 200 µm, 250 µm, 300 µm were fabricated for the verification of the proposed de-embedding method. The measurement was done with Keysight PNA and on-wafer measurement using FormFactor probe station with 100 µm pitch GSG probes. To compare the measured results, 3D full-wave EM simulations were done in HFSS, ANSYS Electronic Desktop 2020 R1.

Fig. 3. below shows the measured S-parameters of three sets de-embedding structures of 200 µm, 250 µm, and 300 µm pitch TMV transitions comparing with the simulated results. The measured results well match the simulations especially for the 200 µm pitch TMV structures. For structure C and D, the insertion loss increases as TMV pitch increase. This could be caused by the higher loss of the fabricated molding compound. Structure D has longer backside TL than structure C. However, the S21 performance of structure D is slightly better structure C. This could be caused by the coupling of the two TMV transitions. The measured S-parameters were then imported into Keysight ADS to apply proposed L-2L de-embedding method to extract the characteristics of the three TMV transitions.




(a)



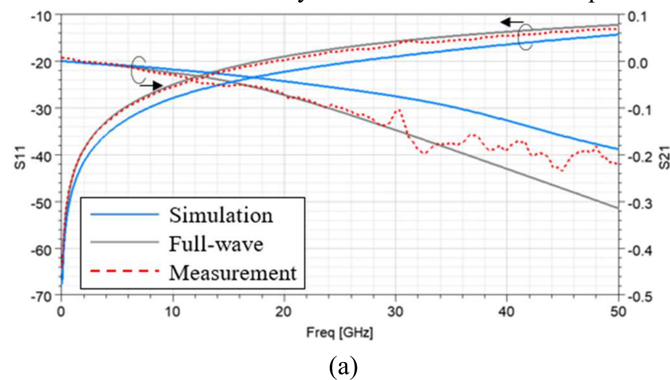

(b)

(c)

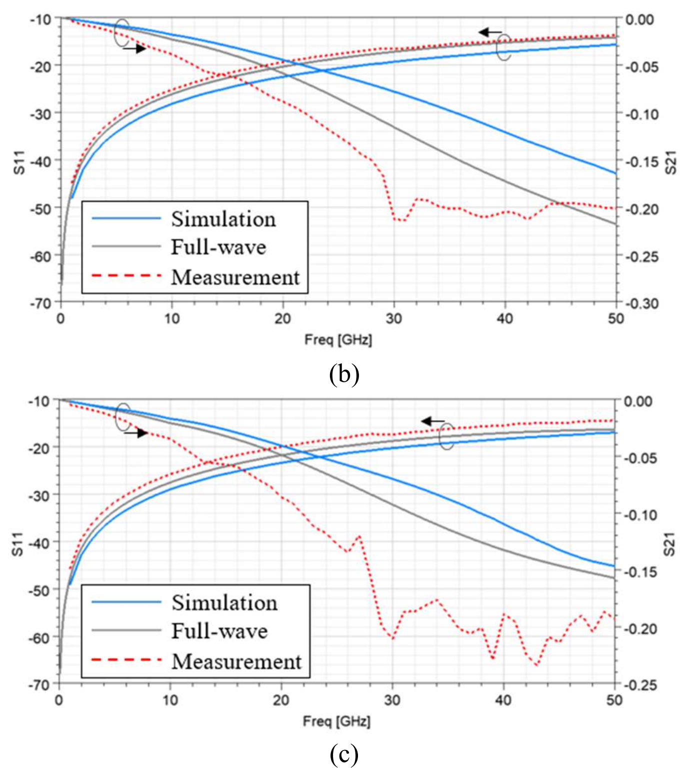
Fig. 3. Measured results of three sets de-embedding structures. (a), (b), (c) are the measurement results of 200 µm, 250 µm, 300 µm TMV de-embedding structures respectively.

## De-embedded Results

Fig. 4. below shows the extracted S-parameters of three TMV transitions with different pitch of 200 µm, 250 µm, and 300 µm. 3D full-wave EM simulations in HFSS of the GSG TMV transition section only are also included for comparison.




(a)




(b)

(c)

Fig. 4. Comparison of extracted S-parameters of TMV transitions from measurement results and simulation results with the 3D full-wave simulation of the TMV transition section only. (a), (b), (c) are for the TMV transition with pitch of 200 µm, 250 µm, 300 µm respectively.

S11 of extracted TMV from both simulation and measurements agrees well with the full-wave TMV transition simulation for all three different pitch TMV transitions. The extracted S21 from measurement has more deviation than simulations for 250 µm and 300 µm pitch TMV than the 200 µm pitch TMV especially at high frequency. This deviation mainly comes from the difference between measurement and simulation in structure C and D.

## Conclusions

In this paper, an extended L-2L de-embedding method to extract the vertical GSG transition TMV from four de-embedding structures are demonstrated. The extracted S-parameters of three sets TMV transitions from measurement and simulation results agrees well with the 3D full-wave EM simulation of the TMV transition. The L-2L de-embedding method for RF characteristics extraction of vertical transitions is validated up to 50GHz.

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