Development of Flip-Chip Packaging for Monolithic Microwave Integrated Circuit

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Abstract

In this paper, the flip chip joints formed by using gold (Au) stud on commercial-off-the shelf (COTS) monolithic microwave integrate circuit (MMIC) designed for wire bond assembly are evaluated. This study demonstrated different interconnect joints starting from chip level with Au stud bumping as main core in these interconnect joints.

Key words: Interposer, flux-less, thermos-compression bonding, Sintering

Introduction

5G demands has generated many topics on packaging method and approached on MMICs devices operating at millimeter wave (mm waves) frequencies. There are also microwave and radio frequency (RF) devices widely used in many applications such as telecommunications, mobile phone, wireless Lan, Bluetooth, radars, satellite communications, and automotive. Gallium Arsenic (GaAs) and Gallium Nitride (GaN) are good candidates to be used as substrate in these devices. Gallium Arsenic substrate is commonly used in commercialized microwave devices with wire bonding interconnects technology. There are a few approaches to package the MMICs devices, where these approaches have its own advantages and weaknesses. However, all the approaches are working to the direction to explore a robust and high-performance module with low loss, low inductance, high thermal dissipation, miniaturize size and high efficiency solutions. These devices can be die attached onto printed circuit board substrate or ceramic substrate with different types of conductive paste, preform and solder paste in conventional way for wire bonding. MMIC device solder attached on Quad-flat-No-Lead (QFN) package for power amplifier module realized in Ka-band by Rasmi Behera et al, reduce of QFN package size minimized the loss in high frequency where additional RF line are avoided [1]. There are some studies which using fan-out wafer level packaging method to assemble GaN device for short and low inductance by Tanjan Braun et al [2]. High resistivity silicon interposer with through silicon via (TSV) are being used to assemble a compact heterogenous integration module for high performance power amplifier, which involved wire bonding and flip chip technologies [3]. In most of the cases, the chips as received are ready diced into chip form and placed in chip tray. To convert the wire bonding interconnect pads into flip chip interconnect pad on microwave devices at chip level, gold stud bumping is an option. Satoru Zama et al. carried out study on flip chip joints on 6mm square area and 1mm thick chip with gold stud bump and copper stud bump on bond pad pitch of 300um, the bonding involved eutectic alloy solder printing on FR4 substrate for the flip chip process. The stud bump on indium lead (InPb) solder, passed 900 cycles thermal shock test [4].

In this paper, the device with wire bond pad were used and Au stud bumps are bonded on the wire bond pad to prepare the interconnect for flip chip process. Stacked bumps are bonded on top chip and single stud bump is bonded at the bottom chip. The stacked gold stud bumps at the signal pads can increase the overall height of the interconnect joints. Between the gold stud bump, there is solder or silver sintered paste. The example of the assembled sample with actual device is shown as figure 1.

Figure 1. Flip chip sample with actual chip.

Experimental Procedures

In the evaluation, two groups of samples were prepared for the study on the flip chip solder joint. First group samples are on gold stud bumping with tin-silver-copper (SAC) solder and second group of samples are on gold stud bumping with silver sintering paste. The main assembly approach for the samples prepared is shown in figure 2.

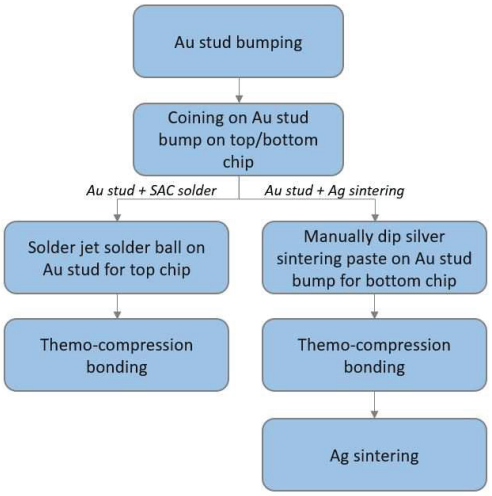
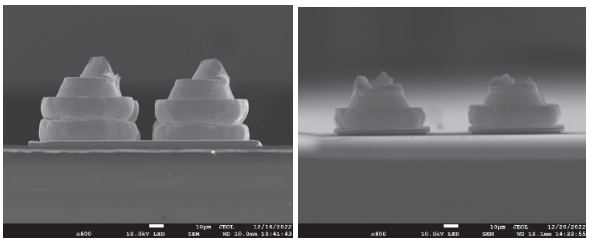


Figure 2. Assembly approach

The top chips that were used in the evaluation are dummy silicon chip with wire bond pads designed. The bond pads

located at one site of the chip with a non-symmetric pad layout as actual functional device. The top chip is about 100um thin with chip size of 2.75mmx2.75mm. The bottom chip was fabricated with high resistant silicon wafer and diced into chip size of 5mmx7mm, with a thickness of 775um. Pad metallurgy for top and bottom chip are the same, both are fabricated with copper nickel gold (3µmCu/2µmNi/0.2µmAu) pad. The bonding of gold stud bumping was using 1.0mil 2N Au wire by thermosonic bonding at chip level, where the chip was heated up at about 150°C at the top plate during stud bumping process. The bonded Au stud bumps are shown as figure 3(a) & 3(b). For the top chip, stacked Au stud bumps were bonded and followed by stud bump coining. Bottom chip was bonded with single stud and then followed by coining process. The coining process provides a flatter surface for the next process. During the coining process, each bumps experience the force of about 37g. The image after coining is shown as figure 4. The sharp tail on the bump is flattened.



(a) (b)

Figure 3. (a) Double stud bump on top chip and (b) single stud bump on bottom chip

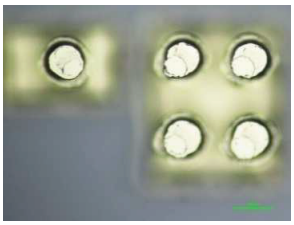
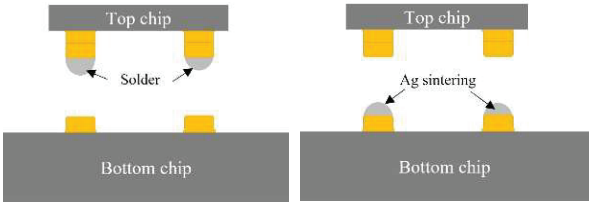


Figure 4. Coining of the stud bump to improve the contact

In flip chip bonding, first group samples have SAC solder at the interconnect joint, where the SAC305 solder ball with diameter of 80µm was jetted on the Au stud bump on the top chip, and perform thermo-compression onto the bottom chip, see figure 5(a). Second group of samples has silver sintering paste at the interconnect joint, where the sintering paste was dipped on the stud bump at the bottom chip and followed by thermo-compression process, see figure 5(b).



(a) (b)

Figure 5. Schematic drawing of sample (a) Au stud bump with SAC solder (b) Au stud bump with Ag sintering paste

SAC solder ball jetting process was set at laser energy of 1ms at 2600mA. Figure 6 shows the scanning electron microscope (SEM) image on wetting of the solder on the stacked bumps. The Ag sintering paste that dipped on individual stud bump of bottom chip is shown in top view image in Figure 7.

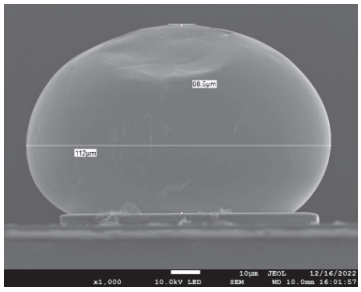


Figure 6. solder ball jetted on stacked bump on top chip

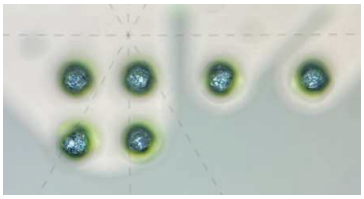
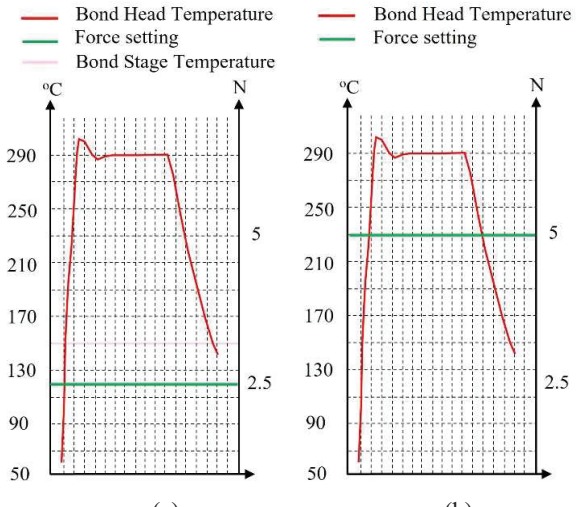


Figure 7. Top view of bottom chip with Ag sintering paste cover on Au stud bump.

The flip chip process used thermo-compression to form the flip chip interconnect for all the samples. During the bonding of interconnect with SAC solder from 1st group samples, bond head was heated up to 290°C peak temperature and constant 150°C at chuck table. For 2nd group's samples where Ag sintering paste was used, the chuck table followed ambient temperature without heating. The bonding profile for both samples group are shown Figure 8(a) & (b).



(a) (b)

Figure 8. Flip Chip bonding profile for interconnect with (1) SAC (b) with Ag sintering paste cover on Au stud bump.

Flipped chip samples with Ag sintering was sintered in the oven at 260ºC for 90 minutes after the thermocompression process. This is to ensure the silver sintering process is complete. After the completion of the main assembly approach, group 1 and group 2 samples were subjected to 150ºC oven cure for 60 hours with nitrogen gas purged. This is to further analyze the joint conditions after the temperature storage.

Results and Discussions

(I) Au stud bump + SAC joints

Sample after thermocompression process were ion milled at the solder joints as shown in figure 9. The solder melted during flip chip process and formed the joint around the Au stud bumps, it can be observed that the top Au stud bump can pierce through the solder and contact with Au stud at the bottom chip. Figure 10 shows the joints after 150ºC curing for 60 hrs. It can be observed that the Au stud on the top chip contact with solder and the bottom is mostly solder is seen and it is at the edge of the interconnection bond pad of bottom chip. There is some misalignment in the themo-compression. This cause ion milling on the unit being could not be located the center of the joints for top and bottom bumps concurrently. Some tiny crack line is observed at the contact surface of the joints to the bond pad of top chip and bottom chip. The bulk of the joint (Au stud + SAC) formation remains good.

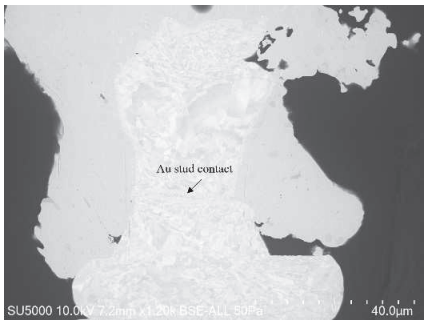


Figure 9. Interconnect joints formed with Au stud bump with SAC solder. (T=0 hour)

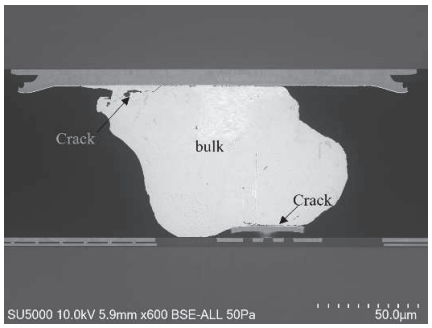


Figure 10. Interconnect joints formed with Au stud bump with SAC solder. (T=60hours)

(II) Au stud bump + Ag sintered joints

The SEM image of the Ag sintered joint after themo-compression and sintered in oven is shown in figure11. It can be observed that at the interconnect joint, a thin layer of Ag sintered layer is formed between Au stud bumps. Better alignment is seen on this unit, and Au stud bumps contacted to the top chip and bottom chip pad. SEM image of the sample with 150ºC temperature storage for 60hours is shown in figure 12. This SEM image on the cross section shows that there is slightly over ion milled from the bumps center. It can be observed that the Ag sintered layer is formed between top and bottom Au stud bumps also. No crack lines seen between Au stud bump and bond pad. There is some porosity is observed at the bulk of the joints (Au stud + Ag)

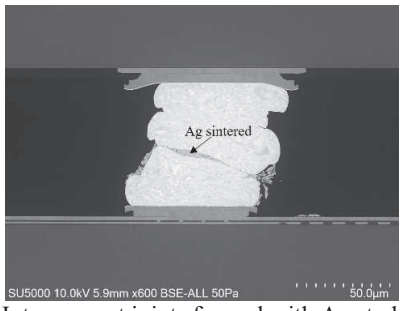


Figure 11. Interconnect joints formed with Au stud bump with Ag sintering paste. (T=0 hour)

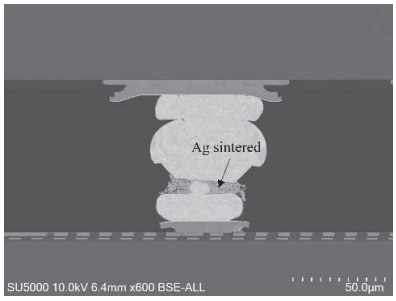


Figure 12. Interconnect joints formed with Au stud bump with Ag sintering paste. (T=60 hours)

(III) Actual chip sample's E-test results

E-test was carried out on samples with actual amplifier device assembled through converting the wire bonding pad to flip chip with Au stud bump and attached onto the bottom chip through flip chip process. The flipped chip module with actual device was then die attached and wire bonded to PCB substrate. After assembled the flip chip module to the PCB, copper heat spreader was attached onto the back of the flip chip. Two types of interface materials were used to attach the copper heat spread. One of the materials is silver epoxy paste and the other one is SAC solder paste. The samples were prepared to the required testing condition as shown in figure 13. A vector network analyzer (VNA) with an output power level of -30 dBm was used for the S parameter test. Figure 14 and figure 15, shows the measured S21 results of the flip chip samples with heat spreader attached. It can be observed that the sample using

the SAC solder paste to attach the heat spreader (figure 14) has higher S21 comparing to that using the sample using silver epoxy (figure 15) due to the improved thermal interface.

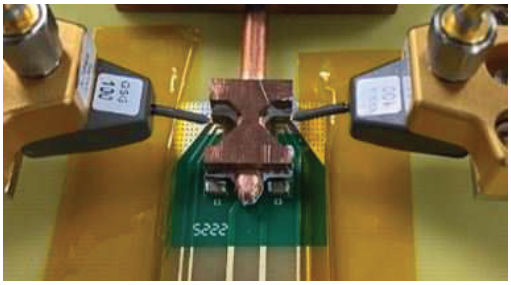


Figure 13. Testing on the flip chip sample

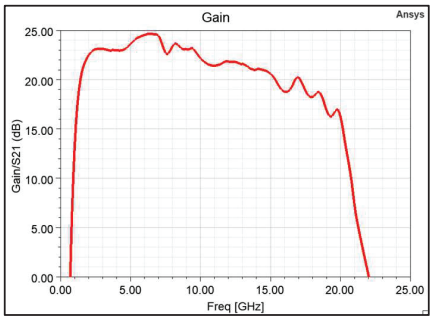


Figure 14. Measured S21 on sample with heat spreader attached (interface material SAC solder).

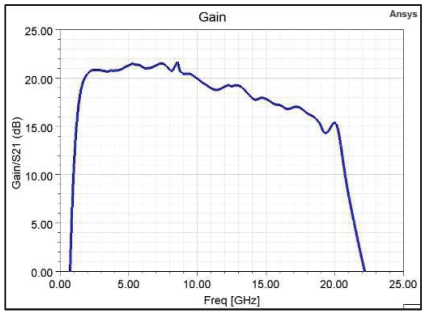


Figure 15. Measured S21 on sample with heat spreader attached (interface material silver epoxy).

Conclusions

The flip chip bonding with interconnect (i) Au stud bump + SAC as well as (ii) Au stud bump + Ag sintering, were demonstrated and applied on the actual amplifier devices. The work of this study is summarized as below:

(i) Au stud + SAC interconnect has good formation at the bulk area of the flip chip interconnect joint.

(ii) There are tiny crack lines as observed between the interconnect and top & bottom chip's pad for Au stud + SAC interconnect after temperature storage at 150ºC for 60 hours.

(iii) A layer of Ag sintering is observed at the Au stud + Ag sintering flip chip interconnect.

(iv) Sample using the SAC solder paste to attach the heat spreader has higher S21 comparing to that using the sample using silver epoxy.

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