Wafer-Scale Monolayer MoS_2 with Tunable Grain Size via Grain Boundary Engineering for Neuromorphic Computing

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Abstract

Grain boundaries (GBs) in two-dimensional (2D) materials, once regarded as detrimental defects, are now increasingly recognized as functional features for tailoring material properties. Here, we report a grain-boundary engineering strategy based on a diameter-tunable chemical vapor deposition (DT-CVD) technique, enabling the wafer-scale growth of monolayer MoS_2 with controlled grain sizes. Systematic tuning of GB density is achieved by adjusting the inner quartz tube diameter, while maintaining uniform monolayer morphology and crystallinity. Structural and spectroscopic characterizations confirm that increasing GB density introduces shallow energy barrier and band bending effects, which are exploited in memtransistor architectures to induce tunable analog switching. Simulations and electrical measurements show that grain-boundary-induced charge trapping and ionic migration synergistically govern the observed resistive switching behavior. Among all devices, the grain size-tunable MoS_2 memtransistor with an equivalent grain size of ~114 ± 48 nm achieves an optimal trade-off between analog precision and cycling endurance. It supports 64-level conductance modulation along with robust long-term synaptic plasticity. When implemented in neural networks, it delivers high training and inference accuracy across diverse datasets, underscoring its promise for next-generation energy-efficient neuromorphic systems.

Keywords: Grain-size tunability, Wafer-scale monolayer MoS_2, Grain boundary engineering, Memtransistors, Neuromorphic network computing

1. Introduction

Two-dimensional (2D) materials are promising for next-generation electronics and quantum technologies due to their atomic thickness and highly tunable physical properties.[1] To fully exploit their intrinsic characteristics, which often rely on atomically perfect crystalline lattices, considerable research has long focused on minimizing structural defects through the development of advanced synthesis and integration techniques.[2, 3] Among various types of defects, grain boundaries (GBs) that naturally form during growth when misoriented crystal domains merge have traditionally been regarded as detrimental, as they disrupt lattice continuity and degrade electrical or optical properties.[4] However, emerging research has begun to challenge this conventional perception, revealing that GBs are not merely imperfections to be eliminated. On the contrary, when precisely engineered, GBs can act as functional design that locally tailor material properties and introduce novel functionalities, thereby significantly expanding the application potential of 2D materials.[5]

In transition metal dichalcogenides (TMDCs), GBs have been shown to enable diverse functionalities ranging from charge modulation to catalytic activity.[6-8] For example, GB-induced structural defects provide abundant active sites for ion adsorption, thereby enhancing the sensitivity of 2D material-based sensors.[9, 10] The 2D molybdenum disulfide (MoS_2) memristor utilizing GBs regulation mechanism has successfully achieved gate-tunable artificial synapses and neural network functionalities.[11, 12] From a catalytic perspective, GBs are frequently identified as highly active regions, playing a key role in promoting hydrogen evolution reactions and facilitating carbon capture.[13, 14] The nanoscale pores formed at GBs in MoS_2 can selectively block larger hydrated ions while allowing water molecules to pass through, demonstrating exceptional ion selectivity and water permeability, as reported in a very recent study.[15] Moreover, biocompatible TMDCs has been used in implantable biosensors, where its biodegradability in physiological fluids often initiates at GBs and associated point defects.[16] These examples illustrate that GBs, far from being mere flaws, offer a rich toolbox for advancing both fundamental science and practical applications of 2D materials.

Despite these advances, grain-boundary engineering in 2D materials remains at an early stage, with limited progress in deterministic control at wafer scale.[17-19] Post-treatment strategies, such as plasma exposure, ion/electron irradiation, and high-temperature annealing, have been reported for introducing nanopores and defects, but they often face inherent limitations in precision and scalability for controlling and atomic configuration, with the additional risk of introducing doping contamination.[20-22] In contrast, controlling nucleation density and orientation during chemical vapor deposition (CVD) offers a pathway to intrinsically tune GB structures. However, CVD growth involves coupled processes of precursor decomposition, adsorption, and atomic migration, making it challenging to precisely regulate GB density.[23, 24] Achieving scalable

synthesis strategies that deterministically engineer GBs remains a key bottleneck.

Here, we report a diameter-tunable CVD (DT-CVD) strategy that enables wafer-scale growth of monolayer MoS_2 with systematically tunable grain sizes. By adjusting the inner tube diameter to regulate gas flow and nucleation density, we reproducibly synthesize grain-size-tunable MoS_2 (GST-MoS_2) while maintaining uniform morphology and crystallinity. Structural and spectroscopic characterizations reveal that increasing GB density introduces shallow trap states and band bending. When integrated into memtransistors, these effects give rise to tunable hysteresis and resistive switching governed by the mechanism of coupled charge trapping and ionic migration. Devices based on GST-MoS_2 exhibit multilevel conductance modulation, robust long-term synaptic plasticity, and high accuracy in neural network simulations, underscoring grain-boundary engineering as a scalable route to multifunctional 2D electronic and neuromorphic systems.

2. Results and Discussion

2.1 DT-CVD system design and GST-MoS_2 growth

Figure 1a presents a schematic illustration of the improved DT-CVD system, which retains the common dual-zone configuration but incorporates a diameter-tunable inner quartz tube, held at both ends by perfluoro elastomer O-rings, nested within a fixed outer tube. Originally designed to accommodate substrates of varying sizes, this geometry was unexpectedly found to provide precise control over the grain size of wafer-scale MoS_2 monolayers. In a typical process, quarter-cut 2-inch sapphire wafers were annealed at 1050 °C in air for surface cleaning, followed by growth at 740 °C by using MoO_3 and sulfur powders as precursors. A Ni foam interlayer was introduced to filter impurities and transform the precursor vapor from a point source to a planar source. A detailed description of the DT-CVD system, along with an enlarged schematic of the reaction chamber and experimental growth parameters, are provided in the experimental section and supporting information (**Figure S1 and S2**).

Atomic force microscopy (AFM) imaging confirmed the formation of continuous polycrystalline MoS_2 monolayer with excellent surface flatness (**Figure 2b-e**). By tuning the inner tube diameter (110, 100, 85, and 70 mm), four representative GST-MoS_2 films (GST-MoS_2-1 to GST-MoS_2-4) were obtained. These films exhibited ultralow root-mean-square roughness values of 0.18, 0.16, 0.17, and 0.24 nm, respectively, sufficiently smooth to resolve the atomic terraces of the c-plane sapphire. Since GBs are prone to oxidation in ambient conditions, AFM images were further revealed clear signatures of GBs, with a negligible height modulation of ~1 Å (**Figure S3**), consistent with their nature as structural rather than morphological defects.[25]

Photoluminescence (PL) and Raman spectroscopy exhibited characteristic peaks of the MoS_2 monolayer, which revealed systematic spectral shifts with decreasing grain size (**Figure**

1f-g). Specifically, the PL peak of monolayer MoS_2 exhibited a blue shift from 1.870 eV of GST-MoS_2-1 to 1.885 eV of GST-MoS_2-4, corresponding to an energy shift of approximately 15 meV. This shift is consistent with previous reports on 2D systems, where the transition from charged excitons to neutral free excitons occurs due to carrier depletion and localization at defect sites.[26] As shown in the raw (non-normalized) PL spectra in **Figure S4**, the overall PL intensity decreases with smaller grain size, consistent with the higher defect density and enhanced nonradiative recombination at grain boundaries. Raman spectroscopy further confirmed the grain size-dependent variations. The frequency difference between the out-of-plane A_{1g} mode and the in-plane E_{2g} mode increased from 19.9 cm^{-1} to 21.5 cm^{-1}, reflecting enhanced GB-induced lattice strain and defect density. The enhanced asymmetry in the Raman spectra suggests increased influence on in-plane vibrational modes, likely due to defect-induced strain and lattice distortions.

The atomic configuration of MoS_2 grains and GBs was directly examined by high-resolution transmission electron microscopy (HRTEM) and selected-area electron diffraction (SAED) (**Figure 1h–j**). The HRTEM image shows crystalline domains with the expected hexagonal lattice, while SAED from individual grain confirms their sixfold symmetry. In contrast, diffraction patterns taken across GBs reveal orientation mismatches characteristic of polycrystalline films. Structural analysis identified dislocation cores (5|7 rings) and high-angle misorientations as the dominant GB motifs, consistent with previous reports.[27] These results collectively confirm that the DT-CVD approach enables deterministic control of grain size and associated GB density in wafer-scale MoS_2 monolayers.

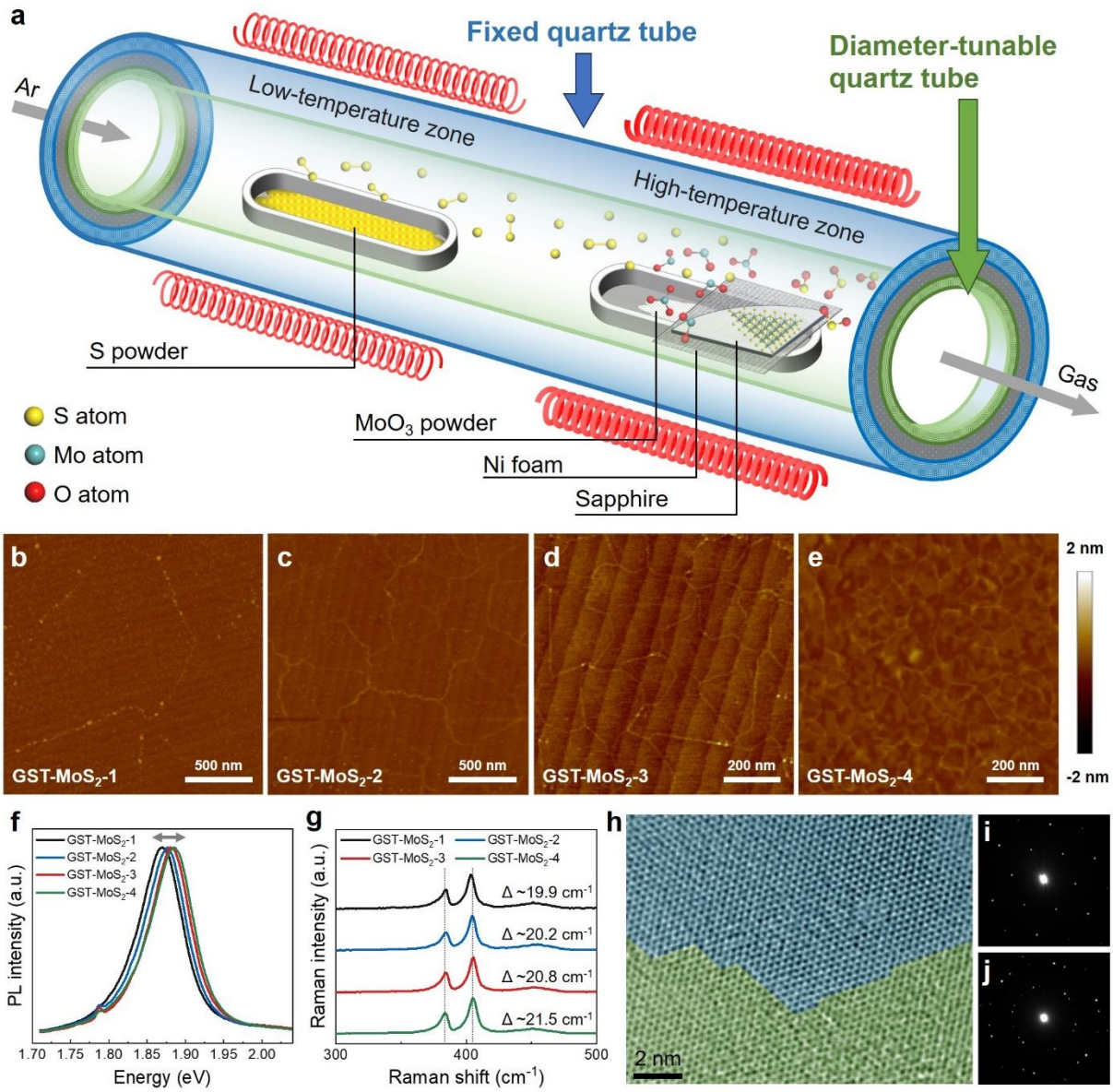


Figure 1. Growth and structural characterization of GST-MoS_2 monolayer synthesized by the DT-CVD technique. (a) Schematic illustration of the DT-CVD system for the growth of GST-MoS_2 monolayer with MoO_3 and S powders as precursors, incorporating a diameter-tunable inner quartz tube nested within a fixed outer tube. (b–e) AFM height images of GST-MoS_2 monolayer grown under different inner tube diameters: 110 mm (GST-MoS_2-1), 100 mm (GST-MoS_2-2), 85 mm (GST-MoS_2-3), and 70 mm (GST-MoS_2-4), showing a gradual increase in GB density. (f) PL spectra of GST-MoS_2 monolayer, displaying slight blueshift and intensity variation with increasing GB density. (g) Raman spectra of the four samples, showing increasing peak separations (Δ) between E_{2g} and A_{1g} modes, indicative of enhanced GB effects. (h) False-color high-resolution TEM image of MoS_2 domain (blue) and GB (yellow). (i, j) SAED patterns acquired from grain (i) and GB (j) shown in (h), confirming the crystalline orientation mismatch between adjacent domains.

The growth of monolayer MoS_2 initiates with rapid nucleation, producing well-defined triangular domains, which subsequently undergo lateral expansion until the film reaches full surface coverage (**Figure 2a-d**). Upon coalescence, grains merge into irregular polygonal shapes along the GBs. To quantify grain size evolution, we introduce the equivalent side length (L_{eq})

based on statistical analysis of AFM images defined as

$$L_{\mathrm{eq}} = \sqrt{\mathrm{Grain\ Area}} \tag{1}$$

To evaluate reproducibility, GST-MoS_2 films were synthesized using inner quartz tube diameters of 110, 100, 85, and 70 mm, each repeated four times. AFM characterization from multiple regions (**Figure S5–S8**) confirmed highly consistent grain sizes and GB densities. The coefficient of variation (CV) for grain size across GST-MoS_2-1 to GST-MoS_2-4 was 12.9%, 19.3%, 18.2%, and 19.2%, respectively, underscoring the robustness of the DT-CVD process for wafer-scale growth.

This reproducibility enabled a systematic study of growth kinetics by tracking grain evolution under different gas flow conditions. Gas flow simulations (**Figure S9**) reveal a near-linear increase in flow rate as the tube diameter decreases. In contrast, L_{eq} exhibits a logarithmic dependence on flow rate to achieve full surface coverage **(Figure 2e**). Time-dependent AFM analysis (**Figure 2f** and **Figure S10**) shows that L_{eq} increases almost linearly with growth time, consistent with a steady lateral expansion mechanism. Although the absolute growth rates vary with tube diameter, as higher flow rates (smaller diameters) yield slower L_{eq} growth. Notably, despite the pronounced differences in grain size, the surface coverage progresses in a nearly identical manner across all tube diameters. This behavior suggests that, under fixed precursor ratio, temperature, and pressure, the lateral diffusion-driven expansion of MoS_2 grains is largely independent of gas flow. Instead, gas flow primarily regulates the nucleation density, leading to grain-size variation without altering the monolayer continuity. As illustrated in Figure S1, the material grows on the top surface of the sapphire substrate, ensuring stable precursor delivery and preventing the formation of bilayer regions even at elevated flow rates. These findings challenge the conventional notion that flow directly governs lateral growth kinetics.

To further investigate the influence of gas flow on nucleation behavior, the statistical analysis of the grain nucleation density (GND) of MoS_2 under various tube diameters and growth durations was performed:

$$\mathrm{GND} = \frac{1}{\mathrm{Grain\ Area}} = \frac{1}{{L_{\mathrm{eq}}}^2} \tag{2}$$

The results reveal that higher flow rates, corresponding to smaller inner tube diameters, promote rapid nucleation, leading to a high density of small grains. In contrast, lower flow rates (larger tube diameters) suppress nucleation, resulting in fewer but significantly larger grains (**Figure 2g**). Additionally, the observed decrease in GND over growth time can be attributed to Ostwald ripening, in which smaller grains are gradually consumed by larger ones. Interestingly, despite variations in growth time, the maximum difference in GND between different tube diameters consistently remains within a range of 10- to 18-fold, showing little dependence on growth duration. It is speculated that the observed growth behavior is closely related to the

unique reactor geometry employed in our process, wherein a Ni foam is placed between the growth substrate and the crucible containing MoO_3 precursor powders (**Figure S1**). While the initial purpose of this design was to filter impurities and to convert the precursor vapor distribution from a point source to a planar one, it was unexpectedly found that the Ni foam also serves as an effective sulfur trap. Consequently, MoS_2 formation is suppressed on the bottom surface due to sulfur deficiency, whereas growth proceeds exclusively on the top surface of the substrate. The MoO_x precursor molecules reach this upper surface via gas-phase diffusion, circumventing the substrate edges from within the crucible. This mechanism differs fundamentally from conventional CVD growth. At higher flow rates, the elevated sulfur concentration near the substrate surface promotes rapid nucleation, but the concurrent hindrance of MoO_x diffusion lowers the precursor concentration at the growth interface. The reduced Mo supply slows the lateral expansion of the nuclei after their initial formation. This explains why samples with higher nucleation densities and those with lower nucleation densities exhibit nearly identical surface coverage at the same growth duration (**Figure 2f**). The delayed coalescence process further suppresses the formation of secondary layer domains or overgrown grains.

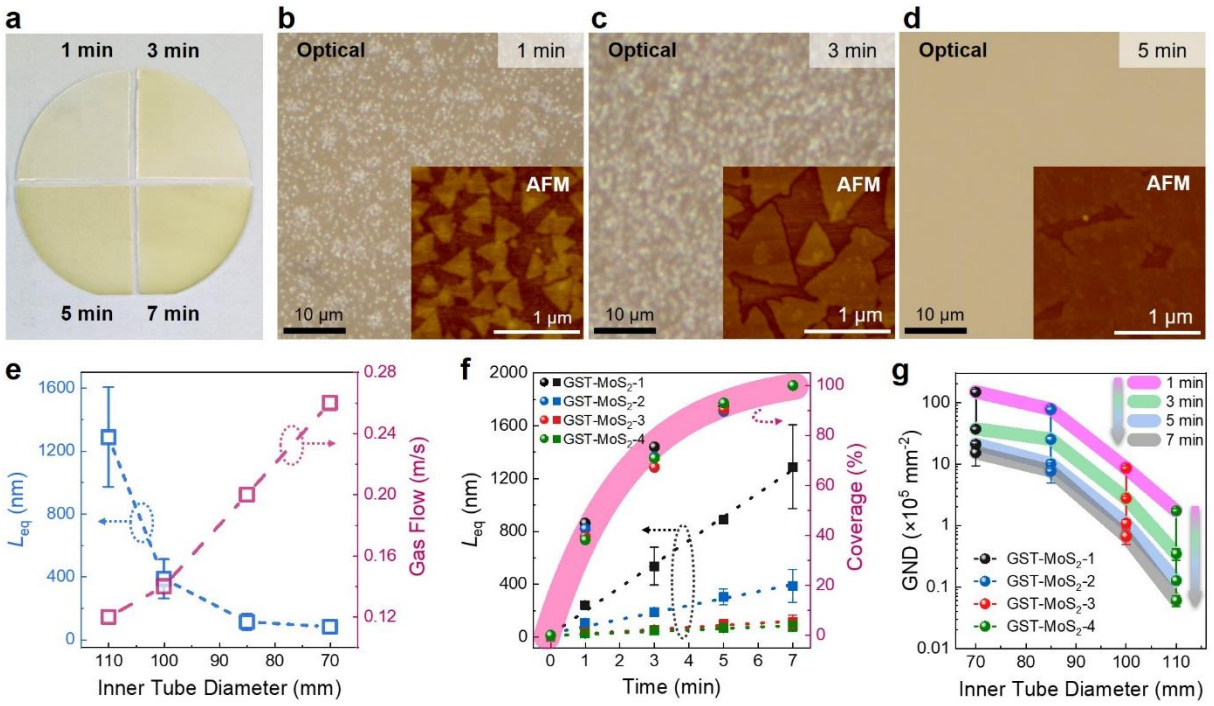


Figure 2. Kinetics analysis of GST-MoS_2 growth. (a) Optical images showing the time-dependent evolution of GST-MoS_2 films on sapphire substrates at growth durations of 1, 3, 5, and 7 min. (b–d) Optical and AFM images of GST-MoS_2-1 films grown for 1, 3, and 5 min, highlighting the merging process originating from well-defined triangular grains. (e) Variation of equivalent grain side length (L_{eq}) and gas flow rate with inner quartz tube diameter. (f) Evolution of L_{eq} and surface coverage as a function of growth time under different gas flow. (g) GND as a function of inner quartz tube diameter at different growth durations.

2.2 GB-regulated memtransistor performance

In polycrystalline monolayer MoS_2, GBs serve as one-dimensional topological defects that locally disrupt atomic and electronic structures, introducing inhomogeneities that significantly impact charge transport.[28] To directly probe their influence, AFM topography (**Figure 3a**), Kelvin probe force microscopy (KPFM, **Figure 3b**), and phase mapping (**Figure S11**) were performed on the same GBs region. Line scan analysis (**Figure 3c**) reveals a contact potential difference (CPD) drop of 16-18 mV across GBs compared to grain surfaces, accompanied by a step height of ~0.15 nm. This local reduction in surface potential gives rise to an energy barrier for electrons at the GB, where Fermi-level pinning causing electron trapping and the formation of a depletion region around the GB, thereby establishing a local potential barrier (**Figure 3d**). [27] The increased density of such depletion regions can further perturb the local Coulombic environment of Mo atoms, which may contribute to the larger E_{2g}-A_{1g} Raman peak separation observed in high-GB-density samples (**Figure 1g**).[29]

Beyond static band alignment, dynamic processes at GBs also play a crucial role in device operation. Prior studies suggest that the resistive switching (RS) behavior in polycrystalline MoS_2 arises from GB-mediated sulfur vacancy migration, where the reduced diffusion barrier along GBs accelerates ionic transport.[11, 21] Consistent with this, our observations support a diffusion–trapping hybrid mechanism, in which GBs simultaneously act as (i) preferential diffusion pathways for ionic species and (ii) shallow defect sites that trap charge carriers and form localized energy barriers.[30] Field-induced vacancy generation and recombination further redistribute trap states near GBs and contacts, leading to local charging effects and the formation of partially depletion region along the GBs.[31] Under high lateral fields, this interplay can give rise to trap-filled space-charge-limited current (SCLC), a conduction mode widely reported in RRAM and neuromorphic devices, driven by trap centers.[32] At higher GB densities, the cumulative effect of additional energy barriers and enhanced diffusion pathways amplifies field-driven charge trapping and ionic migration, thereby widening hysteresis windows and improving ON/OFF ratios. Taken together, these findings highlight that deliberate tuning of grain size and GB density provides an effective handle to couple ionic dynamics with interfacial charge trapping, thereby enabling systematic modulation of resistive switching and synaptic behavior in monolayer MoS_2 neuromorphic transistors.

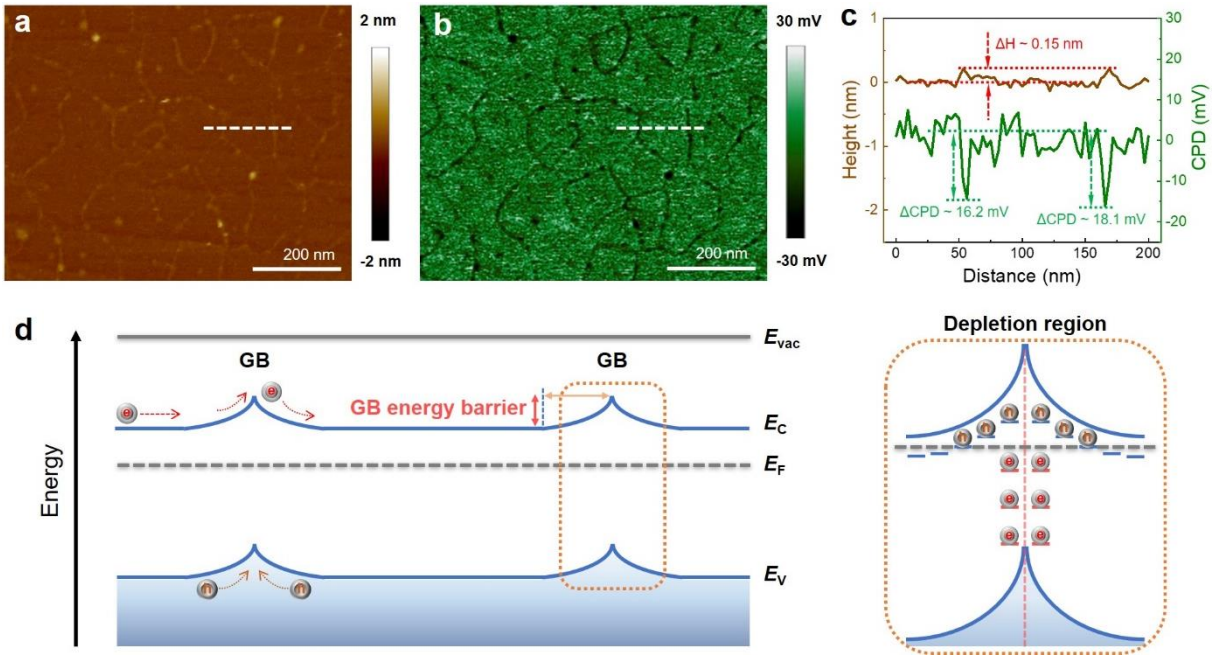


Figure 3. GB-induced mechanisms in GST-MoS_2 memtransistors. (a) AFM height image and (b) KPFM surface potential mapping of GST-MoS_2 acquired over the same region. (c) Height and CPD profiles along the white dashed line in (a) and (b), indicating an elevation of ~0.15 nm and a surface potential drop of ~16-18 mV at the GBs. (d) Schematic band alignment of grain and GB regions. The GBs introduce local energy barriers and depletion region, leading to band bending relative to the grain regions. E_C, E_F and E_V denote the conduction band minimum, Fermi level, and valence band maximum, respectively.

To further investigate the GB-induced hysteresis behavior, we employed Silvaco Technology Computer-Aided Design (TCAD) simulation, which is widely adopted for 2D materials, to construct monolayer MoS_2 transistors and simulate their electronic performance.[33] The device structures were built in the Victory Mesh module, incorporating the Heiman-Warfield model to describe depth-dependent trap cross-sections (**Figure 4a–d**). Key parameters associated with interfacial GBs were defined based on AFM characterizations. The fixed interfacial charge density was varied in the range of 6×10^{12} to 1.3×10^{13} cm^{-2}, while the Gaussian-shaped donor-like trap states (3×10^{13} to 3×10^{14} cm^{-2} eV^{-1}) were introduced as the primary source of hysteresis. Structural relaxation effects were also taken into account during the simulations. Subsequently, current-voltage (I–V) curves were simulated using the Victory Device module, with a voltage step of 0.1 V and a time interval of 0.01 s (**Figure 4e–h**). The simulation results showed that as the grain size decreased, the hysteresis window gradually widened, while the on-state current decreased. These findings attribute the hysteresis primarily to the delayed response of interfacial traps with different time constants.

Experimentally, an array of eight top-gated GST-MoS_2 memtransistors (**Figure S12**) were fabricated directly on sapphire without transfer to ensure statistical reliability. All devices with the channel length of 1 μm displayed bipolar analog resistive switching under closed-loop V_{DS}

sweeps from ±7 V to ±10 V at V_G = 0 V (**Figure 4i-l**). Devices switched reversibly between high-resistance state (HRS) and low-resistance state (LRS), with switching ratios (R_{HRS}/R_{LRS} at V_{DS} = 1 V) increasing markedly with sweep range (**Figure 4m** and **Figure S13**). This behavior aligns well with simulation trends, where devices with smaller grain sizes exhibited denser GBs and consequently wider hysteresis windows. Among them, the GST-MoS_2-3 and GST-MoS_2-4 devices exhibited R_{HRS}/R_{LRS} increasing from 21 and 143 at ±7 V to approximately 302 and 2142 at ±10 V, respectively, highlighting the effectiveness of GB engineering in modulating memtransistor behavior.

Compared to the experimental results, TCAD simulations offered useful insights into the hysteresis trends by considering grain-boundary-induced shallow trapping effects; however, they did not incorporate dynamic ionic diffusion processes. In practice, sulfur vacancy migration plays a critical role in modulating local defect densities near GBs, particularly under high electric fields where the diffusion barrier is lowered.[21] As a result, the device current decreases only slightly with increasing GB density, less than predicted by the static simulation model, which further supports that GBs behave differently from isolated point defects. To gain deeper insight into the underlying conduction mechanisms, further conduction analysis by using GST-MoS_2-3 (**Figure 4n**) and GST-MoS_2-2 (**Figure S14**) as representative samples showed that the LRS follows a ln(I_{DS}) vs ln(V_{DS}) slope of ~2.2, indicative of SCLC mechanism, while the observed linear relation of ln(I_{DS}) with $V_D^{1/2}$ in the HRS clearly reveals its Schottky emission nature.[21] These results corroborate a diffusion-trapping hybrid mechanism as the origin of resistive switching, rather than filamentary conduction. More precisely, at the HRS, current transport is initially governed by carrier injection over the reverse-biased Schottky barrier at the source (or drain) contact. With increasing V_{DS}, positively charged sulfur vacancies (V_S^+) migrate dynamically along grain boundaries toward the source contact, leading to an increase in local dopant concentration within its depletion region. This increase reduces the effective barrier height due to enhanced image-force lowering, which enables higher current injection. This transition drives the switching from HRS to LRS.[12] In the LRS, current transport is constrained by electron traversal across GB barriers and trapping/de-trapping at GB-associated traps states. This explains both the SCLC behavior and the observed decrease in LRS current with increasing GB density.

Endurance measurements (**Figure 4o**, **Figure S15**) confirmed that GST-MoS_2-2 and GST-MoS_2-3 devices maintained stable HRS/LRS states over 100 cycles at ±10 V, with switching ratios of ~100 and ~270, respectively. In contrast, GST-MoS_2-4 device could only sustain stable cycling under ±7 V, but failed after the 6th cycle under ±10 V sweeps (**Figure S16**), likely due to excessive GB density enhancing local field concentration and accelerating defect migration or breakdown near the GBs. Retention measurements (**Figure S17**) further confirmed stable

resistive states over 2400 s, consistent with reliable nonvolatile behavior. Collectively, GST-MoS_2-3 devices strike the optimal balance between resistance tunability and cycling stability, making it the most promising candidate for practical memtransistor applications.

Beyond the two-terminal behavior, the planar GST-MoS_2 devices also exhibited gate-tunable memtransistor characteristics. As illustrated in **Figure 4p** and **Figure S18**, the I_{DS}-V_{DS} response showed strong dependence on the gate voltage (V_G = -2 V to +3 V). Notably, the GST-MoS_2-3 device exhibited a tunable resistance switching ratio (R_{HRS}/R_{LRS}) ranging from ~76 at V_G = –2 V to ~18 at V_G = 3 V, demonstrating its potential for multilevel analog memory and neuromorphic computing applications. In addition, hysteresis properties were also observed in the transfer characteristics of all GST-MoS_2 memtransistors (**Figure S19**). Previous reports have attributed such hysteresis to factors including gas adsorption, interface trapping, and dielectric defects.[34, 35] However, in our vacuum measurements (1×10^{-5} mbar), the large hysteresis persisted, ruling out surface adsorption as the primary cause. Instead, the dominant factor is attributed to the intrinsic GB-induced defects in the MoS_2 channel and their coupling with charge traps in the HfO_x dielectric layer. Simulations incorporating different grain sizes support this hypothesis, with hysteresis increasing as grain size decreases, which is consistent with experimental trends.

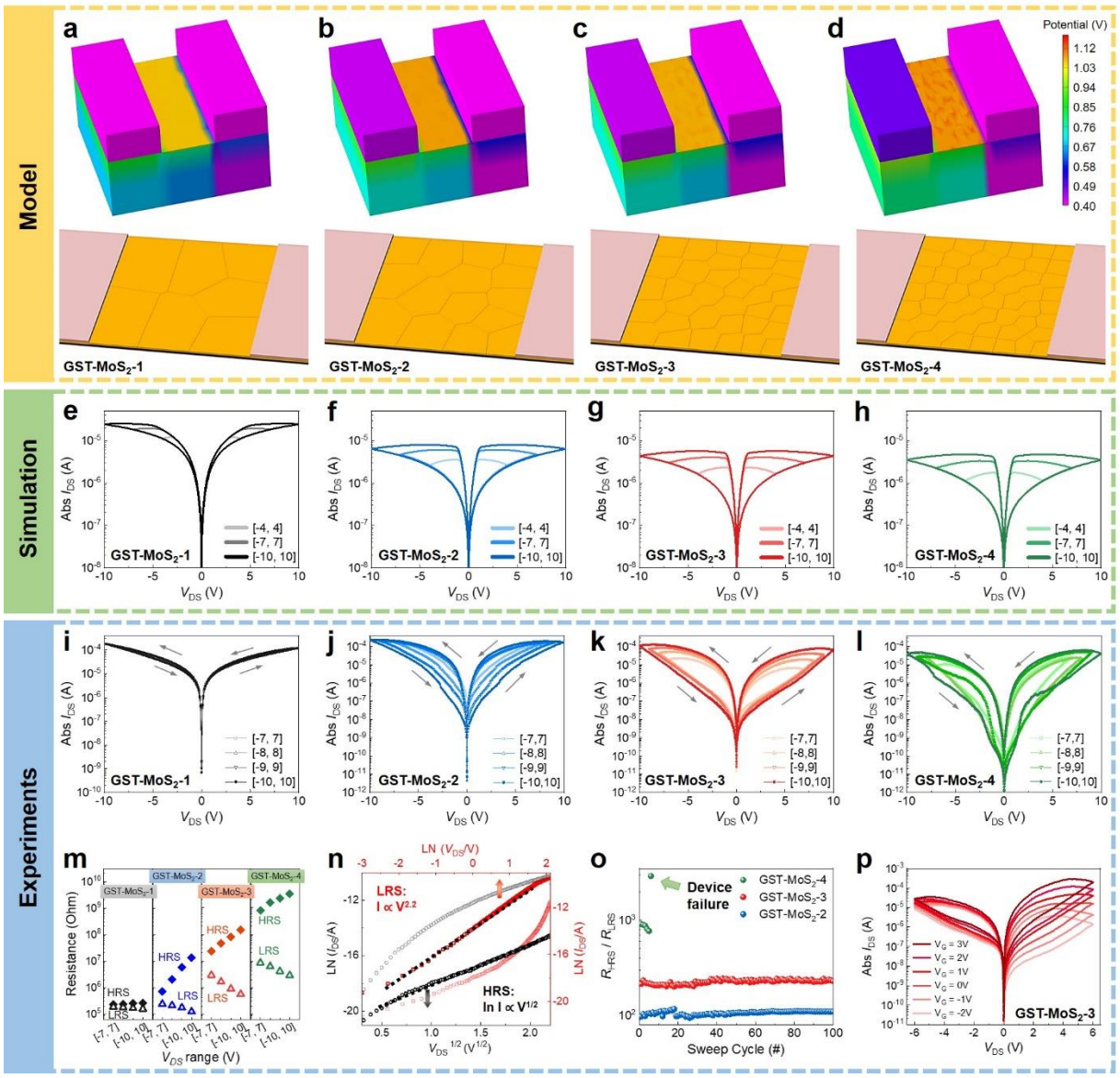


Figure 4. 3D structural modeling, device simulations, and experimental measurements of memtransistor devices based on GST-MoS_2 with varying GB densities. (a-d) 3D structural models and channel potential profile of memtransistors based on GST-MoS_2-1 to GST-MoS_2-4, respectively. Insets show corresponding GB configurations in the channel region, with increasing GB densities from (a) to (d). (e-h) Simulated I_{DS}-V_{DS} hysteresis loops for the models in (a-d), reproducing the experimentally observed trend of enlarged hysteresis and enhanced current modulation with higher GB density. (i-l) Experimental I_{DS}-V_{DS} hysteresis characteristics of devices with different GB density measured at $V_G = 0$ V. Devices with higher GB density exhibit broader hysteresis windows and higher on/off ratios. Gray arrows indicate V_{DS} sweep directions. (m) Extracted HRS and LRS values at V_{DS} = 1 V under different V_{DS} sweep ranges and GB density. (n) I_{DS}-V_{DS} curve fitting for GST-MoS_2-3. (o) R_{HRS}/R_{LRS} evolution over 100 consecutive sweep cycles between V_{DS} = ±10 V. GST-MoS_2-2 and GST-MoS_2-3 show stable performance, whereas GST-MoS_2-4 fails after the 6th cycle. (p) Gate-tunable behavior of the GST-MoS_2-3 memtransistor at varying gate potentials from −2 to 3 V in 1 V steps.

2.3 GB-engineered MoS_2 for neuromorphic computing

Biological synapses, the fundamental units of brain function, transmit action potentials

between neurons through neurotransmitter release and exhibit the essential capability of regulating and maintaining synaptic weights. Inspired by these mechanisms, neuromorphic electronics have emerged as a promising paradigm for energy-efficient computing, particularly for artificial intelligence (AI), where conventional architectures are limited by energy-intensive vector–matrix multiplications and frequent memory access.[36-38] By emulating synaptic integration of sensing, memory, and computation, such systems can minimize data movement and accelerate learning. To probe short-term synaptic plasticity, paired-pulse facilitation (PPF) protocols were applied by delivering two successive excitatory pulses with varying time intervals (Δt = 0.01-1 ms). As shown in **Figure 5a**, the device exhibits an exponential decay in facilitation index, indicative of volatile behavior analogous to biological synapses.

The analog switching capability was assessed through quasi-static d.c. measurements following dynamic pulse programming. As shown in **Figure 5b**, the GST-MoS_2-3 memtransistor exhibits well-resolved, linearly distributed conductance states with at least 64 programmable levels. The linearity and robustness of these states enable precise dot-product operations, which are essential for in-memory vector–matrix multiplication in neuromorphic hardware. Long-term synaptic plasticity was further compared across devices with varying GB densities. As shown in **Figure 5c**, all GST-MoS_2 memtransistors exhibit stable and symmetric long-term potentiation (LTP) and depression (LTD) under asymmetric pulsed stimuli. Notably, the conductance range (G_{max}/G_{min}) narrows with decreasing GB density (**Figure S20**), demonstrating that higher GB density enhances the availability of analog states and improves noise tolerance in synaptic operation.

The neuromorphic applicability of GST-MoS_2 memtransistors was further validated by artificial neural network (ANN) simulations using CrossSim.[39] As illustrated in **Figures 5d-e**, a three-layer ANN was constructed, with synaptic weights mapped directly to memtransistor conductance states within a simulated crossbar array. Training was performed on three benchmark datasets: (i) an 8×8 Optical Recognition of Handwritten Digits dataset, (ii) the 28×28 MNIST dataset, and (iii) a cybersecurity dataset from Sandia National Laboratories, with hidden layers of 36, 300, and 512 neurons, respectively. As shown in **Figures 5f–h** and **Figure S21**, devices with higher GB densities (GST-MoS_2-3 and GST-MoS_2-4) consistently demonstrate superior training and inference accuracy, exceeding 92% across all datasets (**Figure S22**), underscoring the critical role of analog tunability and multilevel conductance states in neuromorphic learning. Among them, the monolayer GST-MoS_2-3 memtransistor offers an optimal trade-off between analog performance and cycling endurance, delivering robust short- and long-term plasticity, fine-grained conductance modulation, and high classification accuracy in hardware neural networks. These attributes collectively highlight GB engineering as a scalable route toward high-precision and energy-efficient neuromorphic computing systems.

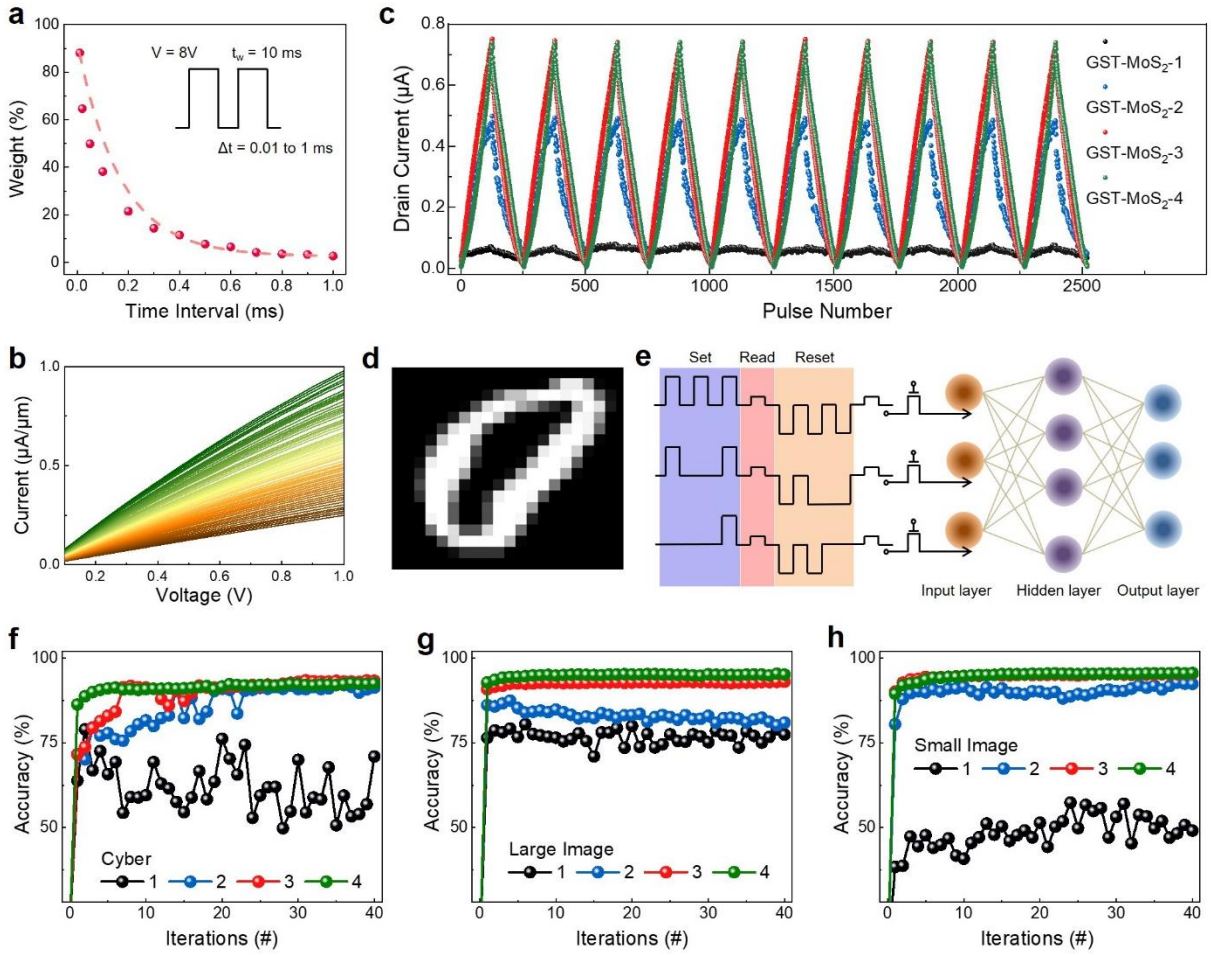


Figure 5. Synaptic characteristics and neural network simulations of GST-MoS_2 memtransistors with varying GB densities. (a) The PPF behavior of GST-MoS_2-3 memtransistor, demonstrating short-term synaptic plasticity. The PPF indexes is defined as $(A_2 - A_1)/A_1 \times 100\%$, where A_1 and A_2 are the amplitudes of the first and second current responses, respectively. (b) Multilevel conductance modulation of a GST-MoS_2-3 memtransistor, programmed into 64 distinct states by applying dynamic voltage pulses. (c) Repetitive LTP and LTD cycles of GST-MoS_2 memtransistors under cyclic pulsed stimuli. (d) Hand-written digit '0' input pattern used for image classification tasks. (e) Schematic illustration of an ANN employing GST-MoS_2 memtransistors as trainable synaptic weights. (f-h) Classification accuracy as a function of training iteration for three benchmark datasets: (f) cyber dataset, (g) large image dataset, and (h) small image dataset, respectively.

3. Conclusion

In summary, we have established a diameter-tunable CVD strategy for the wafer-scale synthesis of monolayer MoS_2 with precisely controlled grain sizes, enabling deterministic tuning of GB density. Given the analogous vapor-phase reaction kinetics and precursor chemistry among two-dimensional chalcogenides, the DT-CVD system should be broadly applicable to other TMDCs. Systematic structural, electrical, and computational analyses reveal that increasing GB density introduces shallow energy barriers and facilitates ionic migration and depletion region, which synergistically govern the observed analog resistive switching. The resulting memtransistors exhibit grain-size-dependent hysteresis, stable multilevel conductance

modulation, and endurance characteristics consistent with a hybrid diffusion-trapping mechanism. Notably, the GST-MoS_2-3 device achieves an optimal balance between switching tunability and stability, supporting up to 64 distinct conductance states with reliable short- and long-term synaptic functionality. When implemented in artificial neural network simulations, these devices deliver markedly improved learning and classification accuracy, underscoring the importance of analog resolution and multistate capability for neuromorphic computing. Overall, this work establishes a direct link between GB engineering in 2D materials and device-level neuromorphic performance, offering a scalable pathway toward energy-efficient, wafer-scale in-memory computing systems.

4. Experimental Section

DT-CVD system. The DT-CVD system was adapted from a commercial Planertech dual-zone CVD furnace (PlanarGROW-5S), consisting of a fixed quartz tube (outer diameter: 120 mm, inner diameter: 110 mm). A diameter-tunable quartz tube (with interchangeable inner diameters of 100, 85, or 70 mm) was inserted concentrically within the fixed tube and sealed at both ends using PTFE rubber O-rings. Stainless steel doors equipped with internal cooling water circulation were employed to maintain thermal stability and prevent heat leakage. Gas flow was regulated using mass flow controllers, while the overall system pressure was stabilized by an exhaust throttle valve (ATOVAC, ATV1000) and continuously monitored with a capacitance pressure gauge (ATOVAC). Automated process control was implemented to minimize operator-induced variations and ensure high reproducibility.

GST-MoS_2 Growth. Single-crystal sapphire wafers (c-axis ±0.2°, Latech Inc.) were first annealed in ambient air at 1050 °C for 2 h to remove surface contaminants and achieve atomically flat terraces. For precursor loading, MoO_3 powder (Sigma-Aldrich, 99.97%) was evenly distributed in a ceramic boat, and a Ni foam (3 × 3 cm^2, purity > 99%, pore density = 110 PPI, thickness = 1.0 mm, mass density = 1500 g m^{-2}) was placed directly on top. The annealed sapphire substrates were positioned above the Ni foam with ceramic spacers. This assembly was loaded into the high-temperature zone of the DT-CVD system. Sulfur powder (Sigma-Aldrich, 99.998%) was placed in a separate ceramic boat located in the low-temperature zone. During growth, 200 sccm Ar was introduced, and the high-temperature zone was first heated to 250 °C at a system pressure of 4 Torr and held for 20 min. Subsequently, the high-temperature zone was ramped to 740 °C, while the low-temperature zone was heated to 200 °C. Once the high-temperature zone reached 660 °C, the Ar flow was reduced to 50 sccm. Growth was maintained for 7 min (or shorter for growth-kinetics studies) until full substrate coverage was achieved, followed by natural cooling under 200 sccm Ar. A schematic of the DT-CVD setup and growth process is provided in **Figure 1a** and **Figures S1-S2**.

Materials Characterization. Optical microscopy (Olympus BX60 and BX53M) and atomic force microscopy (AFM, Bruker Dimension Icon) with RTESPA-300 probes in tapping mode were employed to characterize surface morphology and roughness. Kelvin probe force microscopy (KPFM, Bruker Dimension Icon) with MESP-RC-V2 probes was used to map surface potential variations at GBs, with GST-MoS_2 transferred onto conductive highly oriented pyrolytic graphite substrates. Raman and PL spectroscopy were performed on a WITec alpha300S system with a 532 nm excitation laser (He-Ne, 35 mW). High-resolution transmission electron microscopy (HRTEM) and selected-area electron diffraction (SAED) were carried out on FEI Titan 80/300 (200 kV) and FEI Talos (200 kV) instruments. For TEM imaging, GST-MoS_2 films were transferred onto 200-mesh Cu grids using a poly(methyl methacrylate) (PMMA 950 A5 in anisole, Kayaku Advanced Materials, Inc.)-assisted transfer method combined with PDMS stamps (Gel-Pak DGL-45×45-0065-X4).

Device Fabrication and Electrical Measurements. Top-gated FETs were fabricated using standard electron-beam lithography (EBL). First, the as-grown MoS_2/sapphire substrates were patterned by EBL, followed by electron-beam evaporation of Cr/Au (5/50 nm) source and drain electrodes and lift-off in acetone. The resulting channels had a length of 1 μm and a width of 5 μm. The devices were subsequently annealed in a high-vacuum chamber at 250 °C for 1 h to improve contact quality and remove adsorbates such as water. A 16 nm HfO_x dielectric layer was then deposited by atomic layer deposition (ALD, Picosun) at 150 °C using tetrakis(ethylmethylamino)hafnium (TEMAHf) as the precursor, with H_2O as the oxidant and N_2 as the carrier gas (250/200 sccm). The pulse and purge times for the precursors were 1 s, 100 ms, and 20 s, respectively. Subsequently, a second EBL step was performed for top-gate patterning, followed by the deposition of a 50 nm Au top-gate electrode. Electrical measurements, including both two-terminal and three-terminal I–V characteristics, and artificial synapse devices were conducted at room temperature by using an Keysight B1500A semiconductor device parameter analyzer integrated with a probe station (Probing Solutions, Inc.) under ambient dark conditions, and a Keithley 4200 semiconductor analyzer under vacuum environment.

Non-Isothermal Flow Simulation. Numerical simulations were carried out using COMSOL Multiphysics (COMSOL Inc., USA) with the Non-Isothermal Flow multiphysics interface, coupling Laminar Flow and Heat Transfer in Fluids. A compressible formulation under the low Mach number approximation ($Ma < 0.3$) was employed to capture the temperature dependence of gas density. Argon was used as the working fluid, with all thermophysical properties (density, viscosity, specific heat, and thermal conductivity) taken from COMSOL's built-in Argon library with temperature dependence enabled. The computational geometry was simplified to a 2D axisymmetric heated channel. Boundary conditions included a mass flow rate of 50 sccm Ar at the inlet (reference pressure: 4 Torr) and zero pressure at the outlet. The channel walls were set

as isothermal boundaries: 750 °C (upper wall) and 200 °C (lower wall), while all other surfaces were assumed thermally insulated. The mesh was physics-controlled and refined near the channel walls to resolve velocity and thermal gradients. A stationary, fully coupled solver was used until convergence was achieved with residuals below COMSOL's default tolerances.

Device TCAD Simulation. To gain deeper insight into the hysteresis behavior of top-gated MoS_2 devices, TCAD simulations were performed using the Silvaco Victory suite. Three-dimensional MoS_2-FET structures incorporating grain boundaries were constructed in Victory Mesh, and the corresponding electrical characteristics were simulated in Victory Device. Considering the strong dependence of drain current magnitude on the applied bias, the Poole–Frenkel mobility model was adopted, which accounts for the exponential increase of carrier mobility with electric field. In addition, the interfacial defect density, specifically Gaussian-distributed acceptor-like states at the HfO_2/MoS_2 interface, was set to scale proportionally with grain boundary density, thereby reflecting the enhanced trapping/detrapping processes associated with higher grain boundary concentrations. The gate bias was swept from 0 V to the target bias and back with a step of 0.1 V and a time interval of 0.01 s, enabling quantitative extraction of the hysteresis window as a function of sweep direction.

Artificial Neural Network Simulation. Artificial neural network (ANN) simulations were performed using the experimentally extracted conductance characteristics of GST-MoS_2 memtransistors within the CrossSim platform. For each GST-MoS_2 variant (GST-MoS_2-1 to GST-MoS_2-4), 20 cycles of SET and RESET data were collected to generate lookup tables. The lookup tables were then utilized to accurately simulate the impact of complex conductance update characteristics on network accuracy. Each layer of the network was implemented on a simulated crossbar array, which performed two core operations: vector-matrix multiplication and parallel rank-1 outer product updates. The nonlinear weight update will degrade the ANN training accuracy. To evaluate the weight update linearity, one device behavior model is built. The dependence of conductance change on the pulse number (P) is described with the following equations:

$$G_{LTP} = B\left(1 - e^{-\frac{P}{A}}\right) + G_{min} \tag{3}$$

$$G_{LTD} = -B\left(1 - e^{\frac{-P}{A}}\right) + G_{max} \tag{4}$$

$$\mathrm{B} = (G_{max} - G_{min})/(1 - e^{\frac{-P_{max}}{A}}) \tag{5}$$

where the G_{max}, G_{min}, and P_{max} are the maximum conductance, minimum conductance, and the maximum pulse number, respectively.[40] And these three parameters are directly extracted from the experiment data. A is the parameter that represents the linearity of weight update. The larger A is, the more linear the weight update is, and the higher the accuracy of the ANN is.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information (Figures S1–S22) provides additional supplementary figures and expanded data analyses supporting the main text, including the schematic of the DT-CVD setup, temperature profile, AFM characterization, reproducibility verification, device fabrication and electrical measurement details, SCLC/Schottky/PF model fitting, gate tunability, transfer-curve simulations, endurance and retention behavior, as well as synaptic linearity and classification accuracy. Supporting Information is available free of charge at https://pubs.acs.org/doi/XXXXXXX

Author contributions

M.C., X.L., and Y.H. contributed equally to this work. M.C., H.Z., X.J. and M.Z. conceived the idea and designed the experiments. X.L., Y.H., Z.C., and L.W. completed the simulation. M.C., J.W., and S.W.T. performed material characterization, electrical measurement and data analyzing. D.C., K.-W.A., and L.W. provided resources and supervised the research. All authors participated in writing and revising the manuscript.

Notes

The authors declare no competing financial interest

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