Study on Low Warpage and High Reliability for Large Package Using TSV-Free Interposer Technology Through SMART Codesign Modeling

Fa Xing Che, Masaya Kawano, Mian Zhi Ding, Yong Han, and Surya Bhattacharya

Abstract—Through-silicon via (TSV)-free interposer (TFI) technology eliminates TSV fabrication and reduces manufacturing and material cost. In this paper, structure–material–assembly–reliability–thermal (SMART) codesign modeling methodology is established for a package using TFI technology by considering wafer process, package assembly and package/board-level temperature cycling reliability, and thermal performance to optimize structure design, assembly process, and material selection. Experimental results are used to validate wafer warpage modeling results first. Through wafer-level modeling, suitable carrier and molding compound materials are recommended to control wafer warpage less than 2 mm for 12-in molded wafer. Effects of coefficient of thermal expansion of package substrate and stiffener on package warpage induced by assembly reflow process are simulated and analyzed. The recommended materials and geometry design based on thermal cycling reliability simulation are aligned with that from wafer and package warpage simulation results. The final test vehicle design and material selection are determined based on SMART codesign modeling results for achieving successful TFI wafer process and package assembly and long-term board-level reliability.

Index Terms—Finite-element analysis (FEA), solder joint reliability, structure–material–assembly–reliability–thermal (SMART) codesign modeling, through-silicon via (TSV)-free interposer technology, warpage.

I. INTRODUCTION

THROUGH-SILICON interposer (TSI) is a successful application of through-silicon via (TSV) technology [1]–[3]. The TSI technology realizes the heterogeneous integration of IC chips and vias offer vertical connection from the chips with fine-pitch I/Os to the substrate with medium-pitch I/Os [3]. However, TSV fabrication is facing many challenges, such as void-free filled Cu TSV and lower Cu protrusion [4]–[7], bonding/debonding process [8], thin wafer handling and wafer warpage control [9], [10], and long-term reliability of TSVs [11]–[13]. TSI is not a cost-effective technology due to wafer processes, material cost, and yield loss. New technologies are being explored to provide the similar function to TSI interposer but without TSV formation. Different terminologies are used for such technologies, such as silicon-less interconnection technology (SLIT) [14] and non-TSV interposer [15]. In our previous study, a package using SLIT technology results in a solder joint reliability and package warpage, which is comparable to that obtained using TSI technology [16]. In this paper, we call this technology as TSV-free interposer (TFI) technology. In TFI technology, the back-end-of-line (BEOL) layers are formed based on a Si or glass carrier, followed by chip-to-wafer bonding, wafer-level compression molding and back grinding (BG), carrier wafer (Si/glass) removal, solder ball attachment, and singulation. Therefore, TFI technology eliminates TSV fabrication and reduces manufacturing and material cost.

TFI technology still faces several challenges that need to be addressed, such as wafer warpage during wafer fabrication process, assembly-induced package warpage, and package/board-level solder joint reliability [14], [15]. Finite-element analysis (FEA) is a powerful and useful tool and has widely been used in the packaging design stage for virtual prototyping [9], [10], [16]–[18]. In this paper, a structure–material–assembly–reliability–thermal (SMART) codesign methodology with FEA simulation has been established and applied to TFI technology to optimize structure design, wafer process, assembly process, material selection, and thermal performance. Codesign modeling methodology for TFI technology includes TFI wafer process simulation to reduce wafer warpage, TFI package assembly process simulation to minimize package warpage, package/board-level temperature cycling (TC) simulation to improve controlled collapse chip connection (C4) solder joint reliability, board-level TC (TCOB) simulation to improve board-level solder joint reliability, and thermal simulation to evaluate and enhance thermal performance of TFI package. Through SMART codesign simulation, cost-effective and successful wafer and assembly processes and reliable and high-performance package solutions can be achieved for the advanced package using TFI technology.

II. FABRICATION PROCESS FLOW AND EXPERIMENTAL PROCEDURE

Fig. 1 shows the schematics of TFI package layout, in which one \(15 \times 15 \times 0.56\text{-mm}^3\) larger chip that is supposed to be a graphics processing unit (GPU) and two \(5.5 \times 7 \times 0.49\text{-mm}^3\) smaller chips that are supposed to be high-bandwidth memory (HBM) are mounted onto a
25 × 18-mm² TFI interposer. The final TFI package excluding C4 joint and stiffener has a thickness of 0.62 mm. Fig. 2 shows the process flow of TFI package test vehicle (TV) fabrication. The TFI interposer with three levels of 0.4 μm/0.4 μm fine line/space redistribution layer (RDL) is first fabricated on a Si or glass carrier wafer using BEOL process. Then, chip-on-wafer bonding process is conducted to mount GPU and HBM chips onto the wafer, followed by wafer-level underfilling. After wafer-level compression molding and BG, GPU chips are exposed and HBM chips are embedded with 100-μm overmold. Si stiffener with 500-μm thickness is then attached to the top of the molded wafer to help reduce wafer warpage and assembly warpage and enhance thermal performance of the package. After carrier wafer removal, under bump metallization (UBM) and C4 bumping with 300-μm pitch are conducted. After the singulation process, the obtained TFI package with the stiffener is 25 × 18 × 1.15 mm³ in size. The TFI package is then mounted onto a 30 × 25-mm² organic substrate by using C4 solder joints and finally attached to an FR4 printed circuit board (PCB) through ball grid array (BGA) solder joints. Underfill is used to protect C4 joints, but is not used for BGA joints. The final TV design and material selection are determined based on codesign modeling results for achieving a successful TFI wafer process, package assembly process, long-term package/board-level reliability, and optimal thermal performance.

An experiment is conducted by using a simple structure, as shown in Fig. 3, to validate the wafer warpage modeling method and also to help select suitable epoxy molding compound (EMC) material. Liquid or granular-type EMC is put onto a Si carrier with the calculated weight of the EMC material. Molding temperature for each EMC is applied accordingly. After wafer-level compression modeling, the molded wafer has 400-μm-thick mold compound and 770-μm-thick Si carrier. Wafer warpage after post-mold cure is measured by the Fogale TMAP IR measurement equipment. The measured warpage data are used for correlating with FEA simulation results (refer to results in Fig. 6).

III. SMART CODESIGN MODELING METHODOLOGY

Fig. 4 shows contents and topics included in the SMART codesign methodology, which has been established and applied for TFI packaging technology in this paper by using FEA simulation with ANSYS commercial software. The main purpose of codesign method is to optimize structure and
Fig. 4. SMART codesign modeling methodology.

Fig. 5. FEA models for different simulation purposes. (a) 3-D quarter model for wafer warpage simulation. (b) 3-D half model for package-level simulation. (c) 3-D slice model for package-level simulation. (d) 3-D slice model for board-level simulation.

geometry design, wafer process, assembly process, material selection, and thermal performance. Codesign modeling method for TFI technology in this paper includes wafer-level warpage, package warpage induced by assembly reflow process, package/board-level solder joint reliability, and thermal performance simulation. Wafer process sequence simulation using a 3-D quarter model of the wafer as shown in Fig. 5(a) has been established to simulate compression molding, BG, stiffener attach, carrier removal, and backside RDL processes. C4 bumping process and C4 joints are not modeled in the wafer-level simulation. For small features such as RDL, vias, UBM, and \(\mu\) bumps, thin layer is simplified with considering layer thickness and majority material (relatively high volume) in wafer-level simulation. Through wafer-level modeling, suitable carrier wafer and EMC materials and Si stiffener are recommended to control wafer warpage less than 2 mm for 12-in wafer, which is a requirement of warpage handling by lithography equipment. Effect of organic substrate, coefficient of thermal expansion (CTE), and stiffener thickness on assembly induced package warpage is simulated by a 3-D half model of the package as shown in Fig. 5(b) to reduce package warpage. Long-term package-level and board-level TC reliability are simulated to predict C4 and BGA solder joint thermal fatigue lives. Comparison between 3-D half model in Fig. 5(b) and 3-D slice model in Fig. 5(c) is carried out for C4 joint reliability. In order to reduce solving time and computing resource, a 3-D slice model as shown in Fig. 5(d) is also used for investigating board-level solder joint reliability. In the 3-D slice models, detailed structure and small feature size are included. Proper boundary conditions are applied for each model as shown in Fig. 5. Table I lists material properties used in each model. Stress-free temperature is chosen for materials according to their active (processing) condition in the actual processes. Temperature range from
TABLE I

<table>
<thead>
<tr>
<th>Materials</th>
<th>Modulus (GPa)</th>
<th>CTE (ppm/°C)</th>
<th>Poisson’s ratio</th>
<th>Tg (°C)</th>
<th>Remark</th>
<th>Thermal conductivity (W/m°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>EMC1-reference</td>
<td>18 (&lt;Tg), 1 (&gt;Tg)</td>
<td>7 (&lt;Tg), 22 (&gt;Tg)</td>
<td>0.3</td>
<td>160</td>
<td>Molding 125°C</td>
<td>0.8</td>
</tr>
<tr>
<td>EMC2</td>
<td>34 (&lt;Tg), 0.45 (&gt;Tg)</td>
<td>6 (&lt;Tg), 21 (&gt;Tg)</td>
<td>0.3</td>
<td>180</td>
<td>Molding 135°C</td>
<td></td>
</tr>
<tr>
<td>EMC3</td>
<td>10 (&lt;Tg), 0.5 (&gt;Tg)</td>
<td>4 (&lt;Tg), 21 (&gt;Tg)</td>
<td>0.3</td>
<td>170</td>
<td>Molding 125°C</td>
<td></td>
</tr>
<tr>
<td>Underfill</td>
<td>13 (&lt;Tg), 0.5 (&gt;Tg)</td>
<td>23 (&lt;Tg), 80 (&gt;Tg)</td>
<td>0.3</td>
<td>120</td>
<td>Curing 150°C</td>
<td>0.8</td>
</tr>
<tr>
<td>Silicon</td>
<td>131</td>
<td>2.8</td>
<td>0.28</td>
<td></td>
<td></td>
<td>130</td>
</tr>
<tr>
<td>Passivation</td>
<td>1.6</td>
<td>62</td>
<td>0.3</td>
<td>&gt;250</td>
<td>Curing 180°C</td>
<td>0.25</td>
</tr>
<tr>
<td>Bonding material</td>
<td>2 (&lt;Tg), 0.2 (&gt;Tg)</td>
<td>60 (&lt;Tg), 200 (&gt;Tg)</td>
<td>0.35</td>
<td>220</td>
<td></td>
<td>0.2</td>
</tr>
<tr>
<td>SiO2</td>
<td>73</td>
<td>0.5</td>
<td>0.17</td>
<td></td>
<td></td>
<td>1.5</td>
</tr>
<tr>
<td>Organic sub/PCB</td>
<td>25 (in plane)</td>
<td>11 (out of plane)</td>
<td>0.39 (in plane)</td>
<td>0.11 (out of plane)</td>
<td>Orthotropic</td>
<td>18.9 (in plane)</td>
</tr>
<tr>
<td>Solder-StnAgCu</td>
<td>60.1 (-40°C), 41.7 (25°C)</td>
<td>22 (28.3 (125°C), 0.2 (220°C)</td>
<td>0.35</td>
<td></td>
<td>Creep model</td>
<td>58.7</td>
</tr>
<tr>
<td>Cu</td>
<td>117</td>
<td>17</td>
<td>0.34</td>
<td></td>
<td>Elastic-plastic</td>
<td>386</td>
</tr>
<tr>
<td>Solder mask</td>
<td>2.4 (&lt;Tg), 0.2 (&gt;Tg)</td>
<td>50 (&lt;Tg), 160 (&gt;Tg)</td>
<td>0.3</td>
<td>101</td>
<td></td>
<td>0.2</td>
</tr>
</tbody>
</table>

–40 °C to 125 °C and cycle duration of 1 h are modeled for TC and TCOB loading. The recommended materials and structure design based on reliability are aligned with that from wafer and package warpage simulation results. The optimized TV structure and materials are finalized based on codesign modeling results and ready for process and fabrication.

IV. RESULTS AND DISCUSSION

A. Wafer Warpage Analysis and Validation

First of all, the wafer warpage modeling method is validated by experimental results. Fig. 6 shows correlation between experimental and simulation results (based on structure in Fig. 3). Simulation result has a good agreement with warpage measurement data. EMC 3 leads to the lowest warpage among three EMCs due to the lowest CTE mismatch between EMC 3 and Si wafer. The validated modeling method can be implemented in the real TV fabrication process to analyze and optimize wafer warpage.

In order to identify wafer warpage direction during wafer process, wafer direction and sign are defined in Fig. 7. Process-dependent modeling is conducted for wafer warpage simulation using element birth-and-death technique provided by software. Fig. 8 shows process dependent wafer warpage data at room temperature (25 °C) for the reference model. In the reference model, original molding thickness of 720- and 100-μm-thick molding compound (EMC 1) is removed after BG, and 770-μm-thick Si carrier and 500-μm-thick Si stiffener are modeled. Two critical processes inducing large warpage are identified by simulation results, i.e., molding process and carrier wafer removal process. Smiling shape warpage [>] 1 mm as shown in Fig. 9(a)] occurs after wafer-level compression molding and reduces slightly after BG process. The molded wafer becomes flat.
after stiffener attach. However, crying shape warpage (> 2 mm as shown in Fig. 9(b)) occurs after carrier removal and final RDL process, which arises a challenge for final RDL process. In order to control wafer warpage less than 2 mm through all processes, optimization needs to be conducted by means of FEA simulation.

B. Wafer Warpage Optimization

The effect of mold compound on wafer warpage is significant, as shown in Fig. 10, because wafer warpage is mainly induced by CTE mismatch between Si and EMC materials. EMC 1 and EMC 2 lead to similar wafer warpage, which are different from warpage results in Fig. 6 for the bilayered simple structure due to different structures and volume ratios of EMC to Si. EMC 3 results in the lowest wafer warpage among three EMCs due to low-CTE value of 4 ppm/K, which is one of candidates to ensure wafer warpage less than 2 mm during wafer processes.

If EMC 1 is used in the TFI package, wafer warpage can also be controlled less than 2 mm by choosing a suitable carrier wafer. Table II lists three glass carrier materials with different material properties, especially different CTEs. Fig. 11 shows wafer warpage results for different wafer carriers. Glass-1 carrier leads to the similar warpage results as Si carrier due to their similar CTE property. When glass carrier with high CTE is used, wafer warpage direction can be changed after compression molding. For the molded wafer with EMC 1, selecting glass-2 carrier (CTE = 5 ppm/K) helps to control wafer warpage less than 2 mm during wafer processes. Therefore, carrier wafer and EMC material selection should be considered as a system based on geometry structure and matched CTE requirement, which is also successfully applied in fan-out wafer-level packaging with both mold-first and RDL-first techniques to optimize wafer warpage [19].

Fig. 12 shows the effect of Si stiffener thickness on wafer warpage considering two major processes after stiffener attach, i.e., carrier removal and final RDL process. Wafer warpage is more than 2 mm after carrier removal and final RDL process if the stiffener is not applied. Even though EMC 3 has low-CTE value, wafer with EMC 3 still has large warpage when the stiffener is not used because EMC 3 has low modulus, which makes the structure much softer and flexible.
Stiffener helps to reduce package warpage by 40%–70%. Both EMC 1 and EMC 3 lead to similar package warpage at 25 °C. However, package warpage has a concave or smiling shape at 220 °C and also increases with increasing substrate CTE. Effect of stiffener on package warpage becomes insignificant at high temperature. Based on simulation results, organic substrate with low CTE (< 10 ppm/K) and applying stiffener on the top of the package are recommended to control package warpage less than 100 µm.

Fig. 14 shows the effect of substrate thickness on package warpage. For package with stiffener, substrate thickness influences on warpage are not significant. Effect of substrate CTE on package warpage is more significant than its thickness effect. To control warpage of the TFI package with stiffener, selecting low-CTE substrate is more efficient than changing substrate thickness.

D. C4 Solder Joint TC Reliability

Package-level TC reliability is modeled for TFI package using a 3-D half model [Fig. 5(b)] and a slice model [Fig. 5(c)] to investigate and predict C4 joint thermal fatigue life. The Sn–Ag–Cu lead-free solder is modeled for C4 joints using hyperbolic-sine creep constitutive model [20]. Temperature
range from $-40 \, ^\circ C$ to $125 \, ^\circ C$ and cycle duration of 1 h are modeled for TC loading. Fig. 15 shows creep strain energy density of C4 joints under TC loading for the TFI package with 500-$\mu$m-thick stiffener based on simulation results from the half model. For TFI package without underfill, C4 joints at package edges [Fig. 15(a)] have large creep strain energy density value, which corresponds to low solder joint life. Underfill is used to improve fatigue life of C4 joints at package corners and edges and makes C4 joints under Si die area have more uniform life [Fig. 15(b)]. Volume averaged creep strain energy density accumulation per cycle based on the interfacial layer of solder and package is used for fatigue life prediction.

The energy-based life model of Sn–Ag–Cu solder is expressed in the following:

$$N_f = 137.6 \times W_{cr}^{-1.112} \tag{1}$$

where $W_{cr}$ is the creep strain energy density from simulation results, and then fatigue life, $N_f$, can be predicted.

Fig. 16 shows fatigue life comparison of C4 joints at the package edge [column C1 in Fig. 15(b)] from the 3-D half modeling results [Fig. 5(b)]. For TFI package with stiffener but without underfill, C4 joint life is more sensitive to joint
location and the corner joint has much lower fatigue life. For TFI package without underfill, EMC 3 leads to lower C4 joint life than EMC 1 due to higher CTE mismatch between EMC 3 and organic substrate. C4 joints show more uniform and improved fatigue life when underfill is applied in the package. The effect of stiffener on C4 solder joint life is not significant when underfill is applied in package. Package with stiffener has slightly lower C4 joint fatigue life compared to package without stiffener.
without stiffener because Si stiffener makes the package not flexible and increases CTE mismatch between package and organic substrate. The main purpose of stiffener is to help reduce wafer/package warpage significantly. Therefore, underfill and stiffener are all needed to improve C4 solder joint reliability and reduce package warpage.

3-D half model is one very time-consuming model, which needs more than 50 h to solve one TC simulation for each case of TFI package, like results in Fig. 15. Simplified 3-D slice model cutting along TFI package center to edge with one row or C4 joints [Fig. 5(c)] is adopted for parametric study. In the 3-D slice model, only large GPU die is modeled with the same distance from die edge to package edge as in the 3-D half model. Fig. 17 shows simulation results and fatigue life of C4 joints from the 3-D slice model. C4 joints have similar life with helping from underfill. Life prediction based on bottom interfaces (organic substrate side) of C4 solder joint has slightly lower value compared to that based on top-side interface (chip side). Simulation results from the 3-D slice model are compared to those from the 3-D half model, as shown in Fig. 18. Similar life prediction from 3-D slice model and 3-D half model indicates that slice model is one accurate and simple model that can be used to do more parametric studies effectively. In [21], slice model was also verified as an efficient and accurate model through FEA simulation for BGA package subjected to TCOB loading condition. In this TFI package TC simulation case, solving time of 3-D slice model is just one tenth that of 3-D half model. With TFI package with underfill, EMC 1 and EMC 3 lead to similar C4 joint life (Fig. 18), which is different from results of TFI package without underfill (Fig. 16).

Underfill is important to improve C4 joint reliability, especially for large package size. However, it is essential and critical to choose suitable underfill to protect C4 joints. Otherwise, underfill may decrease C4 joint reliability [22], [23]. Table III lists four underfills and their properties. CTE and Young’s modulus are two critical mechanical properties affecting C4 joint reliability. Fig. 19 shows the effect of underfill on C4 joint reliability. Underfill 1 and 2 lead to similar results and good protection on C4 joint reliability due to their similar mechanical properties and similar CTE value as lead-free solder. Underfill 3 leads to poor C4 joint reliability due to
high CTE and low Tg. Underfill 1 is recommended to improve C4 joint reliability for TFI package, and it will be used in the following simulation.

Organic substrate is another important material affecting C4 joint reliability. The most important material property of substrate is its CTE. Fig. 20 shows the effect of substrate CTE on C4 joint reliability for TFI package with or without underfill using 3-D slice model. Substrate CTE has significant effect on C4 joint reliability of TFI package without underfill, and C4 joint life is sensitive to joint location. C4 joint fatigue life increases with decreasing substrate CTE because low substrate CTE leads to low-CTE mismatch between substrate and package. The effect of substrate CTE on C4 joint reliability is not significant for TFI package with underfill, and C4 joint life is not sensitive to joint location. For package with underfill, low-CTE substrate has no improvement for C4 solder joint reliability but helps to reduce package warpage. Considering both C4 reliability and package warpage concern, organic substrate with CTE of 10 or 7ppm/K is recommended.

E. Board-Level Solder Joint Reliability

When TFI package is assembled onto the PCB, TCOB reliability is another concern for BGA solder joint, which is simulated using a 3-D slice model [Fig. 5(d)]. In the 3-D slice TCOB model, underfill 1 is applied for C4 joints but not for BGA joints, and EMC 3 is used as molding compound. BGA joint has a pitch of 0.9 mm. Organic substrate has the same CTE of 15 ppm/K as the PCB in TCOB simulation, and substrate thickness is 1 mm and PCB thickness is 1.6 mm (common PCB thickness). PCB keeps a constant CTE of 15 ppm/K in TCOB simulation. Fig. 21 shows that C4 joints have slightly higher life under package-level TC test than that under TCOB test for the same TC test condition due to stiffer structure of board-level assembly compared to package-level assembly. Fig. 22 shows that BGA solder joint reliability is sensitive to joint location due to distance to neutral point effect and underfill not used for BGA joints. The bottom interface of BGA joint (PCB side) is critical compared to the top interface (package substrate side). The critical BGA joint is adjacent to Si stiffener edge, not package substrate edge. BGA solder joints show higher fatigue life compared to C4 joints.

Fig. 23 shows the effect of organic substrate CTE on critical C4 joint reliability and comparison between package TC and board-level TCOB conditions. With TFI package with underfill 1 for C4 joints, C4 joint reliability is not sensitive to organic substrate CTE in TCOB testing condition. Fig. 24 shows that substrate CTE affects BGA joint reliability significantly, which is different from its effect on C4 joint reliability. CTE mismatch between chip and substrate and between underfill and C4 joint are the main contribution for C4 joint reliability, while CTE mismatch between whole package (including chip and substrate) and PCB is a main contribution for BGA joint reliability. Substrate with 10-ppm/K CTE leads to high BGA life, which is also recommended for reducing package assembly warpage.

Fig. 25 shows the effect of substrate thickness on BGA joint reliability. When package substrate and PCB have the same CTE value (15 ppm/K), the critical BGA joint locates at Si stiffener edge/corner [Fig. 25(a)] and thin substrate helps to improve BGA solder joint reliability due to more flexible structure. When package substrate has CTE of 10 ppm/K while PCB has CTE of 15 ppm/K, the critical BGA joint locates at package substrate edge/corner [Fig. 25(b)] due to CTE mismatch between substrate and PCB. BGA joint life is less sensitive to substrate thickness with package with 10-ppm/K CTE substrate compared to package with 15-ppm/K CTE substrate, which is also applicable for the effect of substrate thickness on the critical BGA joint life as shown in Fig. 26(a). BGA joint life decreases with increasing substrate thickness. C4 joint reliability is not sensitive to substrate thickness and CTE under TCOB condition [Fig. 26(b)]. Organic substrate with CTE of 10 or 15 ppm/K provides good BGA joint reliability. Considering package warpage, organic substrate with 10 ppm/K is finally recommended.

F. Thermal Performance Modeling and Evaluation

3-D simulation model as shown in Fig. 27 has been constructed using a computational fluid dynamic software for thermal performance modeling. The equivalent thermal conductivity in the in-plane and out-of-plane directions is calculated based on volume averaging method for GPU and HBM microbump joint layer, C4 joint and underfill layer, and TFI interposer layer by considering joint and bump layout design and materials and their volume. Thermal modeling is
carried out for TFI package considering two power supply cases, i.e., 1 W for GPU chip and 1 W for each HBM chip, and 2 W for GPU chip and 0.7 W for each HBM chip. Fig. 28 shows the effect of Si stiffener on the maximum temperature of GPU and HBM chips. The stiffener can work as a heat spreader for HBM chip and slightly improve the thermal performance. Effect of stiffener on GPU thermal performance is not significant. The package can dissipate around 3.5-W total heating power (case 2 in Fig. 28) with help by 500-µm thick stiffener, while maintaining the operation temperature limit of HBM chip temperature less than 85 °C.

V. CONCLUSION

SMART codesign modeling methodology has been established for TFI packaging technology considering wafer process, package assembly and package/board-level reliability, and thermal performance. Low-CTE EMC material has matched properties with Si carrier wafer and helps to reduce wafer warpage. Stiffener is an effective way to reduce wafer warpage after carrier removal and assembly induced package warpage. Package- and board-level reliability show that C4 joint is more critical than BGA joint for TFI package. Through FEA simulation, the optimal underfill has been recommended for improving C4 solder joint reliability. C4 joints reliability is not sensitive to organic substrate CTE and thickness for TFI package with using suitable underfill for C4 joints. Thin substrate with medium CTE value helps to improve BGA joint reliability without violating the package warpage condition. The stiffener works as a heat spreader and thus improves package thermal performance, especially for the HBM chip. Based on the codesign modeling on warpage, reliability, and thermal performance results, geometry and materials are optimized and determined for the final TV design and fabrication: Si or low-CTE glass carrier wafer for wafer process, low-CTE EMC 3, underfill 1 for C4 joints, 500-µm-thick Si stiffener, 0.75-mm-thick substrate with 10-ppm/K CTE, and 1.6-mm thick FR4 PCB with 15-ppm/K CTE. The TV is in manufacturing stage right now, and further correlation work will be conducted.

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REFERENCES


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Masaya Kawano, photograph and biography not available at the time of publication.

Mian Zhi Ding, photograph and biography not available at the time of publication.

Yong Han, photograph and biography not available at the time of publication.

Surya Bhattacharya, photograph and biography not available at the time of publication.