Passive Devices Fabrication on FOWLP and Characterization for RF Applications

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Abstract—This paper presents the demonstration of integrated passive devices on a 300mm mold-first FOWLP technology platform with 3 metal layers (Cu RDL) build-up. In this case, a low-temperature cure, negative-tone polyimide (PI) material is selected as the inter-layer dielectric. MIM capacitors were fabricated on top of M1 RDL layer with low temperature CVD deposited inorganic as the dielectric and typical RDL barrier metal as the top and bottom electrode. Resistors were formed after M1 RDL layer by using typical RDL barrier metal as the thin film resistor. Last but not least, inductors were built on M2 RDL layer over epoxy mold material. Test keys for MIM capacitors, resistors and inductors were designed for electrical and RF characterization at the M2 layer.

Keywords—Passive Devices, MIM Capacitors, Resistors, Inductors, FOWLP

I. INTRODUCTION

As transistor channel lengths are being scaled down to sub-10nm regime for improved performance, this scaling is fast approaching its limits. The significant increase in production cost remains a major concern for continued transistor miniaturization in the industry. Advancement in wafer level packaging has opened up new opportunities for system-level integration and performance improvement. As compared to TSV interposer (TSI), Fan-Out Wafer Level Packaging (FOWLP) provides a cheaper alternative and in certain cases, even better electrical performance [1].

Meanwhile, passive components such as resistors, capacitors and inductors are critical and indispensable elements for RF applications and can be applied for various functions such as matching networks, amplifiers, resonators, filters and so on [2–3]. The market trend for passive devices is the size miniaturization, high integration, high working frequency, light weight and low cost for handheld wireless devices which further accelerate the thin film based passive elements integration together with the development of the advanced lithography to implement the fine featured, better tolerance controlled, high density integrated and better electrically performed passive elements as compared with standard discrete surface mount devices [4]. 3D passive devices integration in Si for system in package has been implemented at wafer level for front-end process to fabricate passive elements combined with active devices in one package for high reliability applications [5]. Kai Liu has reported a RF system with passive devices such as resistors, capacitors and inductors integrated with Si BEOL process [6]. Philippe Benech has also had a good review for passive elements integrated with Si BEOL for microwave and millimeter wave applications [7]. Xiaoyu Mi talked about the 3 different methods of passive elements integration for high frequency applications either with laminate or LTCC or Si based BEOL process [8]. To the author’s knowledge, there is no report yet for passive device integration with Cu RDL process for Fan-Out Wafer Level Packaging technology, which is the most attractive packaging method to provide lower cost, more I/O counts, better electrical performance and higher reliability compared with 2.5D or 3D packaging by TSV or TSV based interposer [9–10].

This paper presents the demonstration of integrated passive devices on a 300mm mold-first FOWLP technology platform with 3 metal layers (Cu RDL) build-up. In this case, a low-temperature cure, negative-tone polyimide (PI) material is selected as the inter-layer dielectric since the low temperature curing matches with epoxy wafers and it also exhibits good mechanical properties after curing [11]. MIM capacitors were designed with different parallel plate area sizes and fabricated on top of M1 RDL layer with low temperature CVD (<180°C) deposited inorganic film as the dielectric and typical RDL barrier metal as the top and bottom electrode. Resistors were designed with different line width and length and fabricated after M1 RDL layer by using typical RDL barrier metal as the thin film resistor material. Last but not least, inductors were also designed with different Cu RDL width and line space and built on M2 RDL layer over low-loss epoxy mold material. Test keys for MIM capacitors, resistors and inductors were all designed for electrical and RF characterization at the M2 layer.
layer with the bottom electrode connected to M2 through Via2 and the top electrode fabricated at M2 layer.

II. FABRICATION OF IPD INTEGRATED WITH FOWLP

A. WAFER RECONSTITUTION FOR FOWLP

FOWLP process here applied for this paper is the “Mold-First” method and Fig. 1 shows the process flow and Fig. 2 shows the schematic drawing for the process flow illustration for “Mold-First” method.

Step1: Chip pick & place on molding tape on frame

Step2: Wafer level molding

Step3: Release from mold & Backgrind

Step4: RDL and bump processing

Step5: Dicing and finish

Fig. 1 Process flow for “Mold-First” FOWLP

Fig. 2 shows the schematic drawing for process flows for “Mold-First” FOWLP and compared with “RDL-First” method, “Mold-First” method is easier and less costly as there is no carrier needed to support the Cu RDL fabrication and thus the following carrier removal process can also be neglected. The wafer reconstitution starts with dummy Al chips pick & place on the molding tape mounted on the stainless steel frame with certain distance allocated for each die to allow the more space for more I/O counts to be fan-out based on the locations for each die. After that EMC (epoxy molding compound) powder was dispensed on the chips manually and the molding tool will impose pressure and heating up to compress and form the molding so that the active chip surface is coplanar with mold compound [12]. Fig 3(a) and (b) shows the photos that were taken after EMC resin was dispensed on the chis and the reconstituted wafer after molding. After molding, a post molding curing was also applied to fully cure the EMC. In order to control the TTV, the molded wafer with original thickness of 1mm was sent for back grinding to reduce thickness further to be below 900um with TTV of around 10um. The die shift can be well controlled within 20um by implementing the pick and place compensation before molding to compensate the die shift caused by molding process.

B. INTEGRATION OF PASSIVE DEVICES WITH FOWLP

After wafer reconstitution was completed, the multilayer Cu RDL and integration of passive devices was followed. Before RDL process, the molded wafers were rinsed with DI water to remove the foreign particles first. As the 1st step, a kind of negative tone photosensitive dielectric polymer was coated, exposed and developed to form via make connectivity to the underlying Al chips. The lithography process window for this negative tone polyimide (PI) was also studied in terms of exposure energy and focus. From the lithography data, this negative tone polyimide works within 200~450mJ/cm2 for the exposure energy for 10um coating thickness while it is working within -15~5um for focus. Different via size was patterned with the smallest via size of 10um achieved. Fig 4(a) shows via profiles by FIB cut for via size of 10um and 30um respectively. After via patterning, the dielectric polymer was cured in the furnace at around 200°C for complete polymerization. After via1 was formed, O2 descum was applied to clear the polymer scum and following with seed layer of Ti/Cu deposition by PVD. After PVD seed layer was deposited, litho for M1 patterning and Cu RDL plating was carried on. After photoresist strip and seed layer wet etch, M1 was fabricated. As shown in Fig 4(b), M1 Cu RDL was nicely plated with a thickness of around 6um without any void.

After M1 fabrication was completed, similar Cu RDL process is repeated for via2/M2 and via3/M3 fabrication. MIM capacitors and resistors were integrated on the first Cu RDL. After formation of first layer Cu RDL, MIM stack is deposited by PVD for bottom and top electrodes and low temperature CVD process for SiN as the dielectric. The MIM stack is then patterned to define the MIM capacitors on the Cu RDL. Resistor structures are also formed after first layer Cu RDL using typical RDL barrier metal to be deposited by PVD. The barrier metal was also patterned to define the designed resistors on the 1st Cu RDL. After litho, both wet etch and dry etch method were evaluated and applied to fabricate MIM capacitors and resistors respectively. For resistors patterned by wet etching method, the isotropic etching will inevitably cause undercut and the fine line width of 2um will be sacrificed and only the line width≥5um resistors survived with almost 1um undercut at each edge of the line. 1um undercut caused by wet etching will affect the resistor precision. For MIM capacitors patterned by wet etching method, as the pad size is big enough and undercut caused by wet etching has very little effect on the performance of MIM capacitors. After MIM capacitors and resistors fabrication, PI coating and patterning of via2 was proceeded and Cu barrier seed PVD, patterning and second Cu RDL plating was then
carried out. Inductors are designed and embedded in the second Cu RDL layer as planar coil-structured with varied Cu line width and space. This is followed by another layer of PI dielectric with via openings for the top-most layer of Cu RDL. Fig.5(a) shows the resistors and capacitors after patterning by wet etching and Fig.5(b) shows the images taken by optical microscope for completed MIM capacitors, resistors and inductors with M2 connected out through Via2 as one of the testing pad and M1 as the other testing pad.

III. CHARACTERIZATION of INTEGRATED PASSIVE DEVICES

After M2 Cu RDL was fabricated, two testing pads for MIM capacitors and resistors were completed. One testing pad is the M2 testing pads connected to M1 through Via2 for bottom electrode and the other testing pad is M2 testing pads for top electrode. For inductors which was designed and embedded in M2 Cu RDL layer, the testing pads are formed after M2 Cu RDL was completed.

A. CHARACTERIZATION OF INTEGRATED RESISTORS

Resistors were designed with different line width of 2um and 5um, different line length of 2um, 5um, 10um and 20um. The film stack is the typical barrier thickness. By probing the 2 test keys, a DC bias voltage was swept from 0 to 10V. Through the Ohm's Law for R calculation: R=V/I, the resistance can be calculated. As discussed previously, the wet etching caused the 1um undercut and the resistor with line width of 5um can only obtain around 3um line width. Also the etching uniformity from device to device and from die to die will be causing some variation; thus the measured resistance may not be lineally to the resistor length. As shown in Fig. 6(a), for a resistor with length of 5um and width of 5um, an average resistance value calculated by Ohm's law is 16Ω; while the resistors with length of 10um and 20um and the same width of 5um, the average resistance value is only 25Ω and 42Ω respectively. On the other hand, from Fig. 6(a), it can be seen that for the total 50 dies that were measured shows very good uniform resistance value within the whole wafer with standard variation of 0.08-0.09 for different sizes of resistors. After wet etching, XSEM was also performed to check the cross section of the MIM resistor structures. As shown in Fig. 6(b), the XSEM data shows the cross section of the resistors with photoresist still remaining. It can be seen clearly that there is around 1um undercut below the photoresist.

B. CHARACTERIZATION OF INTEGRATED MIM CAPACITORS

MIM capacitors were sandwiched parallel plate structure with top and bottom parallel plate to be the typical RDL barrier layer and the capacitor dielectric to be the typical CVD deposited inorganic film. MIM capacitors were designed to be with different parallel plate area: 30umx30um, 50umx50um, 100umx100um and 30umx100um. For capacitance measurement, a C-V analyzer working at 100 kHz was applied to the 2 testing pads with AC=50mV and DC voltage sweep from -10V to 10V; for leakage current measurement, a DC bias voltage sweeping from -10V to 10V was applied. Similar as the resistors, capacitors were also tried with both dry etching and wet etching methods; while C-V measurement results show that the MIM capacitors integrated on FO were functioning. Both dry etched and wet etched MIM capacitors show comparable capacitance value and the capacitors by wet etching method even shows lower leakage current compared with capacitors patterned by dry etching method. As shown in Fig. 7(a), both capacitors by dry etching and those by wet etching exhibits a constant capacitance density of 1 fF/um² when voltage sweeps from -10V to 10V, which indicates that the undercut caused by wet etching has little influence on the capacitance value. For leakage test as shown in Fig. 7(b), the capacitors by wet etching method shows even lower leakage current of 5nA/um² at 10V as compared with that of 15nA/cm² at 10V by dry etching method and in future, further optimization is needed to tune the dry etching recipe to reduce the leakage current. A randomly selected 50umx50um capacitor was also sent for stress test for TDDDB at room temperature with voltage biased at positive value from 0 to 12V. As shown in Fig. 8, the capacitor shows the correct trend and matches with linear fit model.

C. CHARACTERIZATION OF INTEGRATED INDUCTORS

Planar coiled Cu RDL inductors were designed and embedded in M2, so once M2 was completed, the inductors were fabricated also. The planar inductors with different Cu RDL line width and space were designed: 5um-20um for both line width and line space. For inductors RF measurement, open-short deembedded method was performed in order to measure the inductance L, Q-factor and resonant frequency f. As shown in Fig. 9 (a) and (b), 3 inductors with different line width and space were measured and compared. Fig. 9(a) shows the comparison for the inductance value with changing of the RF frequency from 0 to 15GHz. It can be concluded clearly that with smaller line space, the inductor exhibits higher inductance value. Compared with the inductors with bigger line space, the inductor with smaller line space shows higher inductance value of 6.5nH, compared with that of 5.5nH and 4.5nH for bigger line spaced inductors just as shown in Fig. 9(a). Here, the line width all keeps the same value while line space of A<B<C. In terms of Q-factor, all three inductors show excellent Q-factor from 55 to 60, as shown in Fig. 9(b). In future, multi-level Cu RDL inductors will be tried to further optimize the performance in order to get higher inductance density value and even better Q-factor.
IV. SUMMARY

In summary, we have successfully demonstrated the integration of passive devices (capacitors, resistors and inductors) on a 300mm mold-first FOWLP platform. Some of the key results are summarized as follows:

1. 3-layer Cu RDL with varied thickness on encapsulated molded wafers has been successfully fabricated. Minimum line/space is 2/2um.

2. Negative-tone, low cure-temperature polyimide (PI) material as RDL dielectric has been implemented for improved reliability.

3. Integration and electrical performance of passive devices like resistors, MIM capacitors on FOWLP platform have been successfully demonstrated.

4. Low cost wet etching was evaluated for patterning MIM and resistor with results showing comparable performance to dry etching method in terms of leakage and capacitance values. MIM capacitors patterned by wet etching shows very good leakage current of 1E-13 at 10V; and capacitance density value of 1fF/um2 from -10V to 10V has also been demonstrated.

5. Resistors patterned by wet etching shows constant 16Ω for L=5um, W=5um resistors, 25Ω for L=10um, W=5um resistors and 42Ω for L=20um, W=5um resistors.

6. Planar Cu inductor shows highest inductance value of 6.5nH and respectable Q-factor of 60 at 5GHz for all planar Cu coiled inductors as measured by open short method.

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REFERENCES


Fig. 2 Schematic drawing of process flow steps for “Mold-First” FOWLP

Fig. 3 (a) Reconstituted wafer after Al chips pick&place for EMC dispensed on the chips for molding and (b) after wafer reconstituted
Fig 4 (a) FIB cut for 10um Via after PI curing and (b) FIB cut for 1st Cu RDL (M1) with Via size of 10um

Figure 5 (a) OM for resistors and capacitors after wet etching and (b) XSEM for M1/Via2/M2 film stack after M2 completed
Fig. 6. (a) Resistance value measured for 50 dies for different resistor size and (b) XSEM show 1um undercut at resistor edge

Fig. 7 (a) Capacitance density comparison and (b) leakage current comparison for capacitors patterned by dry etching and wet etching
Fig. 8 TDDB as a function of applied bias voltage from 0 to 12V and line represent fits using linear field model.

Fig. 9 (a) Inductance value for 3 inductors with different line space (A<B<C) and (b) Q-factor data with RF frequency from 0 to 25GHz for these 3 inductors.