An Ultra-Low Voltage Level Shifter using Revised Wilson Current Mirror for Fast and Energy-Efficient Wide-Range Voltage Conversion from Sub-Threshold to I/O Voltage

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Abstract-- this paper presents a novel ultra-low voltage level shifter for fast and energy-efficient wide-range voltage conversion from sub-threshold to I/O voltage. By addressing the voltage drop and non-optimal feedback control in a state-of-the-art level shifter based on Wilson current mirror, the proposed level shifter with revised Wilson current mirror significantly improves the delay and power consumption while achieving a wide voltage conversion range. It also employs mixed-Vt device and device sizing aware of inverse narrow width effect to further improve the delay and power consumption. Measurement results at 0.18μm show that compared with the Wilson current mirror based level shifter, the proposed level shifter improves the delay, switching energy and leakage power by up to 3×, 19×, 29× respectively, when converting 0.3V to a voltage between 0.6V and 3.3V. More specifically, it achieves 1.03 (or 1.15) FO4 delay, 39 (or 954) I/transition and 160 (or 970) pW leakage power, when converting 0.3V to 1.8V (or 3.3V), which is better than several state-of-the-art level shifters for similar range voltage conversion. The measurement results also show that the proposed level shifter has good delay scalability with supply voltage scaling and low sensitivity to process and temperature variations.

Keyword-- level shifter, ultra-low voltage, current mirror

I. INTRODUCTION

In the past, voltage scaling has been widely used to reduce the power consumption in digital circuits and systems. Conventional voltage scaling is performed in the super-threshold region, well above the threshold voltage of transistors, resulting in limited power reduction. Recent studies have shown that the supply voltage can be further scaled to near or below the threshold voltage to achieve significant power reduction when high performance is not needed [1-9]. As the complexity and flexibility of Systems on Chips (SoCs) increase, in the future, SoCs are likely to consist of many power domains with significantly different supply voltages to achieve high energy-efficiency for tasks that require substantially different performance. Therefore, level shifters with wide voltage conversion range from near/sub-threshold voltage to nominal voltage or I/O voltage are needed to enable data exchange between different power domains. As the number of power domains or data width in the SoC increases, the number of level shifters increase dramatically and can be as many as tens of thousands. The delay, power and area overhead incurred by the level shifters has significant impact on the overall system [9].

To address this, level shifters with small delay, low power consumption, small area or wide voltage conversion range have been proposed in the past, including low voltage level shifters and ultra-low voltage level shifters [11-22]. As low voltage level shifters have been extensively studied, the ultra-low voltage level shifters are the study focus of this paper. Most of the existing ultra-low voltage level shifters are based on two types of topologies: cross-coupled PMOS based (Type I) and current mirror based (Type II). They have their own advantages and disadvantages as will be discussed later in Section II. Some level shifters achieve small delay at the cost of switching energy and/or area. Some level shifters have large standby power which is problematic for long clock period or low duty cycle applications. Some can only operate with limited voltage conversion range. In addition, the delay of some level shifters does not scale well with supply voltage, making them not suitable for dynamic voltage scaling (DVS).

In this paper, state-of-the-art ultra-low voltage level shifters based on both Type I and Type II topologies have been reviewed. By investigating their advantages and disadvantages, we proposed a ultra-low voltage level shifter for fast and energy-efficient wide-range voltage conversion from sub-threshold up to I/O voltage. The proposed level shifter is based on Type II topology (i.e. current mirror based). By addressing the voltage drop and non-optimal feedback control in a state-of-the-art Type II level shifter - Wilson current mirror based level shifter (WCMLS) [18], the delay and power consumption are significantly reduced for a wide voltage conversion range. In addition, the proposed level shifter has good delay scalability with supply voltage scaling, making it suitable for DVS applications. It also shows low sensitivity to process & temperature variations.

The rest of the paper is organized as follows. Section II discusses the advantages and disadvantages of state-of-the-art ultra-low voltage level shifters based on Type I and II. Section III discuss the voltage drop and non-optimal feedback control issues in the WCMLS. Section IV presents the proposed level shifter. Section V shows the measurement results and
comparison between the proposed level shifter and other state-of-the-art ultra-low voltage level shifters, and Section VI draws the conclusions.

II. STATE-OF-THE-ART ULTRA-LOW VOLTAGE LEVEL SHIFTERS

Fig. 1 (a) shows the topology of the Type I level shifter which uses cross-coupled PMOS devices to achieve full-swing conversion from input voltage (VDDL) to output voltage (VDDH). It has close-to-zero standby power due to complementary pull-up and pull-down network. The major drawback is the strong contention between the pull-up and pull-down network during switching. When IN and VDDL are lowered to around threshold voltage, the pull-down transistors (M1, M2) become extremely weak and cannot overcome the strength of the pull-up transistors (M3, M4) when VDDH is in super-threshold region. As a result, the output fails to flip. A way to increase the strength of pull-down transistors is to upsize the transistors. However, previous studies [14][18] show that the pull-down transistors need to be up sized by several orders of magnitude in order to overcome the strength of pull-up for converting sub-threshold voltages to super-threshold voltages, which is impractical. Another way is to use low Vt transistors for pull-down and high Vt transistors for pull-up. However, the effect is limited as the voltage difference between VDDL and VDDH is far larger than the voltage difference between high Vt and low Vt. As a result the pull-down transistors still need to be heavily up sized, leading to large area and load capacitance which increases the energy consumption and limits the reduction of the delay.

In the past, several ultra-low voltage level shifter based on Type I topology have been proposed [11-17]. In [11][16][17] the pull-up network is weakened by using reduced swing inverter (RSI) or weak keeper with pulsed control. These mechanisms facilitate wide-range voltage conversion while increasing switching energy and complexity substantially. Also, the pull-up network is constantly weakened. This causes delay scalability issue with supply voltage scaling, making them unsuitable for DVS. In [13][14], multi-stage level shifters with intermediate supply voltages are proposed to facilitate wide-range voltage conversion. However, [13] need additional circuits to generate the intermediate supply voltage, resulting in increased power consumption and area. [14] eliminates the voltage generation circuits by using a diode-connected NMOS. A problem is that the voltage across the diode is constant, causing a delay scalability issue similar to [11][16]. Another problem of multi-stage level shifters is that their delay is relatively larger than the single-stage structure. In [12][15], forward body bias is applied to the pull-down transistors to reduce the transition delay. While achieving improved performance, the designs increase the power consumption and complexity due to body-bias control.

Type II topology is based on the current mirror structure as shown in Fig. 1 (b). The advantage of this type of topology is that it has low contention because there is almost no overlap between the pull-up and pull-down. So there is no need to weaken the pull-up for fast wide-range voltage conversion. It is easy to achieve small delay and switching energy as well as delay scalability. However, the problem of this type of topology is that the static current flowing through M1 & M3 causes large standby power for high output, and the standby power increases as the VDDL increases.

To address this issue, several modified Type II level shifter have been proposed [18-20]. [18] proposed the WCMLS. It uses a feedback transistor to cut off the static current after the output goes high. This reduces the standby power significantly with the lowest complexity. However, the delay and power consumption are not optimal due to several issues including output voltage drop and non-optimal feedback control as will be discussed later in section III. [19] proposed a Type II level shifter based on logic error correction. The basic idea is to control the current mirror by sensing the logic error between input and output so that the current is enabled during switching and disabled after the output flips. It significantly reduces the standby power. However, this results in increased delay and switching energy due to the operation of the logic error correction circuits. In [20] a level shifter with a modified Wilson current mirror hybrid buffer is proposed. It uses a delay balancing path and a NOR gate to balance the rise and fall delay for close range voltage conversion. However, the PMOS devices in the NOR gate cannot be switched off completely.

Fig. 1 Conventional level shifter topologies: (a) Type I: cross-coupled structure, (b) Type II: current mirror structure.
causing large static current and thus standby power in the NOR gate. The static current can be reduced by reducing the size of the PMOS and NMOS in the NOR gate, but this will increase the delay. In addition, the stacking PMOS devices in the NOR gate will slow down the output fall transition, leading to increased average delay and switching energy especially for wide-range voltage conversion.

After investigating the advantages and disadvantages of the Type I & II ultra-low voltage level shifters, we chose type II as the topology of the proposed level shifter as it has less contention which provides potential for achieving small delay, low switching energy, and delay scalability. We chose WCMLS as a starting point due to its relatively low standby power and small area.

### III. Wilson Current Mirror Based Level Shifter

Fig. 2 shows the schematic of the WCMLS. It uses a feedback PMOS (M5) to cut off the static current flowing through M1 & M3 after switching. This reduces the standby power in the conventional type II level shifter. However, as the source current is cut off, the mirror current flowing through M4 is largely reduced, resulting in weakened pull-up strength and a voltage drop at node A. Although the voltage drop in turn increases the source current through the feedback control, the current increase is too small to pull the voltage at node A back to VDDH. The output finally stabilizes at a voltage below VDDH, which causes large static current and standby power in the output buffer of the level shifter. To study this, we have re-implemented the WCMLS at a 0.18 µm CMOS technology.

Fig. 3 shows the simulated voltage drop at node A of WCMLS. A voltage drop of more than 250mV can be observed when voltage at node A stabilizes. Fig. 4 shows the values of voltage drop against VDDH, as well as the resultant standby power in the output buffer, which reaches to around 4 nW at VDDH of 1.8V. For ultra-low voltage operation, the clock period is relatively long due to exponentially increasing delay with decreasing supply voltage, so the standby energy can be significant and dominates the overall energy consumption of the level shifter. By simulation, we found that upsizing M4 in WCMLS can reduce the voltage drop at node A to some extent, however, this significantly increases the switching energy, and has a limit in the reduction of voltage drop (VDDL=0.3V, VDDH=1.8V).

Fig. 5 Increasing the transistor width of M4 in WCMLS can reduce the voltage drop at node A to some extent, however, this significantly increases the switching energy, and has a limit in the reduction of voltage drop (VDDL=0.3V, VDDH=1.8V).
Another issue of WCMLS is that during the output fall transition the feedback control turns on M5 causing charge sharing from node B to node C. As node C is at ground level, this results in a pull-down of the voltage at node B and cause a sudden increase in the fall delay. Fig. 6 shows the simulated fall transition of WCMLS for converting 0.3V to 1.8V. It can be seen that the delay increase due to charge sharing is around 60 ns. This also causes large switching current, as shown in Fig. 6.

In addition, while the feedback control from node A cut off the source current, it significantly slows down the rise transition at A as the charging of A becomes weaker with reduced source current. The feedback also increases the load capacitance at A which further slows down the transition. Fig. 7 shows the simulated rise transition at node A of the WCMLS. It can be seen that the rise transition at A is significantly slow down by the feedback, which results in a large rise delay as well as large switching current.

IV. PROPOSED LEVEL SHIFTER

To address the above mentioned issues, a novel ultra-low voltage level shifter with revised Wilson current mirror is proposed as shown in Fig. 8. First, an input-controlled diode chain is proposed to prevent the voltage drop at node A. As a result the static current in internal output buffer is eliminated, which reduces the standby power in the WCMLS. Second, a revised feedback control is proposed to address the charge sharing issue and slow rise transition at A in the WCMLS, which reduces the delay and switching energy. Third, to further reduce the delay and power consumption, a device sizing technique utilizing inverse narrow width effect (INWE) is adopted in the proposed level shifter. In addition, the proposed level shifter utilizes mixed-V<sub>T</sub> devices (1.8V normal, 3.3V normal, 3.3V native) to extend the voltage conversion range to I/O voltage while maintaining small delay. The proposed techniques are described in details in the following sections.

A. Input Controlled Diode Chain

An input-controlled diode chain (M8-M12) is proposed to address the voltage drop issue in the WCMLS. With the rise transition at IN, M1 & M5 are turned on, pulling node B down and generating pull-up current through M4 to charge node A. At the same time, the input-controlled diode chain is activated to help pull node B down. After A is charged to high, the inverted output D turns off M7 to cut off the source current so as to reduce the standby power in the conventional type II level shifter. This tends to raise the voltage at node B and generate a voltage drop at node A. However, in the proposed level shifter, the input-controlled diode chain and the diode-connected PMOS M3 will form a voltage divider to keep the voltage at node B lower than VDDH with sufficient margin. This will maintain sufficient pull-up strength at node A and eliminate the voltage drop. As shown in Fig. 9, when converting 0.3V to 1.8V, node A successfully reaches 1.8V full VDDH in the...
proposed level shifter. The voltage level at B depends on the number of stacking NMOS in the diode chain and varies with VDDH. Fig. 10 shows the simulated voltage levels at node B for both WCMLS and the proposed level shifter against VDDH. It can be seen that the voltage level at B of the proposed level shifter scales well with VDDH and is always lower than that of the WCMLS by around 200 mV. The voltage difference between B and VDDH of the proposed level shifter is around 350mV. In this case the 3.3V PMOS M4 (with a threshold voltage of around 750mV) is still in the sub-threshold region. However, the gate voltages of NMOS M2 and M6 are only zero. Due to the fact that current is exponentially dependent on the voltage in the sub-threshold region as well as the stacking effect in the pull-down path, the pull-up current is much larger than the pull-down current, which provides sufficient strength to maintain the node A at VDDH after rise transition. We have also simulated the leakage current of the input-controlled diode chain against VDDH. As shown in Fig. 11, the leakage current through the diode chain is extremely low (< 10 pA) and the resultant leakage power is negligible. This is mainly due to the large threshold voltage (~750mV) of the 3.3V devices (M3, M9, M10, M11 and M12) which makes the sum of the threshold voltage of these transistors larger than VDDH. In addition, the small gate voltage of the controlling transistor M8 also helps limit the leakage current.

\[ \text{Voltage at B of WCMLS} \]
\[ \text{Voltage at B of Proposed LS} \]
\[ \text{Voltage at A of Proposed LS} \]

Fig. 10 Due to the input-controlled diode chain, the voltage at node B of proposed LS is lower than that of WCMLS, providing sufficient pull-up strength and eliminating the voltage drop at node A.

\[ \text{Voltage [V]} \]
\[ \text{Time [s]} \]

Fig. 12 Fall transition of the proposed LS. The delay and switching current are significantly reduced, compared to WCMLS.

\[ \text{Leakage Current [pA]} \]
\[ \text{VDDH [V] @ VDDL = 0.3 V} \]

Fig. 11 Leakage current through the diode chain is less than 10pA in the proposed LS.

\[ \text{Voltage [V]} \]
\[ \text{Time [s]} \]

Fig. 13 Rise transition of the proposed LS. The revised feedback control significantly reduces rise delay and switching current, compared to WCMLS.

B. Revised Feedback Control

In order to address the charge sharing and slow rise transition issues in the WCMLS, we revised the feedback control by replacing the feedback PMOS with NMOS (M7) and using the inverted output (node D) to control its gate in the proposed level shifter. In addition, the feedback NMOS is placed below the input transistor M1 instead of above it. During fall transition, node D goes from low to high, which turns on the M7. However, M1 is off as the input is low. Therefore there is no charge sharing from node B to node C. This prevents the sudden increase in fall delay and significantly reduces the switching current as shown in Fig. 12.

Another advantage of the revised feedback control is that the feedback now is from the node D instead of node A, which adds a delay in cutting off the source current. This maintains sufficient charging strength in the most time of the rise transition. Also, the load capacitance at node A is reduced, resulting in a faster rise transition. Fig. 13 shows the rise delay and switching current in the proposed level shifter, which is much smaller compared with WCMLS (Fig. 7).

C. Device Selection and Sizing

In the design of ultra-low voltage level shifter, in addition to the topology, device selection and sizing are important in achieving co-optimized delay, power and area.
In order to extend the voltage conversion range to I/O voltage, 3.3 V devices need to be used. However, they have large threshold voltage which is not good for fast voltage conversion. In the proposed level shifter, 3.3 V native devices and 1.8 V devices with connected gates are used for the input transistors while 3.3 V normal devices are used in the high voltage portion as in [17]. The combination of mixed-Vt device helps achieve I/O voltage tolerance while maintaining relatively small delay. It is noted that in the used 0.18 µm process technology there is no multi-Vt transistors available for 1.8 V devices, otherwise they can be used to further optimize the performance as suggested in [14].

Inverse narrow width effect (INWE) [10] has been reported as a parasitic effect which causes the transistor threshold voltage to decrease with decreasing transistor width in the narrow width region. To take advantage of lower threshold voltage at smaller width, we size the transistors in the level shifter by using multiple minimum-width fingers. In this way, the required current is achieved with smaller width. Compared with the conventional sizing, the INWE-aware sizing provides larger current with the same width, or the same current can be delivered with smaller width, which helps reduce the delay and power consumption due to reduced load capacitance. It is noted that as the INWE-aware sizing boosts the transistor current, the current variation also increases as shown in Fig. 14. This is similar to using low Vt transistors. The tradeoff need to be considered during the design optimization.

Fig. 14 INWE-aware sizing gives larger transistor current than conventional sizing due to reduced threshold voltage. In other words, to deliver the same current, INWE-aware sizing requires smaller transistor width than conventional sizing, leading to reduced delay and power consumption.

Fig. 15 Architecture of the testing chip.

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The proposed level shifter is implemented as double-row standard cell and fabricated with the 0.18 µm CMOS process technology. For comparison, the WCMLS from [18] is also re-implemented on the same technology with optimized device sizes through extensive simulation. The device types and sizes in the two level shifters are shown in Table 1. The WCMLS comprises only 1.8V devices for being consistent with [18] while the proposed level shifter comprises mixed-Vt devices (1.8V, 3.3V normal and 3.3V native). We applied INWE-aware sizing to both level shifters for optimized delay and power consumption. The total layout area numbers are also shown in Table 1 for comparison.

Fig. 15 shows the architecture of the testing chip. The input signal is from an external function generator. As the input signal is powered by VDDL, to avoid long delay, it is directly fed into the tested level shifters without buffering. The slope of the input is set to FO4 slope simulated at VDDL. The output of the level shifters are buffered to drive the output pad. Here the buffers for both level shifters are implemented with 3.3V device for fair comparison. In the rest of the paper, we name these buffers as external buffers to differentiate with the internal buffers in the level shifters. The power supplies of the level shifters and the external buffers are separated to facilitate power measurement.

For the proposed level shifter, the measured widest voltage conversion range is 0.21V to 3.3V, while for the re-implemented WCMLS it is 0.23V to 1.8V. To compare the performance of the two level shifters for typical ultra-low voltage applications targeting at hundreds of KHz to MHz range operating frequencies, we set VDDL to 0.3V, and vary VDDH from 0.6V to 3.3V. The delay of the level shifter is measured by subtracting the delay of the external buffer (post-layout simulation result) from the total delay measured between the input pad and the output pad. In most of the testing cases VDDH is much higher than VDDL, so the delay of the external buffer is much smaller than the delay of the level shifter. Therefore the delay variation of the external buffer will

V. EXPERIMENTAL RESULTS AND COMPARISON

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not affect the delay measurement of the level shifters. The only exceptional testing cases are when VDDH is very low (i.e. 0.6V-0.8V), where the delay of the external buffer becomes comparable to the delay of the level shifter. In these cases, the delay variation of the external buffer may cause some inaccuracy in the delay measurement, but this should not affect the comparison as the delay subtraction is the same for the two level shifters. Fig. 17 shows the measured average delay against VDDL. To remove the impact of process technology, the measured delay is also displayed using the FO4 delay at 0.3V. The proposed level shifter shows much smaller delay than the WCMLS for all VDDHs. The maximum delay reduction is 3×, measured at VDDH of 0.6V. The WCMLS is measured up to 1.8V as it does not use 3.3V device while the proposed level shifter is measured up to 3.3V. An interesting phenomenon observed here is that as VDDL is increased from 0.6V to 3.3V, the delay of the two level shifters decreases first and then increases. This is because the delay of the level shifter is composed of the delay of shifting stage and the delay of internal buffer. When VDDL is increased, the delay of shifting stage increases while the delay of internal buffer decreases, resulting in a turning point for the total delay.

Fig. 18 shows the measured average delay of the two level shifters against VDDL, where the VDDH is fixed to 1.8V. It can be seen that the delay of the proposed level shifter is smaller than that of WCMLS for VDDL below 0.7V, but larger than WCMLS for VDDH above 0.7V. This is because the internal buffer of the WCMLS is implemented with 1.8V devices while the internal buffer of the proposed level shifter is implemented with 3.3V devices for I/O voltage conversion. When VDDL is low, the delay of the internal buffer has negligible contribution to the delay of the level shifter. However, when VDDL gets close to VDDH, the delay of the internal buffer becomes comparable or larger than the delay of the level shifter. As 3.3V device has higher threshold voltage than 1.8V device, the delay of the proposed level shifter becomes larger than that of WCMLS for high VDDHs. To confirm this, we replaced the 3.3V devices in the internal buffer of the proposed level shifter with 1.8V devices, and plotted the simulated delay. The simulated delay for WCMLS and FO4 are also plotted for comparison. As can be seen in Fig. 18, the delay of proposed level shifter using 1.8V devices for the internal buffer is much smaller than that of WCMLS at all VDDLs. In addition, its delay tracks the FO4 delay very well even when the VDDL is very close to VDDH. This indicates that the proposed level shifter is suitable for DVS.

Fig. 19 shows the measured leakage power consumption and total power consumption of the two level shifters with an input of 100 kHz. The average switching energy per transition calculated from the measured total power and leakage power is shown in Fig. 20. As depicted in the Fig. 19 and 20, the proposed level shifter consumes much less leakage and dynamic power than the WCMLS for all VDDH due to the input-controlled diode chain which reduces standby power in the internal buffer and revised feedback control which reduces switching energy. The maximum reduction on leakage power and switching energy are 29× and 19×, measured at VDDH of 1.8V and 1.6V, respectively.

To investigate the robustness of the two level shifters, we have simulated them at different corners. Fig. 21 shows the delay of the two level shifters at different corners (FF, SS, FS and SF). Both level shifter operates well at FF, SS and SF corners when VDDH is scaled from 0.6V to 1.8V/3.3V. However, at FS corner the WCMLS stops working when VDDH is below 1V, while the proposed level shifter continue operating for VDDH down to 0.6V. The observed phenomenon is that for rise transition the output of WCMLS is unable to reach to even half VDDH. This is because at FS corner the PMOS becomes very weak. When node A in the WCMLS has not reached half VDDH, the feedback PMOS M5 is already cut off which prevents A being continuously charged. In the proposed level shifter, the feedback is delayed by a inverter which allows more charging time for A. Also, the source of M7 is ground, unlike in the WCMLS where the source of M5 is lower than VDD for around V_f. These makes the output of proposed level shifter able to reach close to VDDH at FS corner. As the feedback control is done with NMOS M7, the proposed level shifter is slightly slower than WCMLS at SF corner for VDDH below 0.9V. For all other voltages and corners, the proposed level shifter is faster than WCMLS. In Fig. 21 we have also added the measured delay of the two level shifters. The results indicate that the fabricated chip has fast NMOS devices and median speed PMOS devices between the fast and slow PMOS corners.
Fig. 22 shows the simulated delay (normalized against FO4 delay at VDDL) of the two level shifters over temperature from -40°C to 125°C. The maximum delay variation over the temperature range is 1.23x/1.16x for the proposed level shifter and is 2.96x/1.27x for the WCMLS, when converting 0.3V to 0.6/1.8V. For both level shifters, the delay variation is less when converting to 1.8V than converting to 0.6V, because the current dependence on temperature is less when VDDH is in the super-threshold region. Compared with the WCMLS, the proposed level shifter has less sensitivity to temperature variation, especially when converting 0.3V to 0.6V. This is because the current and thus the delay is significantly dependent on temperature when VDDH is in the near-threshold region which amplifies the difference between the two level shifters. Also, in this case, as the temperature decreases, the delay of WCMLS increase faster than FO4 increases due to the weak feedback, resulting in an increase in the normalized delay.

Table 2 compares the performance and power consumption of the proposed level shifter with several state-of-the-art ultra-low-voltage level shifters. The delay of the proposed level shifter is 1.03 FO4, 1.04 FO4 and 1.15 FO4 for converting 0.3V to 1.8V, 2.5V and 3.3V respectively, which is the smallest among the compared level shifters for similar range voltage conversion. The proposed level shifter also shows the lowest switching energy and the second lowest leakage power among the compared level shifters for similar range voltage conversion. Regarding the leakage power, the level shifter with logic error correction [19] is the lowest. However, this is achieved in the price of delay and switching energy. We have also performed 2k-point Monte-Carlo simulation, which shows that the delay of the proposed level shifter under 3σ variation is small compared with other compared level shifters. A drawback of the proposed level shifter is that it has relatively large area, however, this can be reduced by using advanced technology nodes. Also, as previously discussed, the area can be reduced by eliminating the native devices if the application does not need I/O voltage conversion.

VI. CONCLUSIONS

In this paper a novel ultra-low voltage level shifter is proposed. The proposed level shifter achieves small delay and low power consumption for wide-range voltage conversion from sub-threshold to I/O voltage by using revised Wilson current mirror which comprises an input-controlled diode chain and revised feedback control. It also employs mixed-V, device and INWE-aware device sizing to further improve the delay and power consumption. Measurement results at 0.18μm show that the proposed level shifter has significantly improved delay, switching energy and leakage power for wide-range voltage conversion, compared with the Wilson current mirror based level shifter. It achieves 1.03 (or 1.15) FO4 delay, 39 (or 954) fJ/transition and 160 (or 970) pW leakage power, when converting 0.3V to 1.8V (or 3.3V), which is better than several state-of-the-art level shifters for similar range voltage conversion. In addition, the measurement results show that the proposed level shifter has good delay scalability with supply voltage scaling and low sensitivity to process and temperature variations.

REFERENCES


Table 2 Comparison with state-of-the-art ultra-low-voltage level shifters

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<td>0.21V - 3.3V</td>
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<tr>
<td>Delay</td>
<td>2.38 FO4 (0.3V → 2.5V)</td>
<td>&lt; 1 FO4 (0.3V → 1.2V)</td>
<td>10 ps (0.4V → 3V) (FO4 delay not available)</td>
<td>7 ns (0.3V → 1V) (FO4 delay not available)</td>
<td>1.40 FO4 (0.3V → 1.8V)</td>
<td>1.15 FO4 (0.3V → 3.3V)</td>
</tr>
<tr>
<td>Energy per transition (fJ)</td>
<td>229 (0.3V → 2.5V)</td>
<td>136 (0.3V → 1.2V) (calculated from 5.44 nW @ 20 kHz)</td>
<td>5,800 (0.4V → 3V)</td>
<td>22 (0.3V → 1V)</td>
<td>588 (0.3V → 1.8V)</td>
<td>954 (0.3V → 3.3V)</td>
</tr>
<tr>
<td>Leakage power (pW)</td>
<td>475 (0.3V → 2.5V)</td>
<td>N/A</td>
<td>230 (0.4V → 3V)</td>
<td>7,000 (0.3 → 1V)</td>
<td>4,650 (0.3V → 1.8V)</td>
<td>970 (0.3V → 3.3V)</td>
</tr>
<tr>
<td>Delay with 3σ variation</td>
<td>4.76 FO4 (0.3V → 2.5V)</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>3.14 FO4 (0.3V → 1.8V) (simulation results)</td>
<td>2.31 FO4 (0.3V → 3.3V)</td>
</tr>
<tr>
<td>Area (µm²)</td>
<td>102.26</td>
<td>16.8</td>
<td>1880</td>
<td>1.38</td>
<td>99.79</td>
<td>153.01</td>
</tr>
</tbody>
</table>


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